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Thermal stability and electric properties of $Ba_{0.7}Sr_{0.3}TiO_3$ parallel plate capacitor with nano-Cr interlayer

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Abstract

A novel sandwich structure of $Ba_{0.7}Sr_{0.3}TiO_3$/Cr/$Ba_{0.7}Sr_{0.3}TiO_3$ (BST/Cr/BST) was sputtered onto Pt/Ti/SiO_2/Si substrate. With the insertion of a Cr layer, the leakage currents are decreased and the thermal stability of the specimens is enhanced. Temperature coefficient of capacitance (TCC) of specimens with BST(200 nm)/Cr(2 nm)/BST(200 nm) multifilms can achieve about 83% lower than those with BST (400 nm) monolayer. However, the dielectric constant of the BST(200 nm)/Cr(2 nm)/BST(200 nm) multifilms decreases to about 37% of that BST monolayer. The leakage current densities under an electric field of 125 kV/cm at 90 °C are 4×10^{-4} A/cm^2 and 9×10^{-1} A/cm^2 for BST (200 nm)/Cr (2 nm)/BST (200 nm) and monolayer BST (400 nm), respectively. X-ray diffraction results indicate the formation of a CrO_3 secondary phase after annealing at 700 °C or above in O_2 atmosphere. The root causes for the improvement of leakage currents and thermal stability with the insertion of nano-Cr interlayer are explored. The results show the insertion of Cr-nanolayer improves the electric properties for application in capacitors.

Keywords: BST thin films; Ferroelectric; Thermal stability; Capacitor

1. Introduction

Each successive DRAM generation has to maintain the same storage charge, while the area of the capacitor has significantly decreased. $Ba_xSr_{1-x}TiO_3$ (BST) thin film capacitor has been one of the promising DRAM cell candidates in the future generation. To satisfy the requirements of the next DRAM generation, BST thin films with considerably high dielectric constant can provide the sufficient storage charge. BST films also require the low leakage current, high breakdown field, high time-dependent dielectric breakdown (TDDB), and low fatigue and aging effects [1–3]. However, the junction temperatures of DRAM cell may range from room temperature to about 125 °C and the dielectric constant of BST films varies with operating temperature, as reported in previous works [4]. On the other hand, capacitors based on BST thin films have also shown great promise for the fabrication of the microwave components. It offers the advantages of integratability, low cost, and high speed [5,6].

The dielectric properties of the BST thin films can be modified with a Bi underlayer [7] and/or various dopants [8–10]. The Cr doping prepared using an alkoxide-based sol–gel method increases the grain size and the dielectric constant and reduces the leakage current of the BST films [9]. This is an on-going research, in our previous work [4], a novel sandwich structure of BST parallel plate capacitor with sputtered nano-Cr interlayer was found to lower the leakage current and temperature dependence of capacitance of the BST capacitor. However, the role that the nano-Cr interlayer plays on the dielectric properties of the BST films is unclear. In this study, the effects of annealing conditions on the electric properties and thermal properties of the sandwich structure are studied. The Cr/

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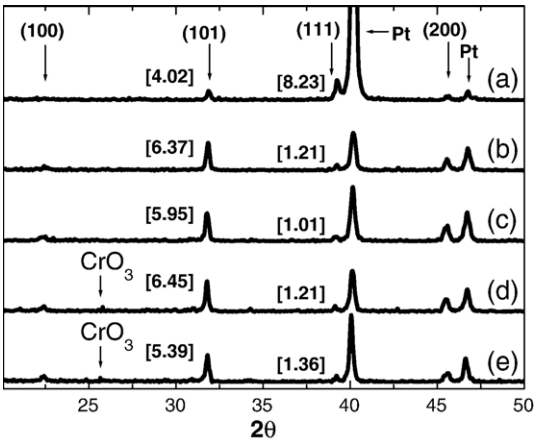

Fig. 1. X-ray diffraction patterns of specimens annealed at various conditions with and without the insertion of nano-Cr interlayer. (a) BST annealed at 800 °C in O_2; (b) BST/Cr/BST annealed at 700 °C in N_2; (c) BST/Cr/BST annealed at 700 °C in air; (d) BST/Cr/BST annealed at 700 °C in O_2; and (e) BST/Cr/BST annealed at 800 °C in O_2. Data in bracket [ ] are the peak ratios I(101)/I(100) or I (111)/I(100). The peaks at $2\theta = 39.76°$ and 46.24° are the Pt bottom electrode.

BST interfaces after annealing in various conditions are investigated and the root causes for the improvement of the dielectric properties are explored.

2. Experimental procedures

Multilayer specimen of Pt/$Ba_{0.7}Sr_{0.3}TiO_3$/Cr/$Ba_{0.7}Sr_{0.3}TiO_3$/Pt was employed to the novel sandwich structure for DRAM capacitor. The starting p-type Si (100) wafers were cleaned by the standard RCA cleaning process. After cleaning, a 100-nm SiO_2 film was grown on the Si substrate. A 10-nm Ti layer was sputtered onto the Si substrate. The bottom electrodes, 100-nm thick Pt films, were dc sputtered at room temperature. The first $Ba_{0.7}Sr_{0.3}TiO_3$ (BST) films were then deposited using an RF magnetron sputtering at a substrate temperature of 400 °C. The sputtering chamber was evacuated to a base pressure of 1×10^{-5} Torr. Then, all films were deposited at a constant pressure of 5×10^{-3} Torr which was maintained by a mixture of argon and oxygen at 9 sccm and 3 sccm, respectively. The RF power for the deposition of both the first and second BST films was 120 W (power density was 2.7 W/cm^2) and the thickness of BST films was about 200 nm. The nano-Cr interlayer was deposited (~2 nm) with a dc sputtering system at 100 W. The second BST films were then deposited. The BST/Cr/BST/Pt multifilms were annealed at 700 °C or 800 °C in various atmospheres (O_2, N_2, or air) for 1 h before deposition of the top Pt electrode.

The phase of the films was characterized by an X-ray diffractometer (XRD) (RU-H3R, Rigaku, Japan). A dual beam (focused ion beam and electron beam) system (Nova 200, FEI company, Japan) was employed to observe the surface morphology of BST thin films. An atomic force microscope (AFM) (NS3a controller with D3100 stage, Veeco Instruments Inc., U.S.A.) was employed to study the surface morphology and roughness of the films. An LCR meter (HP-4285, Hewlett Packard Co., U.S.A.) was employed to study the capacitance as a function of applied voltage and the voltage stability of the capacitors from 0 to 125 kV/cm were then calculated.

3. Results and discussion

The X-ray diffraction patterns of the BST films with and without nano-Cr interlayer annealed at various conditions are given in Fig. 1. All BST films show crystallized cubic phase. However, a diffraction peak appears at $2\theta = 25.92°$ and this peak is attributed to the formation of CrO_3 secondary phase after annealing BST/Cr/BST films at 700 °C and above in O_2 atmosphere. With the insertion of a 2-nm Cr interlayer, a preferred (101) orientation is found. As listed in Table 1, the peak ratio I(101)/I(100) increases from 4.0 for BST monolayer to 5.4–6.4 for BST with a 2-nm Cr interlayer and the (101) peak of the BST/Cr/BST specimens is narrower than that of BST monolayer. While the (111) orientation is suppressed, the peak ratios I(111)/I(100) of BST with 2-nm Cr interlayer range from

Table 1
Process parameters, XRD data, dielectric constant (k), surface roughness, TCC$^{\zeta}$, TCD$^{\zeta}$, and VCC$^{\zeta}$ (DC biased from 0 to 125 kV/cm) of the specimens in this study

Specimens			XRD peak ratio			Surface roughness (nm)	TCC (10^{-3}/°C)	TCD (10^{-3}/°C)	VCC (%)	$k/k_0^{\#\#}$ at 30 °C at 100 kHz
Dielectric films	Annealing temperature (°C)	Annealing atmosphere	I(101)/ I(100)	I(111)/ I(100)	Full width at half maximum*					
BST	800	O_2	4.02	8.23	0.20°	3.27	1.96	5.81	32.1	1.00
BST/Cr/BST	700	N_2	6.37	1.21	0.12°	5.09 [1.51]$^{\delta}$	2.05	2.87	0.8	0.95
BST/Cr/BST	700	air	5.95	1.01	0.18°	4.26 [4.11]$^{\delta}$	2.38	5.31	12.9	0.74
BST/Cr/BST	700	O_2	6.45	1.22	0.16°	3.27 [4.26]$^{\delta}$	1.39	12.11	2.7	0.61
BST/Cr/BST	800	O_2	5.39	1.32	0.12°	15.71 [3.27]$^{\delta}$	0.34	6.61	3.5	0.37
Undoped BST$^{\#}$	700	O_2	–	–	–	3.8	–	–	33	1.00
3 mol% Cr-doped BST$^{\#}$	700	O_2	–	–	–	7.8	–	–	42	1.14
5 mol% Cr-doped BST$^{\#}$	700	O_2	–	–	–	9.1	–	–	47	1.28

*: Full width at half maximum of peak (101).

$$\zeta : \mathrm{TCC} = \frac{C_{150°} - C_{30°\mathrm{C}}}{(150°\mathrm{C} - 30°\mathrm{C}) \times C_{30°\mathrm{C}}}, \mathrm{TCD} = \frac{\mathrm{DF}_{150°} - \mathrm{DF}_{30°\mathrm{C}}}{(150°\mathrm{C} - 30°\mathrm{C}) \times \mathrm{DF}_{30°\mathrm{C}}}, \mathrm{VCC} = \frac{C_{(E=0\mathrm{kV/cm})} - C_{(E=125\mathrm{kV/cm})}}{C_{(E=0\mathrm{kV/cm})}}$$

#: Data from Ref. [9].

δ: Surface roughness of Cr/BST.

##: The dielectric constant (k_0) are 323 for BST monolayer in this work and 386 for undoped BST [9].

1.0 to 1.3 which are much smaller than the peak ratio I(111)/I (100) (≈8.2) of BST monolayer annealed at 800 °C in O_2 atmosphere.

The BST monolayer annealed at 800 °C in O_2 exhibits uniform microstructure and an average grain size of about 150 nm, as shown in Fig. 2(a). Insertion of nano-Cr interlayer seems to reduce the average grain size of the BST films. The average grain size of BST/Cr/BST annealed at 700 °C in N_2 is about 30 nm and the microstructure is uniform (Fig. 2(b)). While heterogeneous microstructure is observed for BST/Cr/BST annealed at 700 °C and above in air or O_2. The formation of a secondary phase is found as shown in Fig. 2(c)–(e). The XRD results suggest the existence of a CrO_3 phase. It is suspected that the second phase as indicated in Fig. 2(c)–(e) is CrO_3, however, further analysis is underway to verify this point.

The root-mean-square (RMS) surface roughnesses of annealed BST, Cr/BST, and BST/Cr/BST films are given in Fig. 3. The surface roughness of BST monolayer is about 3.2 nm. Annealing in oxygen-containing atmosphere increases the surface roughness of the specimens with Cr nanolayer and the surface roughnesses range from 3.27 nm (BST/Cr/BST annealed at 700 °C in O_2) to 15.71 nm (BST/Cr/BST annealed at 800 °C in O_2). While annealing at 700 °C in N_2 atmosphere decreases the surface roughness of the specimens, the surface roughnesses of Cr/BST and BST/Cr/BST annealed at 700 °C in N_2 are 1.11 nm and 1.51 nm, respectively.

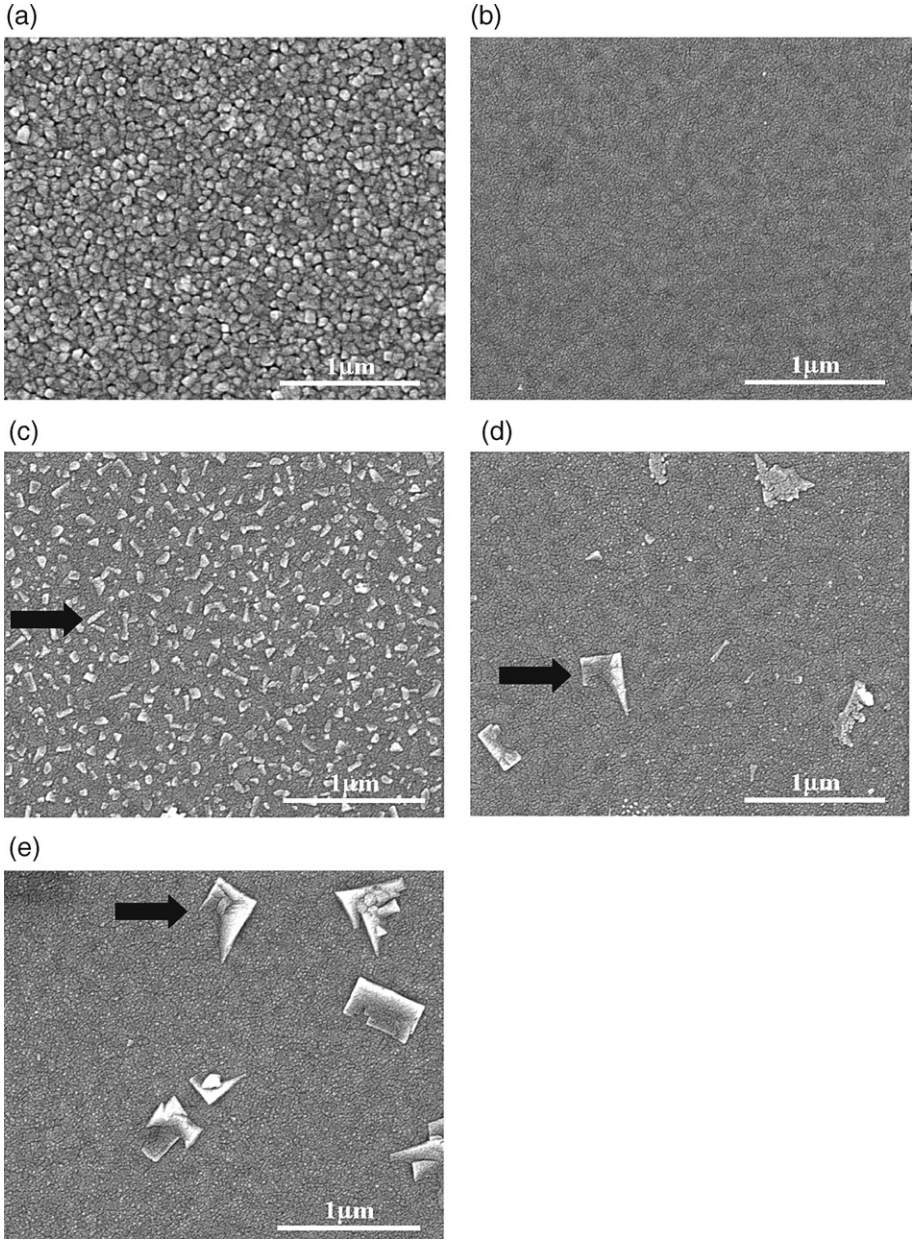

Fig. 2. Microstructure of (a) BST annealed at 800 °C in O_2; (b) BST/Cr/BST annealed at 700 °C in N_2; (c) BST/Cr/BST annealed at 700 °C in air; (d) BST/Cr/BST annealed at 700 °C in O_2; and (e) BST/Cr/BST/Pt annealed at 800 °C in O_2. Segregation of a second phase is observed in specimens annealed in air or O_2 as indicated by arrows in Fig. 2(c)–(e).

Specimens with smaller grain size exhibit smoother surface, as shown in Fig. 3. Also given in Fig. 3 are the surface roughness and grain size of Cr-doped BST films [9] for comparison. The BST films with Cr interlayer have smaller grain size and surface roughness than Cr-doped BST films, as indicated in Fig. 3.

Fig. 4 shows temperature dependence of the dielectric constant (k) and dissipation factor (DF) of specimens with and without Cr-nanolayer at 100 kHz. The dielectric constant decreases while the dissipation factor increases for most of the specimens with the insertion of Cr interlayer. It is believed that the presence of the CrO_3 layer affects both k and DF. The effects of CrO_3 second phase will be discussed in detail after a thorough interface analysis is completed. The thermal stability of the dielectric constant is enhanced with the implementation of the Cr interlayer. The temperature coefficient of capacitance (TCC) and the temperature of coefficient of dissipation factor (TCD) are defined as:

$$\mathrm{TCC} = \frac{C_T - C_{T_r}}{(T - T_r) \times C_{T_r}} \quad (1)$$

$$\mathrm{TCD} = \frac{\mathrm{DF}_T - \mathrm{DF}_{T_r}}{(T - T_r) \times \mathrm{DF}_{T_r}} \quad (2)$$

where T is temperature of interest (150 °C in this study), T_r is temperature of reference (30 °C in this study), C_T and C_{T_r} are the capacitances measured at T and T_r, and DF_T and DF_{T_r} are the dissipation factors measured at T and T_r, respectively. Most capacitors with BST/Cr/BST dielectric show smaller TCC than those with mono-BST dielectric. A TCC of 0.34×10^{-3}/°C is obtained for capacitors with BST/Cr/BST annealed at 800 °C in O_2 as compared to that of 1.96×10^{-3}/°C of that with BST monolayer, as listed in Table 1. The existence of CrO_3 secondary phase could be one of the reasons which reduce the temperature sensitivity of BST capacitor of the novel sandwich structure. However, it is subjected to further analysis. The insertion of Cr-nanolayer reduces the dissipation factor after 800 °C annealing in O_2. The DF of BST/Cr/BST annealed at 800 °C in O_2 is 8×10^{-3} which is smaller than that of BST monolayer of 2×10^{-2}.

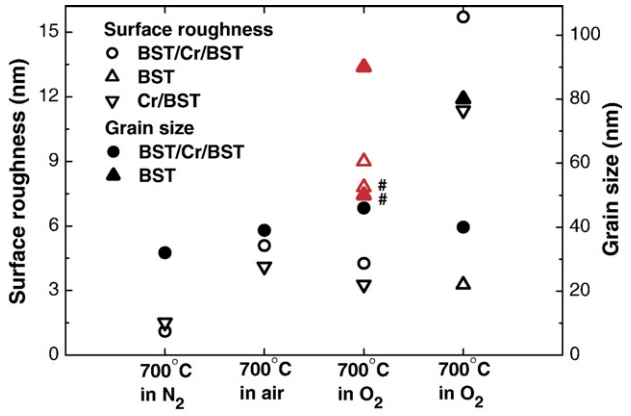

Fig. 3. Surface roughness (RMS) of BST, Cr/BST, and BST/Cr/BST samples under various annealing conditions. #: Data from Ref. [9] for 3 mol% Cr-doped BST thin films (200 nm). ζ: Data from Ref. [9] for 5 mol% Cr-doped BST thin films (200 nm).

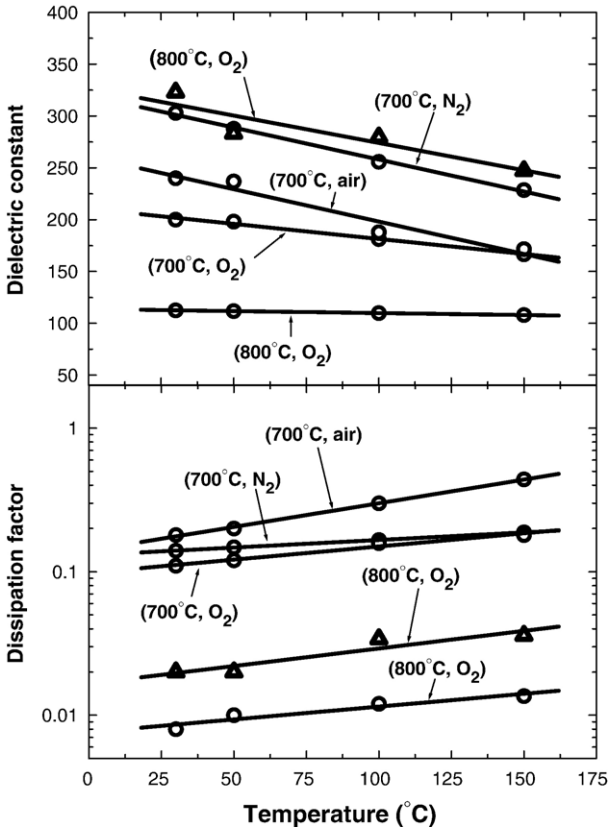

Fig. 4. Temperature dependence of the 100 kHz dielectric constant and dissipation factor of specimens in this study. Data in the parenthesis ( ) are annealing temperature and atmosphere for BST monolayer (ρ) and BST/Cr/BST (○), respectively.

The leakage current densities under an electric field of 125 kV/cm at 90 °C are 4×10^{-4} A/cm^2 and 9×10^{-1} A/cm^2 for BST(200 nm)/Cr(2 nm)/BST(200 nm) and monolayer BST (400 nm), respectively. The data show the leakage current ratio dramatically reduces to 4.4×10^{-4} by insertion of 2-nm Cr interlayer as an inter-medium layer onto BST sandwich structure, while BST/Cr/BST multifilms and BST monolayer were annealed at 800 °C in O_2 atmosphere. The data can be compared with the leakage current ratios of Cr-doped BST to undoped BST. The leakage current density ratios become 0.1 and 0.04 of 3 mol% Cr-doped BST to undoped BST and 5 mol% Cr-doped BST to undoped BST, respectively.

Table 1 summarizes some pertinent properties of specimens in this study. Data from Ref. [9] are also cited for comparison. The insertion of Cr-nanolayer decreases while the addition of Cr dopant [9] increases the dielectric constant (k) of BST films. The k value reduces to 0.37 of the BST monolayer for BST/Cr/BST annealed at 800 °C in O_2, while a 28% raise in k is obtained for 5 mol% Cr-doped BST film. The VCC of BST films is improved with the implementation of Cr-nanolayer. A 3.5% dielectric constant change from 0 to 125 kV/cm is obtained for specimens with BST/Cr/BST annealed at 800 °C in O_2 as compared to 32.1% of specimens with BST monolayer.

4. Conclusions

In this study, parallel plate capacitors with BST/Cr/BST multilayer dielectric are investigated. The insertion of the 2 nm Cr improves both the thermal and voltage stability of the capacitors. A TCC of 0.34×10^{-3}/°C from 30 °C to 150 °C is obtained for BST/Cr/BST annealed at 800 °C in O_2 as compared to that of 1.96×10^{-3}/°C for BST films. Besides, a VCC of 3.5% from 0 to 125 kV/cm (DC biased) is obtained for BST/Cr/BST annealed at 800 °C in O_2 as compared to that of 32.1% for BST films.

However, the dielectric constant decreases from 323 to 112 with the implementation of the Cr layer. Formation of a CrO_3 second phase is obtained for BST/Cr/BST films annealed in air or O_2 and presumably is one of the reasons for the change in the dielectric properties.

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