AIP Applied Physics Letters

Sol-gel-derived double-layered nanocrystal memory

Fu-Hsiang Ko, Hsin-Chiang You, and Tan-Fu Lei

Citation: Applied Physics Letters **89**, 252111 (2006); doi: 10.1063/1.2416248
View online: http://dx.doi.org/10.1063/1.2416248
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/89/25?ver=pdfcov
Published by the AIP Publishing

Articles you may be interested in

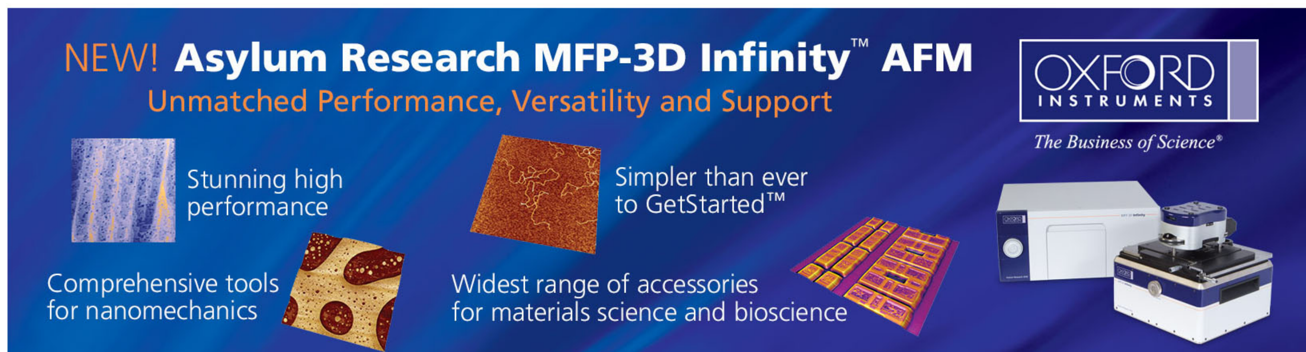
A TiAl 2 O 5 nanocrystal charge trap memory device
Appl. Phys. Lett. **97**, 143504 (2010); 10.1063/1.3496437

Device characteristics of HfON charge-trap layer nonvolatile memory
J. Vac. Sci. Technol. B **28**, 1005 (2010); 10.1116/1.3481140

A high- k Tb 2 TiO 5 nanocrystal memory
Appl. Phys. Lett. **96**, 102904 (2010); 10.1063/1.3354027

Novel coexisted sol-gel derived poly-Si-oxide-nitride-oxide-silicon type memory
J. Vac. Sci. Technol. B **25**, 2568 (2007); 10.1116/1.2794327

Droplet evaporation-induced ferritin self-assembled monolayer as a template for nanocrystal flash memory
Appl. Phys. Lett. **90**, 193512 (2007); 10.1063/1.2737362



This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Thu, 01 May 2014 01:40:47

Sol-gel-derived double-layered nanocrystal memory

Fu-Hsiang Ko[a)]
Institute of Nanotechnology, National Chiao Tung University, Hsinchu 300, Taiwan

Hsin-Chiang You and Tan-Fu Lei
Institute of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan

(Received 26 September 2006; accepted 13 November 2006; published online 20 December 2006)

The authors have used the sol-gel spin-coating method to fabricate a coexisting hafnium silicate and zirconium silicate double-layered nanocrystal (NC) memories. From transmission electron microscopic and x-ray photoelectron spectroscopic analyses, the authors determined that the hafnium silicate and zirconium silicate NCs formed after annealing at 900 °C for 1 min. When using channel hot electron injection for charging and band-to-band tunneling-induced hot hole injection for discharging, the NC memories exhibited superior V_{th} shifting because of the higher probability for trapping the charge carrier. © *2006 American Institute of Physics*.
[DOI: 10.1063/1.2416248]

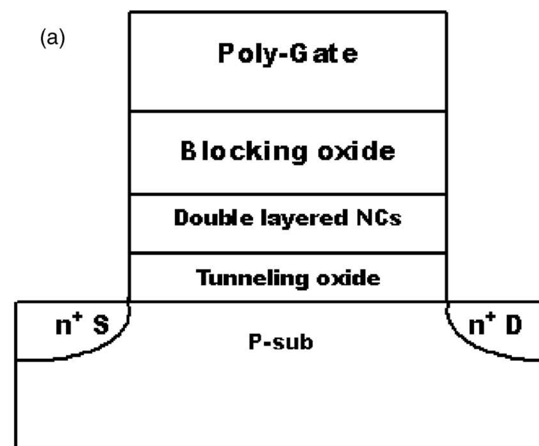
Conventional flash memory devices possess a floating gate structure in which the charge carrier is stored in a polysilicon film.[1] Because the storage charge leaks readily when the tunneling oxide layer is thinner than 85 nm, floating gate structures face severe scaling issues resulting from defects in the tunneling oxide.[2] A discrete single-layered nanocrystal (NC) memory was proposed recently as a replacement of the single poly-Si film of a floating gate structure.[3–7] NC memories can preserve the trapped charge efficiently—i.e., they avoid the problems associated with the charge loss of conventional flash memories—while also displaying desirable features such as fast program/erase speeds, low programing potentials, and high endurance.[8,9]

Many methods have been developed recently for the preparation of a range of NC memories using physical vapor deposition,[4,5] chemical vapor deposition (CVD),[6] and ion beam synthesis.[7] Wang *et al.*[4] formed Ge NCs through the cosputtering of Ge, Al_2O_3, and HfO_2. Yeh *et al.*[5] deposited a nickel layer through electron beam evaporation; prior to forming $NiSi_2$ NCs through annealing at 900 °C, an amorphous Si film was deposited. Liu *et al.*[6] self-assembled SiGe NCs from a mixture of GeH_4 and Si_2H_6 gases in a room-temperature CVD system. Muller *et al.*[7] implanted Si^+ ions into an SiO_2 layer to form Si NCs.

In addition to these versatile deposition methods for forming NCs, an alternative single-layer NC preparation technique—using a sol-gel spin-coating method—was published recently.[10] During NC formation through spin coating, the sol-gel system of interest was blended in the solution. The most valuable feature of using this sol-gel method is that the precursors and equipment are relatively cheap. We became interested in investigating whether double-layered NCs would perform better than single-layered NCs memories.

In this study, we used a sol-gel spin-coating method to fabricate a double-layered NC memory. $HfCl_4$ (99.5%, Aldrich), $ZrCl_4$ (99.5%, Aldrich), and $SiCl_4$ (99.5%, Aldrich) precursors were dissolved in isopropanol (IPA) (Fluka; water content: <0.1%) to prepare a mother solution in which the $HfCl_4:ZrCl_4:SiCl_4$ molar ratio was 1:1:1. We combined $HfCl_4$, $ZrCl_4$, and $SiCl_4$ to fabricate coexisting hafnium silicate ($HfSi_xO_y$) and zirconium silicate ($ZrSi_mO_n$) NC memories.

Figure 1(a) illustrates the fabrication of the sol-gel spin-coating NC memories, beginning with a local oxidation of silicon isolation process on a *p*-type (100) 150 mm silicon



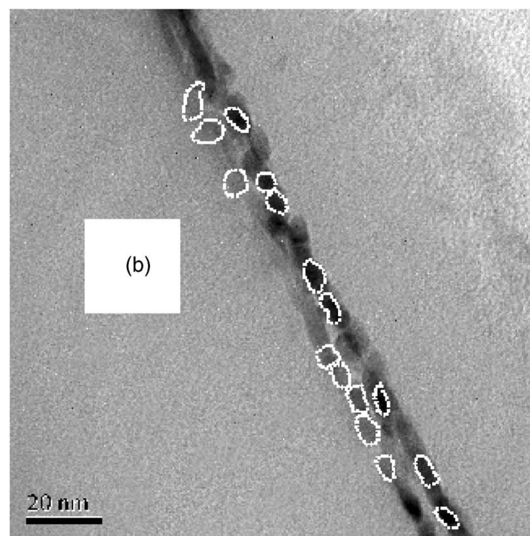


FIG. 1. (a) Device structure of the double-layered NC memory. (b) TEM image of hafnium silicate and zirconium silicate NCs.

a)Electronic mail: fhko@mail.nctu.edu.tw

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Thu, 01 May 2014 01:40:47

 © 2006 American Institute of Physics

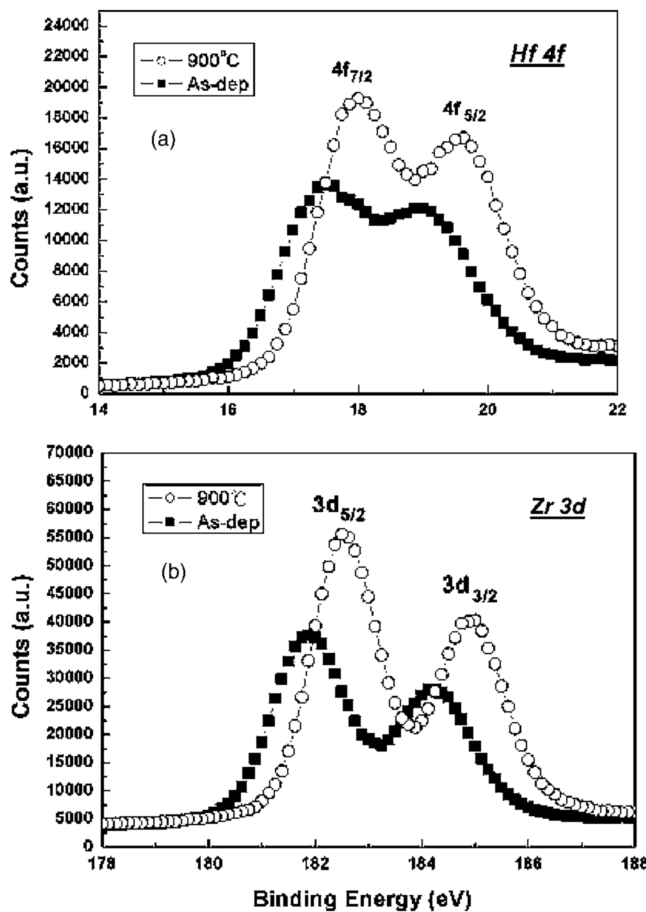


FIG. 2. (a) Hf 4*f* and (b) Zr 3*d* XPS spectra of as-deposited and 900 °C-annealed samples.

substrate. A 4-nm-thick tunneling oxide was grown thermally in a furnace at 925 °C. The charge trapping layer was deposited through spin coating at 3000 rpm for 60 s at ambient temperature (25 °C) using a TEL Clean Track Model-MK8 apparatus (Japan). After spin coating, the wafer was subjected to rapid thermal annealing at 900 °C for 60 s in an O_2 ambient to form the coexisting $HfSi_xO_y$ and $ZrSi_mO_n$ NC memory. A 30-nm-thick blocking oxide was deposited through low-pressure chemical vapor deposition tetraethylorthosilicate (LPCVD TEOS), followed by deposition of a 200-nm-thick poly-Si gate. After the LPCVD TEOS deposition, the TEOS oxide was densified in a N_2 ambient by annealing at 900 °C for 30 s. Finally, gate patterning, source/drain implanting, and the remaining steps of the complementary metal-oxide semiconductor processes were performed to fabricate the double-layered NC memory.

The high-resolution transmission electron microscopy image in Fig. 1(b) clearly depicts the transformation of sol-gel film into NCs after annealing at 900 °C for 60 s; we observe two differently colored NCs in this image. We used x-ray photoelectron spectroscopy (XPS) to characterize the nature of the chemical bonding in the NCs. Figure 2 provides a comparison of the XPS results for (a) Hf 4*f* and (b) Zr 3*d* bonding in the as-deposited (as-dep) and 900 °C-annealed samples. The Hf 4*f* peaks for the hafnia film (as-dep) appeared at 17.4 and 19 eV, while the Zr 3*d* peaks for the zirconia film (as-dep) appeared at 181.9 and 184.3 eV. Interestingly, these peaks for both Hf 4*f* and Zr 3*d* shifted toward higher bonding energies after annealing to form the NCs.

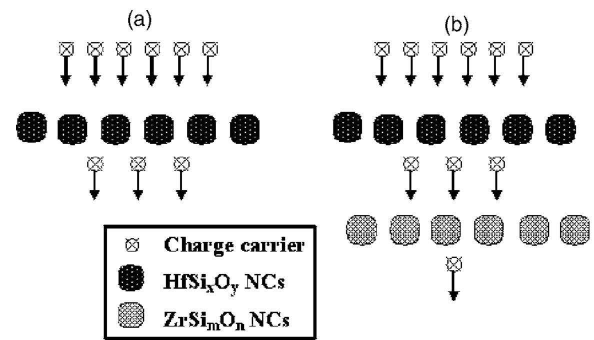


FIG. 3. Trapping model for the (a) single- and (b) double-layered NC memories.

This observation suggests that the oxygen atoms of Hf–O and Zr–O bonds reacted with their nearby Si atoms, forming hafnium silicate and zirconium silicate.[11,12] The darker NCs in Fig. 1(b) are those of high-molecular-weight hafnium silicate; the bright NCs are formed from low-molecular-weight zirconium silicate.

NC memories use channel hot electron injection (CHEI) for charging and band-to-band tunneling-induced hot hole injection (BTBHHI) for discharging. The charge and discharge speeds are closely related to the trapping probability[13,14] of the NCs. Briefly, the electron carrier in Fig. 3(a) can be trapped in the $HfSi_xO_y$ NCs (e.g., see Ref.

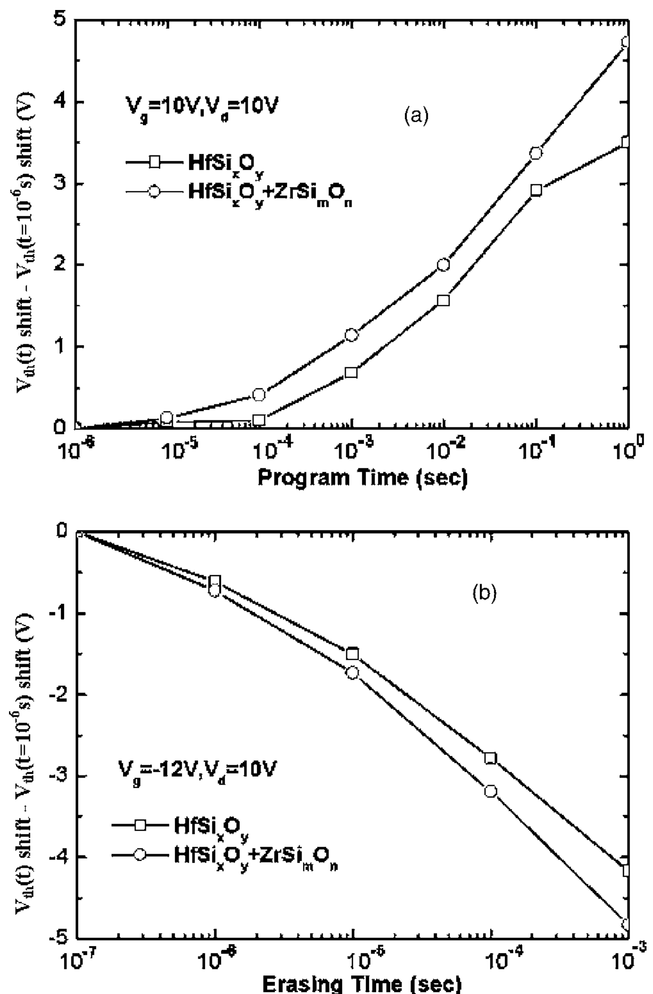


FIG. 4. (a) Program and (b) erase speeds of the single- and double-layered NC memories.

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Thu, 01 May 2014 01:40:47

10) during the charging period. As the hole carrier is injected into the NCs, the trapping capability can influence the discharging speed. In other words, the double-layered NCs in this study may offer a higher trapping probability for the charge carrier than do the single-layered NCs. Figure 3(b) illustrates the trapping model through which the double-layered NCs improve the hole/electron trapping probability.

Figure 4(a) displays the charging speeds of both a single-layered memory[10] and the double-layered NC memory. We used CHEI to program (charge) the system under conditions of V_g and V_d both being 10 V. Obviously, the double-layered NC memory exhibited a larger value of "$V_{\mathrm{th}}(t)$ shift–$V_{\mathrm{th}}(t=10^{-6}$ s) shift" than did the single-layered NC memory. For example, the values of $V_{\mathrm{th}}(t)$ shift–$V_{\mathrm{th}}(t=10^{-6}$ s) shift at 1 ms were 0.68 and 1.14 V for the single- and double-layered NC memories, respectively; i.e., the value of $V_{\mathrm{th}}(t)$ shift–$V_{\mathrm{th}}(t=10^{-6}$ s) shift was improved by 68%, presumably because of the better charge carrier trapping probability of the latter system. We are unaware of any other report describing the performance for double-layered NC memories. Figure 4(b) displays the discharging speeds of the single-[10] and double-layered NC memories. We used BTBHHI to erase (discharge) the system under conditions where is V_g and V_d were −12 and +10 V, respectively. Again, the double-layered NC memory exhibited a significant value of $V_{\mathrm{th}}(t)$ shift–$V_{\mathrm{th}}(t=10^{-6}$ s) shift relative to that of the single-layered NC memory; we also attribute this phenomenon to the higher trapping probability of the double-layered NCs.

In summary, we have used a sol-gel spin-coating method to fabricate a double-layered NC memory. From transmission electron microscopy (TEM) and XPS analyses, we confirmed that the NCs consisted of hafnium silicate and zirconium silicate. The double-layered NCs in this study provided a higher trapping probability for charge carriers than did the corresponding single-layered NC devices.

This study was supported financially by the National Science Council, Taiwan, through Contract No. NSC 95-2113-M-009-032-MY3 and NSC 95-2120-M-009-003.

[1] Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, IEEE Trans. Electron Devices **49**, 1606 (2002).
[2] B. D. Salvo, C. Gerardi, R. V. Schaijk, S. A. Lombardo, D. Corso, C. Plantamura, T. Serafino, G. Ammendola, M. V. Duuren, P. Goarin, W. Y. Mei, K. V. D. Jeugd, H. Baron, M. Gély, P. Mur, and S. Deleonibus, IEEE Trans. Device Mater. Reliab. **4**, 377 (2004).
[3] Y.-N. Tan, W.-K. Chim, B. J. Cho, and W.-K. Choi, IEEE Trans. Electron Devices **51**, 1143 (2004).
[4] Y. Q. Wang, J. H. Chen, W. J. Yoo, Y.-C. Yeo, S. J. Kim, R. Gupta, Z. Y. L. Tan, D.-L. Kwong, A. Y. Du, and N. Balasubramanian, Appl. Phys. Lett. **84**, 5407 (2004).
[5] P. H. Yeh, C. H. Yu, L. J. Chen, H. H. Wu, P. T. Liu, and T. C. Chang, Appl. Phys. Lett. **87**, 193504 (2005).
[6] Y. Liu, S. Tang, and S. K. Banerjee, Appl. Phys. Lett. **88**, 213504 (2006).
[7] T. Muller, K.-H. Heinig, W. Moller, G. Bonafos, H. Coffin, N. Cherkashin, G. B. Assayag, S. Schamm, M. Tence, and C. Colliex, Appl. Phys. Lett. **85**, 2373 (2004).
[8] M. She and T.-J. King, IEEE Trans. Electron Devices **50**, 1934 (2003).
[9] M. Takata, S. Kondoh, T. Sakaguchi, H. Choi, J.-C. Shim, H. Kurino, and M. Koyanagi, Tech. Dig. - Int. Electron Devices Meet. **2003**, 553.
[10] H.-C. You, T.-H. Hsu, F.-H. Ko, J.-W. Huang, and T.-F. Lei, IEEE Electron Device Lett. **27**, 644 (2006).
[11] G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys. **87**, 484 (2000).
[12] P. D. Kirsch, C. S. Kang, J. Lozano, J. C. Lee, and J. G. Ekerdt, J. Appl. Phys. **91**, 4353 (2002).
[13] W.-T. Lu, P.-C. Lin, T.-Y. Huang, C.-H. Chien, M.-J. Yang, I.-J. Huang, and P. Lehnen, Appl. Phys. Lett. **85**, 3525 (2004).
[14] M. Ishii and B. Hamilton, Appl. Phys. Lett. **85**, 1610 (2004).

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Thu, 01 May 2014 01:40:47