NEW UNDERSTANDING OF METAL-INSULATOR-METAL (MIM) CAPACITOR DEGRADATION BEHAVIOR

Chi-Chao Hung, Anthony S. Oates, H. C. Lin*, Percy Chang, J.L. Wang, C.C. Huang, and Y.W. Yau
Taiwan Semiconductor Manufacturing Company, Ltd.
*Department of Electronics Engineering, National Chiao Tung University
9, Creation Rd.1, Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.
Phone: +886-3-5636688; Fax: +886-3-5662051; e-mail: cchungm@tsmc.com

ABSTRACT

This work provides an innovative understanding of MIM capacitor degradation behavior under a wide range of constant current stress (CCS) conditions. It was found that capacitance degrades with stress, but the behavior of the degradation strongly depends on the stress current density. At high stress levels, the capacitance increases logarithmically as the injection charge increases until dielectric breakdown occurs. At lower stress conditions, the degradation rate is proportional to the stress current, and reverses after a certain period of time. A metal-insulator interlayer is observed to explain this reversal phenomenon. [*Keywords*: MIM capacitor, capacitance degradation, charge trapping, metal-insulator interlayer]

INTRODUCTION

Metal-insulator-metal (MIM) capacitors embedded in the backend inter-level dielectric layers as passive components are widely used for analog and RF applications. The stability of MIM capacitors is an important issue when considering the accuracy of analog functions. For applications requiring extreme precision, such as A/D and D/A converters, only a ±0.01% mismatch is allowed [1]. However, the capacitance degradation behavior of a single capacitor has not been well characterized. Besset et al. depicted the MIM capacitance variation under electrical stress, and observed that the relative capacitance variation was dependent on the injected charge, but was independent of stress current [2].

In this study, the degradation of SiO_2 MIM capacitors was investigated under a wide range of stress conditions. This work provides an innovative understanding of MIM capacitor degradation behavior under a wide range of constant current stress (CCS) conditions.

EXPERIMENTAL

A 380Å SiO_2 MIM structure with a 1fF/μm^2 capacitance and an area of 6000μm2 was used in this study. A SiO_2 layer was deposited using plasma enhanced chemical vapor deposition (PECVD). AlCu and TiN/AlCu layers were used as the top and bottom electrodes of the MIM, respectively. The samples were stressed under a constant current in a range of 0.01-20nA, corresponding to a current density of 0.17-333μA/cm^2, at various temperatures from 25 to 75°C in order to study the capacitance variations under different electrical stress conditions.

RESULTS AND DISCUSSION

To determine the degradation, a capacitor with an initial capacitance C_0 was measured periodically while under stress conditions. Figure 1 shows the relative capacitance variation, $(C-C_0)/C_0$, as a function of the injected charge at 25°C for various constant current stress values from 0.01 to 20nA, corresponding to a current density of 0.17-333μA/cm^2. In general, the relative capacitance variation increases logarithmically as the injected charge increases, and is similar to the charge trapping behavior in dielectric film [3], which implies a correlation between the capacitance variation and the charge trapping.

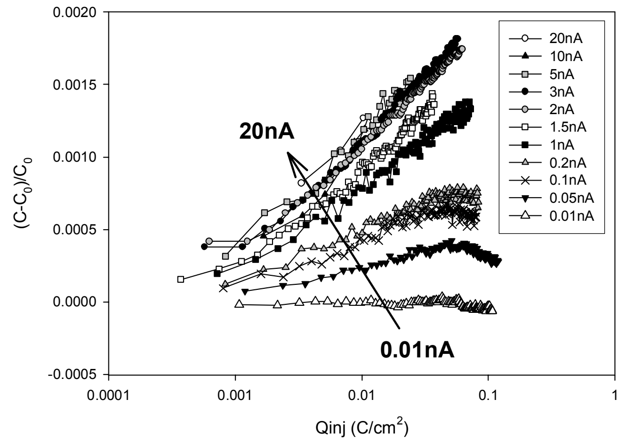


Figure 1. Relative capacitance variation as a function of the injected charge at 25°C for various CCS values from 0.05 to 20nA

In an MIM system, which is composed of two parallel metallic plates with an insulator thickness *d*, the capacitance is calculated by using:

$$C = \varepsilon \frac{A}{d} \quad (1)$$

where ε is the permittivity of the insulator, and *A* is the area of the plate. The capacitance is proportional to the dielectric permittivity. Moreover, the dielectric local permittivity ε can be expressed as a function of the trapped charge [4].

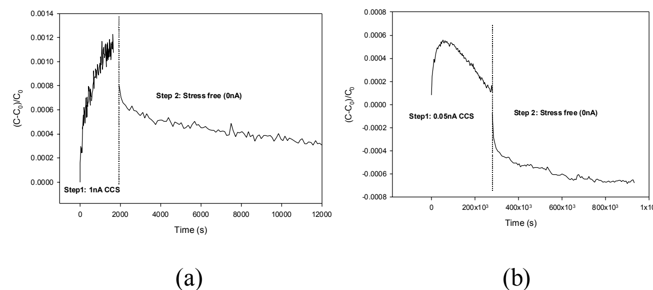
$$\varepsilon = \varepsilon_{SiO_2} + N_e \cdot \frac{8 \cdot \alpha \cdot q^2}{\pi \cdot A^3 \cdot K^e} + N_h \cdot \frac{8 \cdot \alpha \cdot q^2}{\pi \cdot A^3 \cdot K^h} = \varepsilon_{SiO_2} + \varepsilon_q \quad (2)$$

where α is the atomic polarizability of the dielectric, *q* is the unit charge, *A* is the distance between the molecules, and K^e / K^h and N^e / N^h are the potential energy profile of the trap and the density of the trapped charges inside the dielectric for the electron and the hole, respectively. The increase in capacitance can be correlated to the

generation of new dipoles in the dielectric as a result of charge trapping [2,5].

The dependence of relative capacitance variations on the different stress-current levels at a 0.01C/cm^2 injected charge can also be observed in Figure 1. When applying a current greater than 3nA, the variation is injected-charge dependent and stress current independent, as other studies have observed [2]. However, in lower current conditions, the variations are shown to be not only dependent on the injected-charge, but also dependent on the stress-current. High current stress is applied through higher voltage, and hence, the charge carriers are more energetic and can create traps in the dielectric. This may explain the differences in behavior of stressed currents greater than 3nA.

It was noted that the capacitance in most samples continued to increase until such time that a breakdown occurred. But for lower-stressed current conditions that are able to sustain stress for longer durations without breaking down, such as 0.1 and 0.05nA, corresponding to a current density of 1.66 and 0.83μA/cm^2, respectively, a reversal in capacitance variation was observed after a certain period of time, as shown in Figure 1. When applying a current density greater than 1nA, a breakdown occurred in the sample and further stressing could not continue, thus the reversal phenomenon was not observed in samples subjected to higher stress levels due to the relatively short stress time.

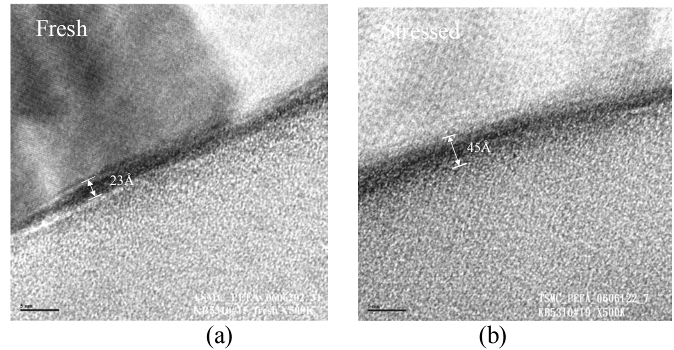


(a) (b)

Figure 2 Time dependence of the capacitance variation during on and off stress for I = (a) 1 and (b) 0.05 nA stress conditions

To evaluate the capacitance changes after detrapping, a 2-step experiment was performed. Figure 2(a) shows the time dependence of the capacitance variation during both on and off stress at 1nA. Once the stress bias is removed, the capacitance begins to decrease rapidly. The post-stress capacitance variation appears to have a saturation-like behavior after the initial rapid decrease, which demonstrates that the capacitance decrease is associated with the detrapping of the previously trapped charge. For lower stress conditions, together with the variation reversal indicated in Figure 2(b), the capacitance also decreases when the stress bias is removed, and culminates at a lower value than the initial capacitance value, which indicates that the capacitance decreases intrinsically when the effect of the trapped charge is not considered.

Figure 3 shows the TEM cross-sectional images at a magnitude of 500K for both a fresh sample and a sample that had been stressed for an extended period. An interlayer is observed between the top AlCu electrode and the SiO_2 dielectric. The interlayer grows thicker during the stress. A thicker interlayer results in a lower capacitance, which influences the total capacitance of the MIM system, which can explain the capacitance reversal phenomenon in a capacitor under long-term stress conditions.



(a) (b)

Figure 3. TEM cross-sectional images for (a) a fresh sample and (b) a sample that was stressed for an extended period

As shown in Figure 1, the maximum degradation of a single SiO_2 capacitor is about 0.2%. This value implies that mismatch degradation may possibly be an issue for high precision analog applications. However, the stress conditions used in this study are not realistic and are much higher than real use conditions. But for materials that have more obvious charge trapping properties, the degradation might be a concern when considering the accuracy of analog functions that require extreme precision.

CONCLUSION

The degradation of 380Å SiO_2 MIM capacitors under a wide range of constant current stress was investigated in this study. It was observed that differences in behavior occur under both high- and low-current stress conditions. Oxide trapped charges increase the local permittivity, thus leading to an increase in capacitance. At lower stress conditions, the degradation reversed after a certain period of time. The capacitance culminates at a lower value than the initial capacitance value when the stress bias is removed after the reversal, which indicates that the capacitance decreases intrinsically when the effect of the trapped charge is not considered. The decrease in capacitance may arise from a growth in the interlayer between the metal electrode plate and the dielectric. In most normal use conditions, the 380Å SiO_2 MIM capacitor will not be vulnerable to degradation. But for materials that have more obvious charge trapping properties, the degradation may be an issue for high precision analog applications.

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