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Effect of gate metal on polymer transistor with glass substrate

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Poly(3-hexylthiophene) (P3HT) field-effect transistors (FETs) are fabricated on glass substrates with SiO_2 as a gate dielectric over the gate. Indium tin oxide (ITO), Al, and Cr are employed as gate metals. For spin-coated FET, the mobility increases from 10^{-4}–10^{-5} cm^2/V s for ITO and Al gates to 10^{-2} cm^2/V s for Cr gate. After O_2 plasma treatment, the SiO_2 roughness can be made as low as 0.7 nm. The mobility is further improved up to 0.3 cm^2/V s by dip-coating P3HT. ″Crossed rods″ such as morphology can be observed in dip-coated FET with high mobility, indicating high degree of self-assembly facilitated by the flat SiO_2 surface over Cr gate. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2403921]

Over the recent years, organic/polymeric semiconductors have received considerable attention as the active channel materials for thin film field-effect transistors (FETs). In particular, soluble polymer semiconductors have attracted tremendous interests owing to the fact that these materials can be easily spin coated to form electronics on glass or plastic substrates, with the advantages of a large-area coverage, structural flexibility, room-temperature processing, and low cost. Among the various polymers studied poly (3-hexylthiophene) (P3HT) has become one of the most promising candidates for organic field-effect transistors due to its self-assembling properties to reach relatively high mobility.[1] The microstructure in P3HT is shown to be affected by regioregularity (RR),[2] molecular weight (MW),[3] solvent,[4] film-formation method,[5] and blends with small molecules[6] or polymers.[7,8] High field-effect mobility of 0.5 cm^{2}V s (Ref. 6) has been demonstrated on Si substrates with high-quality thermal oxide as the gate dielectric.

It is well known that the morphology of the gate dielectric is a crucial factor to determine the carrier mobility in a polymer FET. Good self-assembly of P3HT occurs only on atomically smooth substrate. Thermally grown SiO_2 films on Si substrates have such a smooth surface and excellent insulating characteristics to achieve better performance than other gate dielectrics. However, from the perspective of application it is highly desirable to fabricate polymer FET over glass or plastic substrates instead of silicon due to the requirements of flexibility, light transparency, and low cost. Employing bottom-contact FET using glass substrate, a mobility of 0.06 cm^2/V s was achieved.[9] However, the leakage current through the gate dielectric significantly reduces the on/off ratio. Dielectric films deposited on a glass substrate by the commonly used chemical vapor deposition (CVD) or sputtering methods suffer from porosity and polar groups such as Si–H, O–H, and Si–OH.[10] In fact, the low thermal tolerance and uneven surface morphology of the glass sub-strate itself partially account for the poor SiO_2 quality and device performance. Our aim in this work is to demonstrate that high FET mobility and reproducibility can nevertheless be achieved on glass substrates. Even though the gate metal has no direct contact with the active polymer, it turns out that the surface of atmospheric pressure CVD (APCVD) SiO_2 depends sensitively on the gate metal underneath. With proper choice of gate metal the performance of polymer transistor can match the best on Si substrate. Such high-performance polymer FET can be combined with polymer light-emitting diode to realize all-polymer active matrix display on glass substrate.[11]

The P3HT batches with head-to-tail fraction greater than 98.5% and high molecular weight M_w of 84 000 are used as received from Aldrich. 0.2 μm filtered solutions of P3HT in high-purity chloroform from Merck were made with concentrations of 0.5, 0.13, 0.08, and 0.06 mg/ml for dip coating and with a concentration of 5 mg/ml for spin coating. Prior to filtration the solutions were always annealed to 50 °C for at least 10 min in order to increase their solubility and attain the homogeneity of the films.

Three types of gate electrodes are studied in our cases: Indium tin oxide (ITO), Al, and Cr. All the three cases start from an ITO-coated glass from commercial source. For ITO gate transistors the gate electrode is defined by etching process using aqua regia (mixture of hydrochloric acid and nitric acid, HNO_3:HCL:H_2O=1:12:12). Substrates were preliminarily cleaned by standard wet process with acetone, isopropanol, and de-ionized water. For the other two gate metals Al and Cr films are evaporated on top of the glass substrates as the gate electrodes. SiO_2 film with 300 nm thickness is deposited over the three kinds of gates by APCVD as the gate dielectric layer. Au source-drain contacts were thermally evaporated on top of the APCVD SiO_2 surface and the drain/source electrodes of 5 μm channel length and 200 μm width were achieved using the standard photolithographic lift-off process. All the samples are treated by UV ozone to obtain hydrophilic surface. O_2 plasma treatment is employed to reduce the SiO_2 surface roughness. Prior to deposition of the

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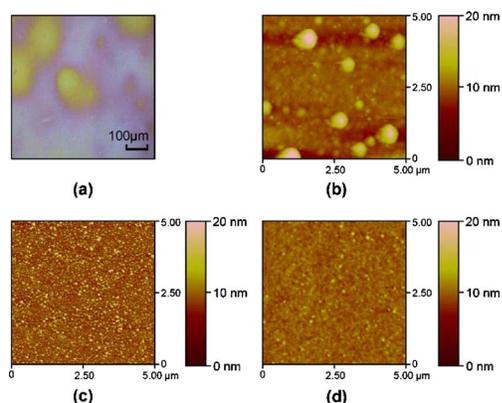
FIG. 1. (Color online) (a) Optical image of SiO$_2$ gate insulator surface on ITO gate electrode. [(b)–(d)] AFM topographic images of SiO$_2$ gate insulator surface based on different gate metallic electrodes. (b) is for Al (roughness 9.5 nm). (c) is for Cr before O$_2$ plasma treatment (roughness 2.6 nm). (d) is for Cr after O$_2$ plasma treatment (roughness 0.75 nm).

TABLE I. Comparison of surface roughness of oxide, mobility, and on/off ratio with different substrate conditions and deposition methods. (I), (II), (III), (IV), and (V) spin-coated P3HT films; (VI) and (VII) dip-coated P3HT films.

Sample	Gate	Oxide roughness (nm)	Mobility (cm^2/V s)	On/off ratio
(I)	ITO	3.3	10^{-5}–10^{-6} (unstable)	<100
(II)	Al	9.5	6.3×10^{-4}	970
(III)	Cr	2.6	8.8×10^{-4}	750
(IV)	Cr (after O$_2$ plasma)	1.2	3.3×10^{-3}	2 200
(V)	Cr (after O$_2$ plasma)	0.7	1.1×10^{-2}	10 000
(VI)	Cr (after O$_2$ plasma)	1.2	5.5×10^{-2}	320
(VII)	Cr (after O$_2$ plasma)	0.7	3.0×10^{-1}	1 100

P3HT, the hexamethyldisilazane (HMDS) layer is spun on to convert the hydrophilic surface to hydrophobic surface, upon which P3HT is ready to self-assemble into microcrystalline structures.[1] HMDS is then baked at a range from 30 to 110 °C to get better adhesion and lower surface roughness. From the atomic force microscope (AFM) topographic images, there is an optimal baking temperature around 50–70 °C, with less clusters and better surface morphology.

P3HT films are deposited on HMDS by either spin-coating or dip-coating methods. In the case of dip-coated P3HT transistors, the samples are dipped vertically into the P3HT chloroform solution and extracted at a linear rate of 32 μm/s using a controlled stepping motor. During dip coating all the samples are kept in inert atmospheres with O$_2$/H$_2$O levels below 0.1 ppm. After coating, the films were dried in vacuum (10^{-3} torr) for more than 24 h to remove any residuals of solvent being used. Finally, the FET is packaged in N$_2$ ambient and the FET characteristics of all samples were measured by a high impedance HP 4157 parameter analyzer under ambient.

Figure 1 shows the images of SiO$_2$ layer over various gate electrodes including (a) ITO, (b) Al, and (c) and (d) Cr. Optical microscope is used for (a) whereas AFM (Digital Instruments Dimension 3100) is used for (b), (c), and (d). Speckles of 100 μm scale can be seen in Fig. 1(a) for SiO$_2$ over ITO. The heights of regions with different colors differ by as much as 30 nm. Such speckles show up for ITO glasses from different commercial sources with varied patterns. We therefore attribute this to the intrinsic chemical stability of ITO in the high-temperature reaction chamber for SiO$_2$ APCVD growth. No such large-scale speckles are observed for SiO$_2$ over Al and Cr gates. However, the topographic AFM image of SiO$_2$ on Al in Fig. 1(b) shows formation of hillocks. The main cause of the hillocks is the large stress mismatch between Al and the glass substrate originated from the difference in thermal expansion coefficients.[12] Indeed, the APCVD oxide growth temperature is as high as 400 °C. The root-mean-square roughness of SiO$_2$ is up to 9.1 nm due to the hillocks. It turns out that the problems of ITO and Al gates can be solved by using Cr, which is chemically stable during the APCVD reaction and does not exhibit hillocks on glass due to good adhesion. The AFM image of the as-grown SiO$_2$/Cr surface is shown in Fig. 1(c). The roughness becomes 2.5 nm and no hillocks are seen. Using O$_2$ plasma treatment, the roughness of SiO$_2$/Cr surface can be further reduced to as low as 0.75 nm, as shown in Fig. 1(d). Note that the hillocks in SiO$_2$/Al surface are too robust to be eliminated by O$_2$ plasma.

It is well known that the mobility of polymer FET is very sensitive to the interface roughness. A smooth gate dielectric promotes structure ordering in the polymer active layer, which improves the carrier mobility.[13] Comparison for P3HT transistor characteristics with SiO$_2$ gate dielectric on various gate metals is shown in Table I. The field-effect mobility can be obtained from the saturation current $I_{ds}=(W\mu C_{ox}/2L)(V_g-V_0)^2$ at saturation voltage $V=-40$ V. $C_{ox}=11.13$ nF/cm^2 is the SiO$_2$ capacitance per unit area. We first compare results for spin-coated P3HT films listed in items (I)-(V). For ITO gate the mobility is not stable and varies widely from sample to sample, presumably resulting from the speckles shown in Fig. 1(a). The mobility is generally between 10^{-6} and 10^{-5} cm^2/V s, with some rare occasion to reach 10^{-3} cm^2/V s. This is four orders of magnitude lower than the P3HT mobility on Si substrate. For Al gate the 9.5 nm roughness is, in fact, larger than the roughness of 3.3 nm for ITO gate but there is now no speckle. The mobility is enhanced to 6.3×10^{-4} cm^2/V s and is more stable. Apparently the hillocks of SiO$_2$ over Al hinder the self-assembly of P3HT and prevent the mobility to reach higher level. For Cr gate without O$_2$ plasma treatment the roughness is 2.6 nm and the mobility is slightly above the Al gate value. The reproducibility is further improved. What is special about the SiO$_2$ on Cr is that its roughness can be significantly reduced by the O$_2$ plasma. As the roughness is reduced to 0.7 nm, the mobility reaches 1.1×10^{-2} cm^2/V s, only one order of magnitude lower than the Si substrate value.

The very flat SiO$_2$ surface on Cr after plasma treatment opens the possibility to an even better self-assembly of P3HT. It was shown that dip-coating process allows the polymer chain more time to assemble than spin-coating process because the solvent dries out rapidly in the latter. Figure 2 shows carrier mobilities of P3HT transistors dip coated with various concentrations of chloroform solution. For a constant extraction speed at 32 μm/s, there is an optimum concentration of P3HT solutions at 0.08 mg/ml. This is attributed to the increased solubility at low concentration. On the other hand, when the concentration is even lower, P3HT coverage of the channel may become incomplete and the mobility drops rapidly. The transistor characteristics under optimal dip-coating extraction speed of 32 μm/s with 0.08 mg/ml
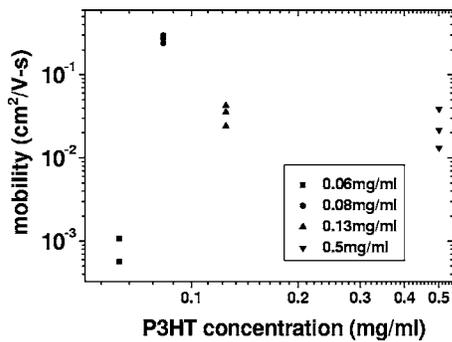
FIG. 2. Mobility of dip-coated P3HT transistor vs the concentration of P3HT in chloroform solution.

FIG. 4. (Color online) AFM image of a dip-coated P3HT film with high mobility (0.3 cm^2/V s) (a) and spin-coated P3HT film with low mobility (10^{-4} cm^2/V s) (b).

chloroform solution are shown in Fig. 3, with a mobility as high as 0.3 cm^2/V s. This value is about the same as the highest value reported for polymer transistor on Si substrate so far. AFM images of the surfaces of dip-coated P3HT films with O_2 plasma treated oxide are shown in Fig. 4(a), and spin-coated P3HT films without O_2 plasma treated oxide are shown in Fig. 4(b). For dip-coated P3HT surface, "rodlike" morphology can be observed [see Fig. 4(a)]. The rodlike structure has been analyzed by x-ray diffraction as well as UV absorption, and is shown to possess a high degree of crystallinity formed by self-assembly of P3HT.[5,14,15] Since self-assembly is very surface sensitive so far it is achieved only for silicon substrate. Our AFM images demonstrate such that polycrystalline structure is possible even for transistor on rough glass substrate once the gate metal is properly selected. Films with large crystalline grains in general yield higher a field-effect mobility. In contrast, no rodlike structure is observed for spin-coated film with lower mobility. The transistor performances of dip-coated P3HT with two different SiO_2 roughness are listed in (VI) and (VII) of Table I.

Despite the high mobility in dip-coated devices, their on/off ratio is inferior to the spin-coated devices, as shown in Table I. As a positive V_g is applied the off-current approaches

the gate leakage current I_g, indicating that the reduced on/off ratio is caused by the increased APCVD SiO_2 conductivity after dip coating. This seems to be caused by the permeation of P3HT from the chloroform solutions to the pores of SiO_2 when the sample is immersed in the solutions for a long period during dip coating. Further surface treatment for the APCVD oxide by, for example, organic monolayer is needed to reduce the permeability and maintain insulation even after dip coating.

In summary, using Cr instead of ITO or Al as the gate metal on glass substrate, we obtain very flat SiO_2 gate dielectric surface free from chemical instability and hillocks. The polymer transistor mobility reaches as high as 0.3 cm^2/V s. This implies that high-performance polymer electronics can be fabricated on low-cost transparent substrates such as glass and plastics.

FIG. 3. (Color online) Characteristics of P3HT FET deposited by dip-coating methods with 0.08 mg/ml solution concentration, Cr gate, and APCVD oxide treated by O_2 plasma for 15 min. I_g is the gate leakage current.

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