CMOS Active Bandpass Filter Using Compacted Synthetic Quasi-TEM Lines at C-Band

Ching-Kuang C. Tzuang, *Fellow, IEEE*, Hsien-Hung Wu, *Student Member, IEEE*, Hsien-Shun Wu, *Member, IEEE*, and Johnsea Chen

***Abstract*—This paper presents a fully monolithic transmission-line-based active bandpass filter (BPF) fabricated in a 0.18-μm standard complementary metal–oxide–semiconductor (CMOS) technology. The half-wavelength resonators are realized by synthetic quasi-TEM complementary conducting-strip transmission lines (CCS TLs). To lower the insertion loss of the BPF, the differential nMOS cross-coupled pairs are combined with the parallel resonators. Besides, the active devices and CCS TLs are vertically integrated on the standard CMOS substrate. The Q-enhanced resonator, which is comprised of a CCS TL and an nMOS cross-coupled pair, is theoretically investigated. Simulation results indicate that the Q factor of the resonator can be increased from 3.4 to 84.0 at 6.53 GHz. Additionally, the prototype of the second-order BPF occupies an area of 1230 μm$\times$ 880 μm, and the measured results demonstrate that the center frequency is 6.02 GHz with a bandwidth of 1.14 GHz. The $P_{1\mathrm{dB}}$ and insertion loss are -15.2 dBm and 2.2 dB, respectively, when the BPF consumes 3.0 mA from a 1.8-V supply. A two-port noisy network is also reported to examine the noise figure (NF) of the proposed BPF. Theoretical results reveal that the NF is 11.38 dB at 6.0 GHz, with a difference of less than 7.2% among the measured data.**

***Index Terms*—Active bandpass filter (BPF), C-band, CMOS, transmission line (TL).**

I. Introduction

ON-CHIP radio or RF systems-on-chip (RF SOCs) incorporating monolithic complementary metal–oxide–semiconductor (CMOS) bandpass filters (BPFs) have become increasingly attractive in the world of a congested frequency spectrum for personal communications service (PCS) band [1], wideband code-division multiple-access (WCDMA) receivers [2], and time-division-duplex (TDD) systems [3]. Elimination of off-chip filters often means adding RF performance, improving selectivity requirements, reducing noise pick-up, and lowering overall RF power consumption [2], [3]. On-chip CMOS passive resonators formed of transmission lines (TLs) typically have quality factors (Q factors) proportional to the square root of the operating frequency. A carefully designed CMOS BPF at millimeter-wave frequency generally provides an adequate Q factor. Therefore, a passive BPF at 30 and 40 GHz have been found to perform reasonably well [4], [5]. However, most wireless applications operate below C-band (4–8 GHz) where the CMOS on-chip spiral inductor necessary for carrying out the resonator design has a fairly low Q factor, of typically 5 or below [6, Table I]. This paper presents the recent advance in the state-of-the-art CMOS active BPF design achieving a small size, low passband loss, high outband rejection, low power consumption, low noise figure (NF), and high input 1-dB compression point. The literature survey indicates that most active CMOS BPFs below the C-band incorporate inductors for resonator designs, e.g., actively Q-enhanced coupled inductors [2], [7], emulated coupled inductors [6], energy-recovered spiral inductors [8], and Q-enhanced LC bandpass biquads [9].

This paper presents a novel approach based on a microwave filter design procedure incorporating low-Q half-wavelength resonators loaded by active circuits to compensate losses [10]. In contrast to the recently reported C-band passive lumped-element filter [11], which was fabricated in a highly resistive silicon substrate with a resistivity 100 times that of a typical CMOS foundry wafer, the proposed design methodology adopts synthetic quasi-TEM TLs on a standard CMOS substrate, rendering a high-performance miniaturized active BPF design. The previously published research briefly reported the measurement results of the proposed active BPF [10]. However, this paper explores in detail the design of the active TL resonator based on a complementary conducting-strip transmission line (CCS TL) followed by the differential- and common-mode analyses on the active resonator in Section II. Section III then presents a practical example with the design parameters and experimental characterizations. Section IV then investigates the NF of the presented active BPF with a two-port noisy network. Conclusions are finally drawn in Section V.

II. CMOS TL-Based Resonators

A. CMOS CCS TL

Recently the synthetic quasi-TEM TL so-called CCS TL had experimentally demonstrated its application in [10], [12], [13]. The CCS TL is made of a unit cell, which has dimensions much smaller than the operating wavelength, typically one-thousandth. The unit cell consists of a mesh ground and a four-arm signal trace. The guiding characteristics of the CCS TL had been investigated intensively, showing the following features [12]–[14]. First, the characteristic impedance and propagation constant of the CCS TL can be controlled by the varying geometric parameters such as the width of the signal

Manuscript received April 8, 2006; revised May 30, 2006.

C.-K. C. Tzuang and H.-S. Wu are with the Graduate Institute of Communication Engineering, Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan 106, R.O.C. (e-mail: cktzuang@cc.ee.ntu.edu.tw).

H.-H. Wu is with the Department of Communication Engineering, National Chiao Tung University, Hsinchu, Taiwan 300, R.O.C. (e-mail: hhwu_msn@yahoo.com.tw).

J. Chen is with the Cadence Methodology Service Company, Taipei, Taiwan 116, R.O.C.

Digital Object Identifier 10.1109/TMTT.2006.881507

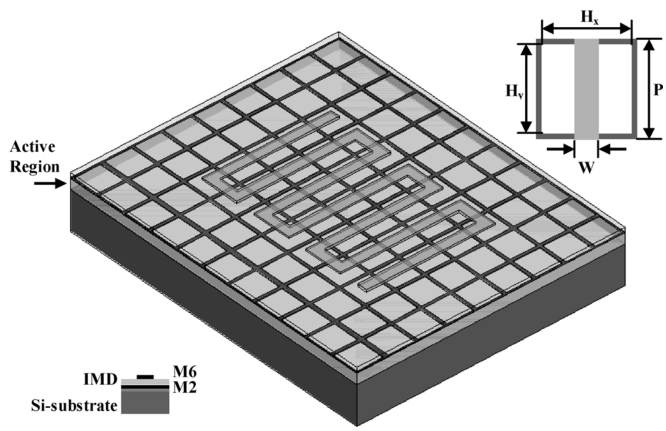

Fig. 1. Monolithic CCS TL of 7 × 5 unit cells integrating above the active devices.

trace and the mesh area of the mesh ground plane. Second, the real estate of the CCS TL-based passive circuit is proportional to the period of unit cell, which is scalable with advance in photolithography. Third, the mesh ground plane can provide good electromagnetic (EM) shields to avoid cross coupling of circuits integrated by the CCS TL. Fig. 1 reports for the first time that the CCS TL is right on top of transistor region. The inset of Fig. 1 shows the cross-sectional view of the CCS TL adopted in this paper, in which top metal forms a meandered signal path. M2 is applied to realize the mesh ground plane, which is sandwiched between the CCS TL and the first metal layer (M1) for interconnections between active devices. Such connections also include the biasing paths for the terminals (source, drain, and gate) in a MOS transistor backbone buses for paralleling the MOS transistors.

The guiding characteristics of the CCS TL on the silicon substrate shown in Fig. 1 were investigated by performing full-wave EM simulations using Ansoft's finite-element-based High-Frequency Structure Simulator (HFSS). The following material and structural parameters, which were defined in the EM simulations, were specified based on a typical 0.18-μm CMOS 1P6M process. The thicknesses of M6 and M2 metal layers are 2.0 and 0.55 μm, respectively. The relative dielectric constant and the thickness of inter-media-dielectric (IMD) sandwiched between M6 and M2 are 4.0 and 5.88 μm, respectively. The thickness and conductivity of the silicon substrate are 482.6 μm and 11 S/m, respectively. The linewidth (W) of the CCS TL is 30.0 μm, the period (P) of the unit cell is 44 μm and the mesh area ($H_x \times H_y$) is 40 μm $\times$ 40 μm.

The TL parameters, including complex characteristic impedances and propagation constants, were extracted from the two-port scattering analyses [12]. Fig. 2 shows the extracted results of the typical CCS TL design example of Fig. 1 based on the above-mentioned parameters.

From 1.0 to 8.0 GHz, the real part of the characteristics impedance (Z_c), which is the solid line plotted in Fig. 2(a), nearly keeps at a constant value of 34.2 Ω. The imaginary part of Z_c is capacitive, ranging from -11.7 to -2.04 Ω. The normalized phase constant shown in solid line in Fig. 2(b) illustrates the value of 1.86 at the desired operating frequency.

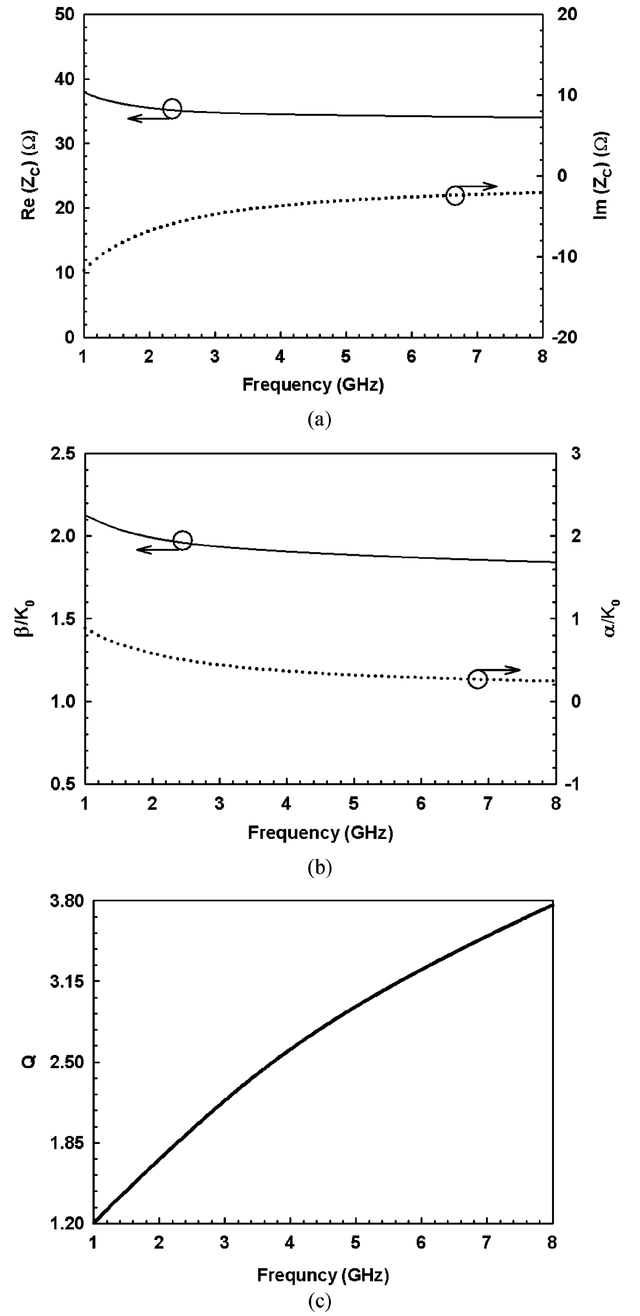

Fig. 2. Guiding characteristics of the meandered compacted CMOS-based CCS TL of Fig. 1. (a) Complex characteristic impedance. (b) Normalized complex propagation constant. (c) Q factor.

Therefore, we can estimate the physical length of a half-wave-length CCS TL at 6.0 GHz to be 13 210-μm long and such TL can be compacted in the area of 792 μm $\times$ 792 μm by using the meandered CCS unit cells with a period of 44.0 μm.

The normalized attenuation constant, which is plotted by the dotted symbol in Fig. 2(b), however, shows a relatively high loss aspect of the TL. In the low frequency limit (1 GHz), the metal thickness employed in the CCS TL is smaller than the skin depth, thus we observe larger attenuation losses. Fig. 2(c) plots the Q factor of the CCS TL against frequency, showing 2.19, 2.94, and 3.40 at 3.0, 5.0, and 6.53 GHz, respectively. The Q factors employed in our design of an active resonator

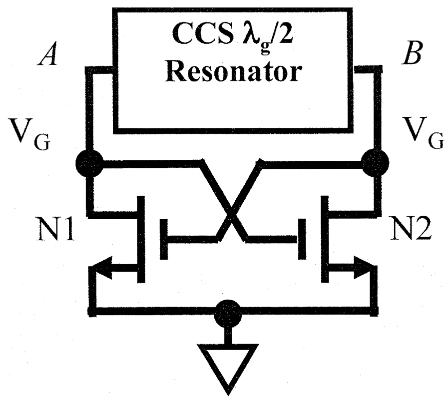

Fig. 3. Q-enhanced CCS half-wavelength resonator incorporating an nMOS cross-coupled pair.

are comparable, but smaller than those of inductor-based design [1]–[3], [6]–[9].

Since the Q factor of the CCS TL suffers from the process limitation, the losses of CCS-TL-based resonators need to be compensated. In Section II-B, a MOS-based active network is reported for elevating the Q factor of the CCS half-wavelength resonator.

B. Q-Enhanced Monolithic Half-Wavelength Resonator

Fig. 3 shows the concept of a Q-enhanced complementary conducting-strip (CCS) half-wavelength resonator. A cross-coupled pair, which consists of two identical nMOS transistors, is integrated into a half-wavelength resonator. The drain terminal of N1 is directly connected to the gate terminal of N2 and vise versa. Two transistors are biased at the same dc potential (V_G), and the drain terminals of both N1 and N2 are directly loaded with a CCS half-wavelength resonator forming a new composite resonator.

Since the active resonator will be excited single endedly, not differentially, both common- and differential-mode signals will exit in the active resonator structure. Fig. 4(a) and (b) illustrates the equivalent circuits for differential- and common-mode excitations, respectively.

When a differential-mode signal transmits into a cross-coupled nMOS transistors pair and establishes a positive feedback, a virtual ground is formed at the symmetric plane rendering a negative differential resistance $-R_d$ in Fig. 4(a) with magnitude approximately equal to the inverse of transconductance of the cross-coupled pair [15]. On the other hand, the capacitance across the resonator is approximately half of the combined capacitance ($C_{\rm gs} + C_{\rm gd}$).

Since the potentials on the drain and gate terminals of the nMOS are equal under a common-mode excitation, the nMOS acts as a gate–drain-connected diode. Therefore, two parallel *RC* networks are loaded with both sides of the half-wavelength resonator. The shunt resistance R_c shown in Fig. 4(b) represents the small-signal resistive loss of the transistor operated in the saturation region. To make proper operation of the active BPF, the differential mode must prevail over the common mode in the passband. Since the cross-coupled pair can amplify the differential-mode signal and attenuate the common-mode signal, such a circuit characteristic can increase the common-mode rejection

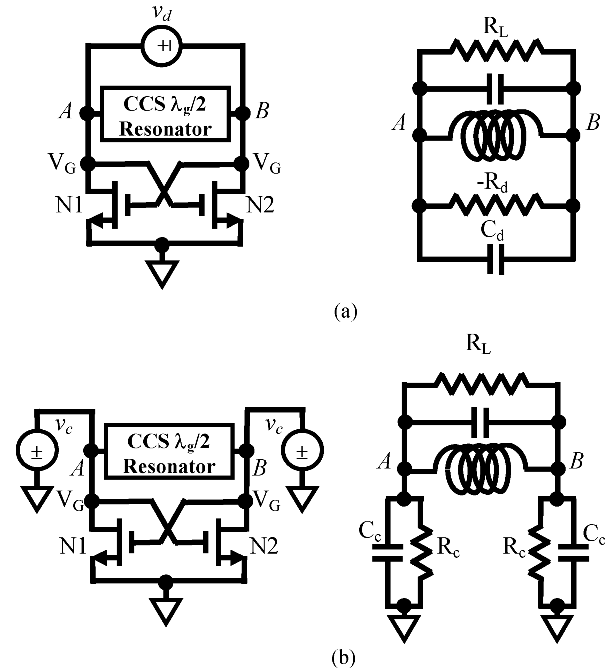

Fig. 4. Small-signal analyses of the Q-enhanced half-wavelength resonator. (a) Differential-mode analysis. (b) Common-mode analysis.

of the proposed Q-enhanced resonator, and relax the issue on symmetrical layout of the resonator during the filter integration.

The complex input impedance under differential-mode excitation was theoretically investigated by using Agilent's ADS2004A software. Through the analysis, the length and width of the two transistors were set at 0.18 and 80 μm, respectively. V_G was isolated from the differential RF signal by an RF choke. The results illustrate that the value of C_d and $-R_d$ were nearly constant from 1.0 to 8.0 GHz, revealing a broadband characteristic of the equivalent active *RC* circuit. The total equivalent resistance ($R_{\rm equ}$) of the differentially driven active resonator can be expressed by

$$R_{\rm equ} = \frac{-R_d \cdot R_L}{R_L - R_d} \qquad (1)$$

where R_L represents the loss of the CCS half-wavelength resonator. Since the value of the frequency-dependent R_L increases with increasing frequency, the active resonator tends to become more stable at frequency higher than the resonant frequency. Furthermore, the value of $-R_d$ is inversely proportional to the drain current of the nMOS transistors [15]. Thus, as shown in Fig. 5, V_G can be applied to adjust proper negative resistance for realizing a stable half-wavelength resonator.

The inset in Fig. 6 depicts the schematic for extracting the unloaded Q factor of the active half-wavelength resonator shown in Fig. 3. Two tiny capacitors of 0.01 fF formed the EM coupling between the resonator and loads. Clearly the excitation was single ended. The size of the nMOS transistor was the same as that reported in Fig. 5, and the half-wavelength resonator was realized by using the meandered CCS TL reported in Section II-A. The value of R_L of the CCS half-wavelength resonator and $-R_d$ of the cross-coupled pair

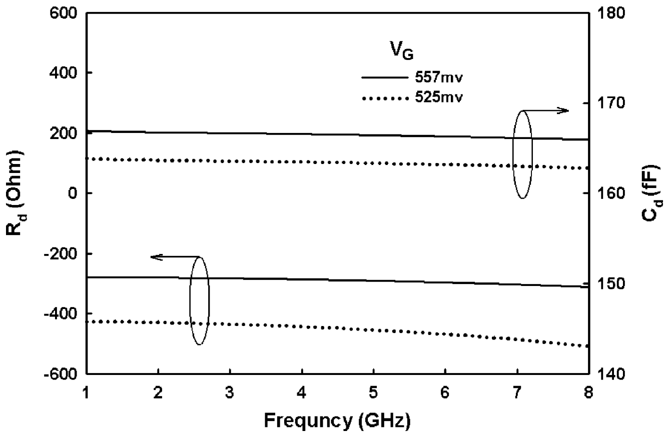

Fig. 5. Differential input impedance of a 0.18-μm nMOS cross-coupled pair with length of 0.18 μm and width of 80.0 μm.

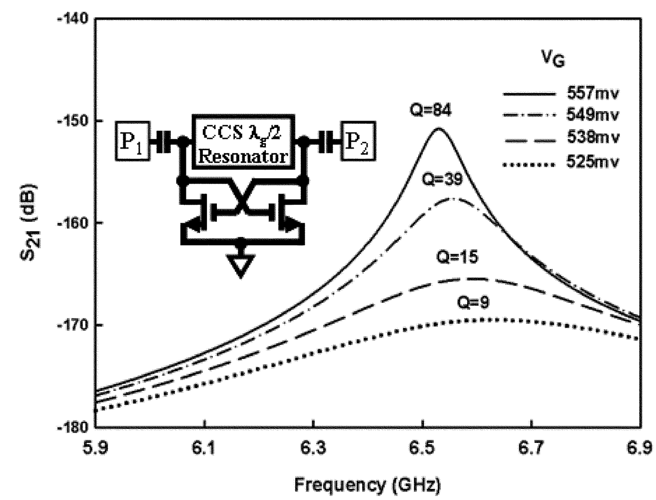

Fig. 6. Unloaded Q factor of Q-enhanced half-wavelength resonator incorporating a 0.18-μm nMOS cross-coupled pair.

biased at 557 mV are 298.4 and -301.34 Ω at 6.53 GHz, respectively. Therefore, according to (1), Fig. 6 illustrates a stable active half-wavelength resonator.

The extracted Q factors shown in Fig. 6 follow the definition of the unloaded Q factor in [16]. Moreover, the magnitudes of the transducer gain of the weakly coupled active resonator are also illustrated in Fig. 6. The Q factor was only 3.40 for the passive CCS half-wavelength resonator. With the active Q-enhanced circuit biased at 525, 538, 549, and 557 mV, the enhanced Q factors were 9, 15, 39, and 84, respectively. Notably, the resonant frequency of the Q-enhanced resonator was slightly shifted from 6.633 to 6.531 GHz when V_G was increased. Such frequency drift was caused by the increase of C_d shown in Fig. 5.

III. CMOS TL-Based Active BPF

Fig. 7 shows the complete schematic of a second-order BPF incorporating the Q-enhanced half-wavelength resonators [10]. The J-inverters were realized by series capacitors C_1, C_2, and C_3. The design procedure of the BPF is well documented in [16]. In this practical example, f_c of the BPF was located at 6.02 GHz, and bandwidth (BW) was 1.0 GHz with a ripple of

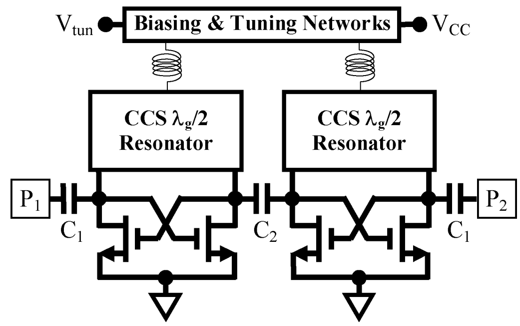

Fig. 7. Second-order CMOS TL-based BPF.

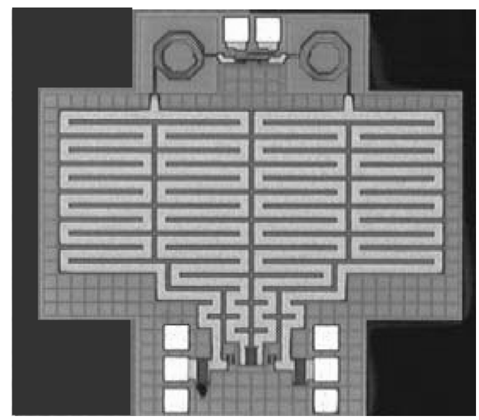

Fig. 8. Chip photograph of the prototype BPF in Fig. 7.

0.2 dB. The order of the BPF was two and the reference impedances of two terminals (P_1 and P_2) were 50 Ω. The biasing and tuning networks controlled by $V_{\rm tun}$ provided biasing currents for the nMOS cross-coupled pairs. These networks were isolated from the CCS TL resonators by the on-chip spiral inductors, as shown at the top of Fig. 8. Fig. 8 also illustrates the chip photograph of the prototype filter in Fig. 7.

The entire active BPF, including the CCS TLs, capacitors, inductors, active networks, and pads were fully integrated in a chip area of 1230 μm $\times$ 880 μm. The capacitor was realized with the so-called interdigital metal–oxide–metal (MoM) capacitors of top-three metal layers. In the realizations, C_1 was 380 fF with an area of 45.9 μm $\times$ 79.8 μm, and C_2 was 220 fF with an area of 41.9 μm $\times$ 52.8 μm, respectively. Additionally, the inductance of the on-chip spiral inductors was approximately 3.0 nH and occupied an area of 251 μm $\times$ 247 μm.

The small-signal experiments were performed after the on-wafer short-open-load-thru (SOLT) procedures had been conducted by the vector network analyzer (VNA) Agilent E5091A. In the measurements, the prototype shown in Fig. 7 was biased by a supplying voltage (V_{CC}) of 1.8 V with a current consumption of 3.0 mA. The value of $V_{\rm tun}$ and the power level of input signals were set at 1.0 V and -20 dBm, respectively. Additionally, the measured result was compared with simulations performed by Agilent's ADS2004A. Before the simulation, all the passive components including capacitors, inductors, and CCS TL were characterized by Ansoft's HFSS. The BSIM3 V3.2.4–based RF models used for active devices were provided by the foundry. Fig. 9(a) shows the comparisons

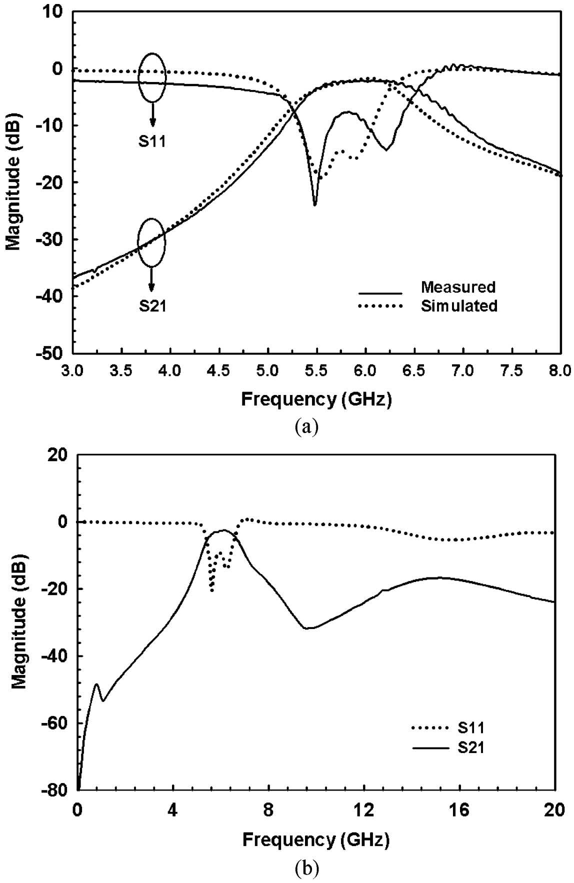

Fig. 9. Transmission and reflection characteristics of the active BPF in Fig. 8. (a) Comparison of measured and simulated data over 5-GHz narrow BW. (b) Measured responses across 20-GHz broad BW for investigating spurious responses.

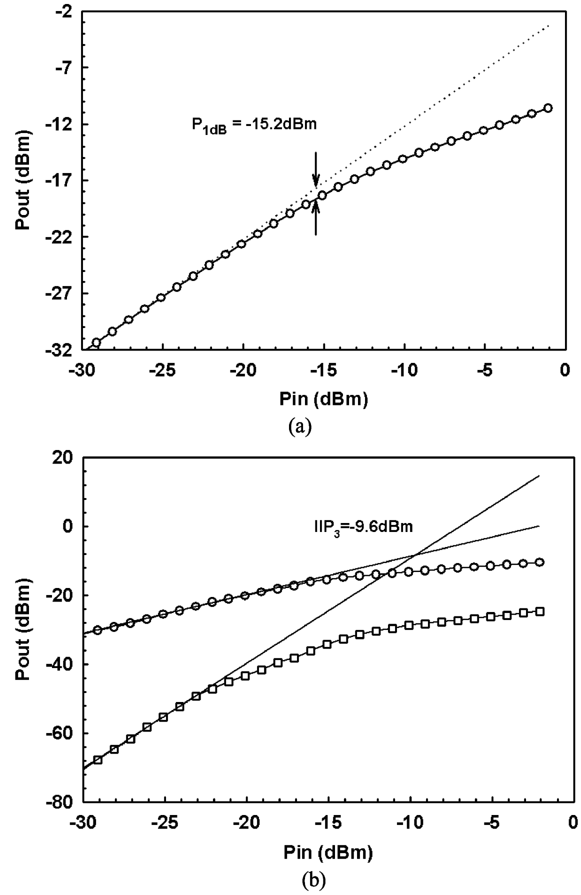

Fig. 10. Nonlinear characteristics of the active BPF in Fig. 8. (a) Input 1-dB compression point ($P_{1\mathrm{dB}}$). (b) Input third-order intermodulation intercept point (IIP_3).

from 3.0 to 8.0 GHz, revealing good agreement between the simulated and measured data, except for the return loss at passband. The slight mismatch shows that the capacitive coupling between the two Q-enhanced half-wavelength resonators were well controlled through the J-inverter C_2, and parasitic coupling through the lossy substrate was not serious owing to the good EM shield from the meshed ground plane of the CCS TL. In other words, the CCS TL can effectively confine the EM propagations and eliminate the unwanted coupling of the adjacent signal lines in the compact layout.

The measured results of two-port scattering parameters based on the 50-Ω system lead the following observations. The center frequency of the second-order BPF is 6.02 GHz, and the insertion loss is approximately 2.2 dB from 5.38 to 6.65 GHz. The BW is approximately 1.14 GHz (5.26–6.40 GHz) with a return loss of 7.64 dB. Two reflection zeros are identified at 5.47 and 6.20 GHz. Additionally, the prototype can reject the low-side signal approximately 28.18 dB at 4.0 GHz and the high-side signal approximately 18.33 dB at 8.0 GHz. The spurious response of the prototype, which is observed in Fig. 9(b), is suppressed approximately 16.67 dB at 15.25 GHz.

The nonlinear characteristics of the prototype had also been investigated by measuring the input third-order intermodulation intercept point (IIP_3) and the 1-dB compression point ($P_{1\mathrm{dB}}$). For the measurement of $P_{1\mathrm{dB}}$, the signal generator Agilent E8267D provided an input continuous wave (CW) at 6.02 GHz, and the spectrum analyzer Agilent E4440A was applied to observe the output signals of the prototype. For the measurement of IIP_3, two signal generators were applied to generate two fundamental frequencies centered at 5.8 GHz with a separation of 10 MHz. The testing system, which includes the connectors and cables, were calibrated before the experiments. Additionally, the biasing conditions of the prototype were kept the same as those in the S-parameter experiments. The measured results, as shown in Fig. 10, indicate the input power levels for $P_{1\mathrm{dB}}$ and IIP_3 are -15.2 dBm and -9.6 dBm, respectively.

IV. Noise Analyses of TL-Based Active BPF

Experimental results in Fig. 9(a) indicate that the prototype is a passive filter with an insertion loss of 2.2 dB in the passband. According to the textbook definition, the NF of a passive two-port network is equivalent to the inverse of its available power gain [17]. However, the proposed BPF, as depicted in Fig. 7, is comprised of a CCS TL and differential nMOS cross-coupled pairs. The cross-coupled pairs not only provide negative resistance to elevate the Q factor of the resonators, but also produce the noise simultaneously. Therefore, the noise contributions from the transistors need to be incorporated into the NF of the proposed BPF. Therefore, a noisy network is presented here to investigate the NF of the proposed BPF shown

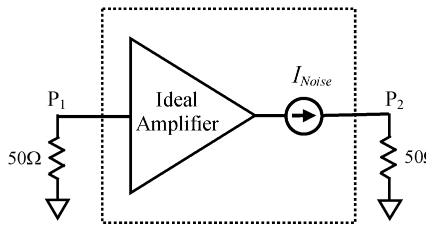

Fig. 11. Equivalent noisy two-port network of the prototype BPF in Fig. 7.

in Fig. 7. Fig. 11 illustrates the two-port network consists of an ideal amplifier and a noise current source. The gain of the ideal amplifier indicates the transmission coefficient of the BPF, and the noise current source at the output of the ideal amplifier represents the total noise current generated by the nMOS cross-coupled pairs.

The noise characteristics of an nMOS cross-coupled pair had been well documented in [18] and [19]. The differential output noise current spectral density of an nMOS cross-coupled pair is equivalent to the summation of thermal noise generated in the channels of two nMOS transistors [19]. Furthermore, the channel noise of an nMOS transistor operating in saturation can be quantified by an equivalent noise current between the drain and source terminals

$$\overline{i_n^2} = 4kT\gamma g_m \tag{2}$$

where g_m and γ are the transconductance and channel noise coefficient of an nMOS transistor, respectively [20], [21].

To demonstrate the feasibility of the proposed noisy network, the theoretical analyses were conducted with the two-port network illustrated in Fig. 11 and the transistor parameters reported in Section II-B. The value of g_m derived according to the definition in [21] was 8.872 mS. The γ value extracted from the small-signal noise analysis of the nMOS transistor was 1.012 at 6.0 GHz [21]. Thus, the total noise current spectrum density of the nMOS cross-couple pairs was $6.436e - 22$ A^2/Hz at 298.15 K. The calculated NF of the proposed BPF after following the procedures described in [22] was 11.38 dB. Additionally, the calculation results from 5.5 to 6.0 GHz were compared with those of the simulations and experiments, as illustrated in Fig. 12, revealing a difference of less than 7.2% on the noise analyses. The measurements, which were undertaken using the Agilent NF analyzer N8974A, reveal that the NF of the prototype was approximately 12.36 dB at 5.5 GHz, which was slight decreased to 10.92 dB at 5.8 GHz. Simulation results indicate that the NF of the proposed bandpass filer was 12.30 and 11.40 dB at 5.5 and 6.0 GHz, respectively. These good agreements indicate that the proposed noisy network is valid for predicting the NF of the BPF shown in Fig. 7.

Furthermore, the NF of the proposed BPF with different transistor width was also theoretically analyzed by following the same above-mentioned analytical procedures. Through the analyses, the characteristics of the BPF, including the insertion loss, reflection coefficient, and BW, were identical to those reported in Fig. 9(a).

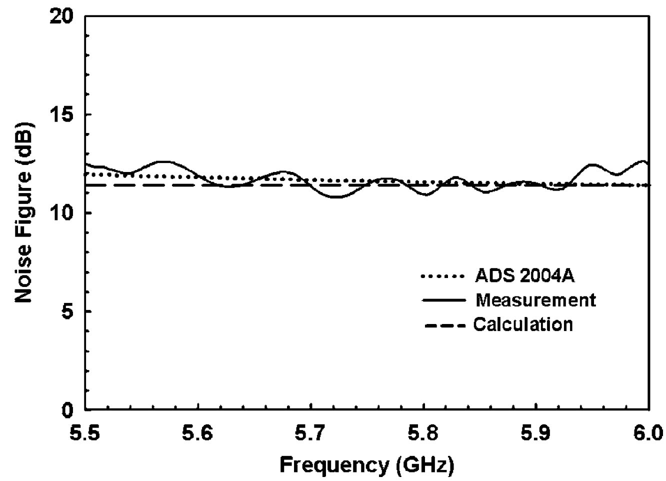

Fig. 12. NFs of the proposed BPF.

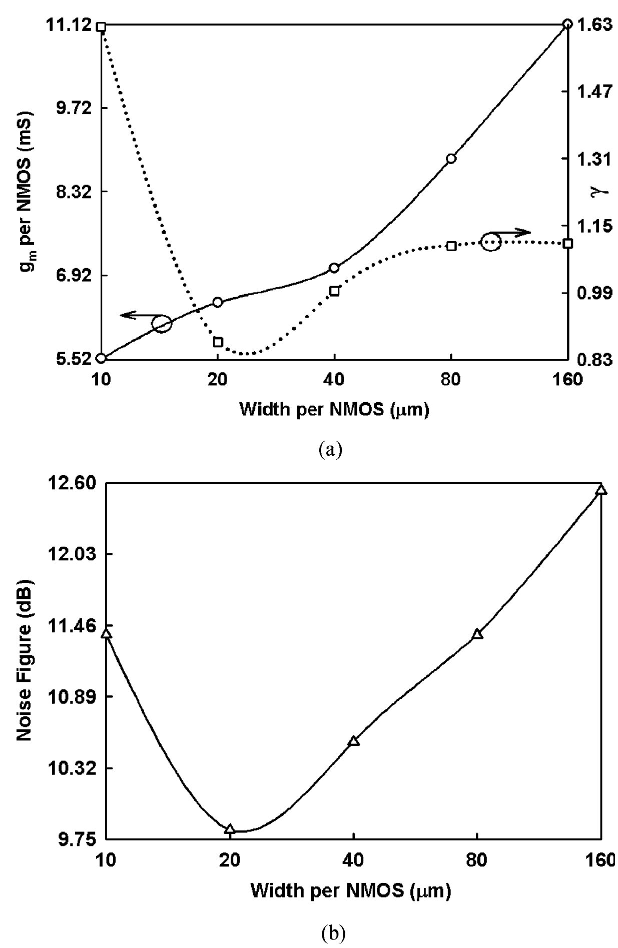

Fig. 13. Theoretical predictions of noise performances for the proposed BPFs with different transistor widths. (a) g_m and γ. (b) NFs of the BPFs.

Fig. 13(a) and (b) plots the statistical results from which the following observations can be drawn. The value of γ, denoted by the curve with square symbols in Fig. 13(a), is highest at 1.63 with the smallest transistor width of 10.0 μm. However, γ can be reduced and kept with a constant value of 1.10 when the width is larger than 80 μm. Conversely, g_m is increased from 5.52 to 11.12 mS, corresponding to the increase of transistor width from 10 to 160 μm. Since the equivalent small-signal resistor between the drain and source terminals increases due to the nonquasi-static (NQS) effect [23], the higher value of g_m is required to reduce the ohmic loss from the CCS TLs and the resistive loss in the channels of transistors. As revealed in (2), the noise current of the transistor is proportional to the product of g_m and γ. Consequently, the NF, denoted by the curve with triangular symbols in Fig. 13(b), is 11.38 dB, corresponding to the transistor width of 10 μm. Increasing the width of the transistor from 10 to 20 μm causes the NF linearly reduced to its minimum value of 9.82 dB. However, using the transistor width larger than 20 μm in the BPF increases the resultant NF. These observations demonstrate the design tradeoff for minimizing the NF of the proposed BPF.

V. Conclusion

A TL-based active BPF was realized by using standard 0.18-μm CMOS 1P6M technology. The active BPF was constructed using the Q-enhanced half-wavelength resonators, which consisted of a differential nMOS cross-coupled pair and synthetic quasi-TEM CCS TL. In the CMOS process, the top metal (M6) and bottom metal (M1) formed the meandered traces and interconnections of the CCS TL and active devices. A mesh ground plane, located at M2, was sandwiched between M6 and M1, completing a vertical integrations for the proposed active BPF. The on-chip guiding characteristics of the CCS TL were theoretically extracted as the basic parameters for designing the Q-enhanced resonator. The circuit behaviors of the Q-enhanced resonator were theoretically investigated by conducting the differential- and common-mode analyses. The Q-enhanced resonator acted as a stable parallel resonator with Q-enhancement when the nMOS cross-coupled pair provided a negative resistance with an absolute value larger than that of a parallel resonator at the resonant frequency. The theoretical results indicate that the Q factor of the resonator was elevated from 3.4 to 84 at 6.53 GHz. This resonator was applied in designing a prototype of a second-order BPF at C-band with a chip area of 1230 μm$\times$ 880 μm. The comparisons between the on-wafer measurements and simulations reveal that the proposed active TL-based BPF is feasible. Drawing 3.0 mA from a 1.8-V supply, the prototype achieved 2.2-dB insertion loss and 7.64-dB return loss when operating with a 1.14-GHz BW at 6.02 GHz. The suppressions of spurious responses were 24 and 16.67 dB at 12.0 and 15.25 GHz, respectively. The high- and low-side rejections were 18.33 and 28.18 dB at 8.0 and 4.0 GHz, respectively. The input 1-dB compression point ($P_{1\mathrm{dB}}$) and third-order intermodulation intercept point (IIP_3) were -15.2 dBm and -9.6 dBm, respectively.

Additionally, a noisy two-port network was constructed to examine the NF of the proposed BPF. In the network, the total noise of the BPF consists of its transmission loss and the noise current produced by the nMOS cross-coupled pairs. The results of the analysis were compared with those of the simulations and experiments, revealing a difference among them of less than 7.2%. Such agreements validate the feasibility of the proposed noisy network. Furthermore, the NF of the active TL-based BPFs designed with different transistor widths were theoretical analyzed using the proposed noisy network. A design curve demonstrating the tradeoff on minimizing the NF of the proposed active BPF was also reported.

References

[1] D. Li and Y. Tsividis, "Design techniques for automatically tuned integrated gigahertz-range active *LC* filters," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 967–977, Aug. 2002.

[2] T. Soorapanth and S. S. Wong, "A 0-dB IL 2140$\pm$30 MHz bandpass filter utilizing Q-enhanced spiral inductors in standard CMOS," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 579–586, May 2002.

[3] X. He and W. B. Kuhn, "A 2.5-GHz low-power, high dynamic range, self-tuned Q-enhanced *LC* filter in SOI," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1618–1628, Aug. 2005.

[4] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Design of CMOS for 60 GHz applications," in *IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, Feb. 2004, pp. 440–441.

[5] H.-T. Tso and C.-N. Kuo, "40 GHz miniature bandpass filter design in standard CMOS process," in *Silicon Monolithic Integr. Circuits RF Syst. Top. Meeting*, Atlanta, GA, Sep. 2004, pp. 239–242.

[6] A. N. Mohieldin, E. Sanchez-Sinencio, and J. Silva-Martinez, "A 2.7-V 1.8-GHz fourth-order tunable *LC* bandpass filter based on emulation of magnetically coupled resonators," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1172–1181, Jul. 2003.

[7] S. Bantas and Y. Koutsoyannopoulos, "CMOS active-*LC* bandpass filters with coupled-inductor Q-enhancement and center frequency tuning," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 51, no. 2, pp. 69–76, Feb. 2004.

[8] Y.-C. Wu and M. F. Chang, "On-chip RF spiral inductors and bandpass filters using active magnetic energy recovery," in *Proc. IEEE Custom Integr. Circuits Conf.*, Orlando, FL, May 2002, pp. 275–278.

[9] F. Dulger, E. Sanchez-Sinencio, and J. Silva-Martinez, "A 1.3-V 5-mW fully integrated tunable bandpass filter at 2.1 GHz in 0.35 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 918–928, Jun. 2003.

[10] C.-K. C. Tzuang, H.-H. Wu, H.-S. Wu, and J. Chen, "A CMOS miniaturized C-band active bandpass filter," in *IEEE MTT-S Int. Microw. Symp. Dig.*, San Francisco, CA, Jun. 2006, pp. 772–775.

[11] K. Entesari, T. Vaha-Heikkila, and G. M. Rebeiz, "Miniaturized differential filters for C- and Ku-band applications," in *Proc. Eur. Microw. Conf.*, Munich, Germany, 2003, pp. 227–230.

[12] C.-C. Chen and C.-K. C. Tzuang, "Synthetic quasi-TEM meandered transmission lines for compacted microwave integrated circuits," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 6, pp. 1637–1647, Jun. 2004.

[13] H.-S. Wu, H.-J. Yang, C.-J. Peng, and C.-K. Tzuang, "Miniaturized microwave passive filter incorporating multilayer synthetic quasi-TEM transmission line," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 9, pp. 2317–2720, Sep. 2005.

[14] H.-H. Wu, H.-S. Wu, and C.-K. C. Tzuang, "Synthesized high-impedance CMOS thin-film transmission line," in *Silicon Monolithic Integr. Circuits RF Syst. Top. Meeting*, Atlanta, GA, 2004, pp. 302–304.

[15] R. Behzad, *RF Microelectronics*. Upper Saddle River, NJ: Prentice-Hall, 1998, p. 228.

[16] G. L. Matthaei, L. Young, and E. M. T. Jones, *Microwave Filters, Impedance Matching Networks, and Coupling Structures*. Norwood, MA: Artech House, 1980, ch. 8.

[17] G. D. Vendelin, A. M. Pavio, and U. L. Rohde, *Microwave Circuit Design using Linear and Nonlinear Techniques*. New York: Wiley, 1990, p. 103.

[18] P. A. Layman and S. G. Chamberlain, "A compact thermal noise model for the investigation of soft error rates in MOS VLSI digital circuits," *IEEE J. Solid-State Circuits*, vol. 24, no. 2, pp. 79–89, Feb. 1989.

[19] E. Hegazi, H. Sjoland, and A. A. Abidi, "A filtering technique to lower *LC* oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, no. 2, pp. 1921–1929, Feb. 2001.

[20] D. K. Shaeffer and T. H. Lee, *The Design and Implementation of Low-Power CMOS Radio Receivers*. Norwell, MA: Kluwer, 1999, pp. 52–53.

[21] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2001, pp. 212–213.

[22] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*, 2nd ed. Upper Saddle River, NJ: Prentice-Hall, 1997, ch. 4.

[23] Y. Cheng and C. Hu, *MOSFET Modeling & Bsim3 User's Guide*. Norwell, MA: Kluwer, 1999, ch. 10.

Ching-Kuang C. Tzuang (S'80–M'80–SM'92–F'99) received the B.S. degree in electronic engineering from National Chiao Tung University, Hsinchu, Taiwan, R.O.C., in 1977, the M.S. degree from the University of California at Los Angeles (UCLA), in 1980, and the Ph.D. degree in electrical engineering from The University of Texas at Austin, in 1986.

From 1981 to 1984, he was with TRW, Redondo Beach, CA, where he was involved with analog and digital MMICs. Since 1986, he has been with the Institute of Communication Engineering, National Chiao Tung University. In February 2004, he joined the Graduate Institute of Communication Engineering, Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, R.O.C., where he conducts research on advanced guiding structures for research and development of RF SOC, integrating active and passive microwave/millimeter-wave RF signal-processing components into a single chip. His research activities also involve the design and development of millimeter-wave and microwave active and passive circuits and the field theory analysis and design of various complex waveguide structures and large-array antennas. He has supervised 61 M.S. students and 21 Ph.D. students.

Dr. Tzuang helped in the formation of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) Taipei Chapter, and served as secretary, vice chairman, and chairman in 1988, 1989, and 1990, respectively. He recently served as the chairman of the Millimeter-Wave Industry Alliance, Taiwan Electrical and Electronic Manufacturers' Association (TEEMA), an assisted interest group in promoting standardization and application of millimeter-wave technology.

Hsien-Hung Wu (S'04) received the B.S. and M.S. degrees in electronic engineering from National Chiao Tung University, Hsinchu, Taiwan, R.O.C., in 1997 and 1999, and is currently working toward the Ph.D. degree in communication engineering at National Chiao Tung University.

His research interests include RF integrated circuits and computer-aided design (CAD) methodologies.

Hsien-Shun Wu (S'97–M'05) received the B.S. degree in electronic engineering from National Taipei University of Technology, Taipei, Taiwan, R.O.C. in 1999, and the M.S. and Ph.D. degrees in communication engineering from National Chiao Tung University, Hsinchu, Taiwan, R.O.C. in 2001, and 2005, respectively.

He is currently a Post-Doctoral Research Fellow with the Graduate Institute of Communication Engineering, National Taiwan University. His research interests include the design of wireless system modules and the development of synthetic waveguides for RF circuits.

Johnsea Chen received the B.S. degree in materials science and engineering from National Tsing Hua University, Hsinchu, Taiwan, R.O.C., in 1977, and the M.S. and Ph.D. degrees in materials science from the University of Southern California, Los Angeles, in 1982 and 1985, respectively.

From 1985 to 1991, he was with Rockwell International, Science Center, Thousand Oaks, CA, where he was involved with II–VI compound semiconductors. In 1991, he cofounded the 4′′ GaAs Research and Manufacturing Corporation, Hsinchu, Taiwan, R.O.C. It was the first III–V compound semiconductor IC design and fabrication facility in Taiwan, R.O.C. In 1996, he joined Etron Technologies Inc., a silicon-based integrated circuit (IC) design company, as the Senior Executive involved with development and business-oriented operations. Early in 2002, he joined the Cadence Methodology Service Company (CMSC), Taipei, Taiwan, R.O.C., a wholly owned subsidiary of Cadence Design Systems, which is the world leading electronic design automation (EDA) developer and supplier. He helped to develop RF related materials and devices in Taiwan, R.O.C., over the past 15 years. His recent research interests focus on the development of RF SOC chips using advance CMOS-based silicon processes.