Process and Characteristics of Fully Silicided Source/Drain (FSD) Thin-Film Transistors

Chia-Pin Lin, Yi-Hsuan Hsiao, and Bing-Yue Tsui, *Senior Member, IEEE*

***Abstract*—In this paper, high-performance fully silicided source/drain (FSD) thin-film transistors (TFTs) with FSD and ultrashort source/drain extension (SDE) fabricated by the implant-to-silicide (ITS) technique are studied thoroughly. Using the ITS technique, not only the implantation damage but also the silicide spiking is avoided so that the thermal budget can be decreased obviously. The offstate current ($I_{\rm off}$) of the FSD TFTs is equal to (n-channel) or smaller than (p-channel) that of the conventional TFTs. At onstate, due to the FSD and the SDE structure, the parasitic resistance of the S/D region and the carrier-injection resistance between silicide and channel are reduced. Therefore, superior onstate/offstate current ratio can be obtained. The influences of annealing temperature and time are also examined in this paper. A 600 °C/30-s rapid thermal annealing is sufficient to diffuse and activate dopants and, then, fabricate high-performance FSD TFTs. Excellent short-channel behavior of the FSD TFT is also confirmed. To conclude, the high-performance FSD TFT with low parasitic resistance fabricated by low-thermal-budget process is very promising for active-matrix liquid-crystal display, active-matrix organic light-emitting-diode display, and system-on-panel applications.**

***Index Terms*—Implant-to-silicide (ITS), silicide, thin-film transistor (TFT).**

I. Introduction

POLYCRYSTALLINE-SILICON thin-film transistors (poly-Si TFTs) are attractive for many applications including the active-matrix liquid-crystal display (AMLCD) and active-matrix organic light-emitting-diode display (AMOLED) [1], [2]. In order to integrate peripheral driving circuits on the same glass substrate, a low-temperature process ($\sim$600 °C) without compromising device performance should be developed. Therefore, a long position-implantation annealing, which is used to activate dopants and remove implantation damages, is carried out using a furnace system at around 600 °C for 12–24 h after the source/drain (S/D) implantation. The prolonged process time causes low throughput in the fabrication of conventional (CN) poly-Si TFTs. To overcome this drawback, dopant activation at higher temperature of above 700 °C in a rapid-thermal-annealing (RTA) system has been suggested to improve the activation efficiency and throughput. Nevertheless, the high-temperature process violates the low-temperature requirement. Thus, poly-Si TFTs suffer from a substantial tradeoff between performance and throughput.

On the other hand, the use of a thinner active layer to obtain a higher driving current, lower offstate leakage current, and superior short-channel characteristics has been reported [3], [4]. Nevertheless, the high parasitic resistance due to thin S/D regions degrades device performance such as driving capability and effective field-effect mobility ($\mu_{\rm FE}$). Especially for the AMOLED, the high S/D parasitic resistance not only reduces the brightness but also enlarge the fluctuations of brightness [5]. To reduce this parasitic resistance, various methods such as raised-S/D, SiGe-raised-S/D, and tungsten-clad-S/D techniques were proposed [6]–[8]. Ni-salicide TFTs structure with process similar to the salicide-CMOS was also proposed to reduce the S/D parasitic resistance [9]. However, in order to suppress the leakage current induced by S/D silicide spiking of salicide TFTs, not only the poly-Si at S/D cannot be fully consumed to maintain a proper S/D junction but also an excess mask is needed to block the gate electrode. At the same time, the long dopant-activation time is still an issue in the process of salicide TFTs.

To reduce the S/D series resistance of CN TFTs, while more efficiently improving the throughput, we proposed a novel fully silicided S/D TFTs (FSD TFTs) with FSD and ultrashort S/D extension (SDE) at the interface of silicide and inverted channel by the implant-to-silicide (ITS) technique has been proposed [10], [15]. Forming a FSD by the low-temperature self-aligned salicide technique, the parasitic resistance of FSD TFTs can be decreased dramatically. Adding an extension doping in the silicon by the ITS technique at about 600 °C, on the other hand, not only drastically improves the contact resistance at the Ni-silicide/poly-Si junction but also abbreviates the SDE length and avoids the silicide-spiking effect. This concept has been approved in n- and p-channel FinFETs and the preliminary results have been reported [16], [17].

In this paper, we demonstrated that both n-channel FSD TFTs (FSD nTFTs) and p-channel FSD TFTs (FSD pTFTs) can be fabricated simultaneously. The detailed fabrication process of the FSD TFTs will be described. The characteristics of the proposed FSD TFTs are presented and discussed using CN TFTs and simple Schottky-barrier (SB) TFTs as comparisons.

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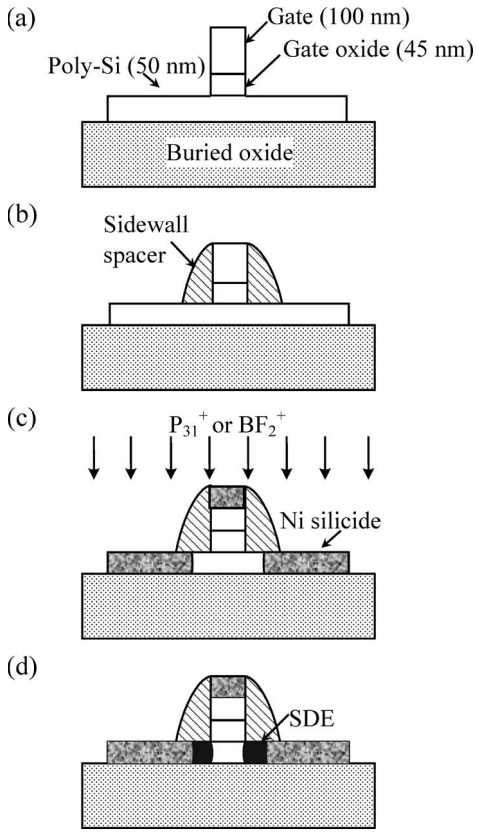

Fig. 1. Key fabrication steps of the proposed FSD TFTs.

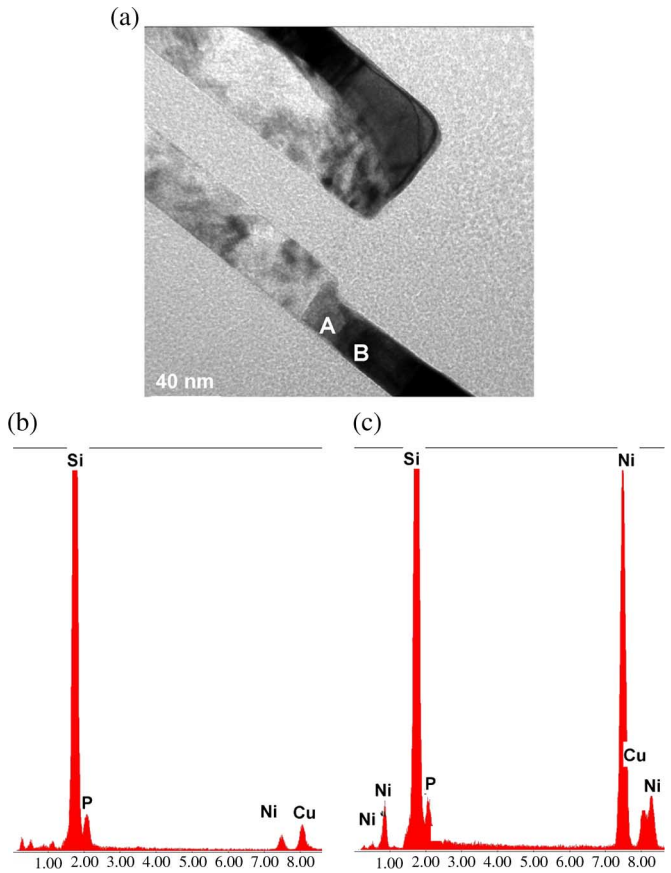

Fig. 2. (a) Cross-sectional TEM micrograph of the proposed FSD TFTs and the EDS analysis at (b) point "A," and (c) point "B."

Furthermore, the impact of activation temperature and time of the ITS process on the characteristics of FSD TFTs are also illustrated and analyzed. Excellent short-channel effect (SCE) is also demonstrated.

II. Device Fabrication

Fig. 1 shows the key fabrication steps for the proposed FSD TFTs. Briefly, the fabrication was begun by depositing an amorphous Si (α − Si) layer 50-nm thick at 550 °C in a low-pressure chemical-vapor deposition on 6-in Si wafers capped with a thermal oxide layer of 1-μm thick. The deposited α − Si layer was then crystallized by a solid-phase-recrystallization method at 600 °C in a N_2 ambient for 24 h. After patterning the active region, a 45-nm-thick CVD gate oxide and a 100-nm-thick poly-Si layer were deposited. The poly-Si layer was then patterned to form the gate electrode, as shown in Fig. 1(a). Then, a 100-nm-thick CVD oxide layer was deposited and etched to form a sidewall spacer abutting the poly-Si gate, as shown in Fig. 1(b).

Afterwards, a self-aligned silicidation process was performed to form the FSD. A thin Ni layer of 22 nm thick was deposited on the wafer. After a RTA at 500 °C for 40 s in a N_2 ambient, a wet-etching step in a H_2SO_4/H_2O_2 solution was then used to selectively remove the unreacted Ni. Ni-silicide was also formed on poly-Si gate simultaneously, as shown in Fig. 1(c). The FSD region shows a sheet resistance of about 7 $\Omega/\square$, whereas the nonsilicided S/D region shows a sheet resistance of about 800 $\Omega/\square$. Since the poly-Si gate was also partially silicided, the gate resistance was also obviously improved by a factor of 100 compared with a nonsilicided poly-Si gate.

Next, ITS process was employed to form a shallow SDE region. BF_2^+ ions were implanted to silicide at 35 KeV with 5×10^{15} cm^{-2} for FSD pTFTs and P_{31}^+ ions were implanted to silicide at 30 KeV 5×10^{15} cm^{-2} for FSD nTFTs. The high implantation dose is used to increase the dopant concentration of the SDE region and preserve the S/D junction characteristics [10], [12], [14]. Dopants were then diffused out of silicide to form an ultrashort SDE at the channel–S/D interface by a low-temperature RTA process in a N_2 ambient at temperatures of 600 °C, 650 °C, 700 °C, and 750 °C for 30, 90, and 150 s. Because of the low solid-state solubility of phosphorous and boron atoms in Ni silicide, they diffused out and piled up at the Si/silicide interface to form a ultrashort SDE as shown in Fig.1(d) [10]–[13]. Finally, typical oxide passivation layer deposition, contact hole patterning, and Al metallization completed the fabrication process.

The cross-sectional transmission electron microscopy (TEM) image of the proposed FSD TFTs activated at 600 °C for 30 s in a N_2 ambient is shown in Fig. 2(a). From the results of energy-dispersive spectrometer (EDS) analysis at the points A and B labeled in Fig. 2(a), it is observed that the silicided S/D does not grow into the channel region and a phosphorous-doped SDE region is formed. Although we could not distinguish the oxide spacer edge from the oxide passivation layer, the silicide lateral-growth length (L_s) could still be extrapolated by sheet resistance (R_s) measured by the four-terminal R_s test structure shown in Fig. 3(a). In this test structure, a 100-nm oxide

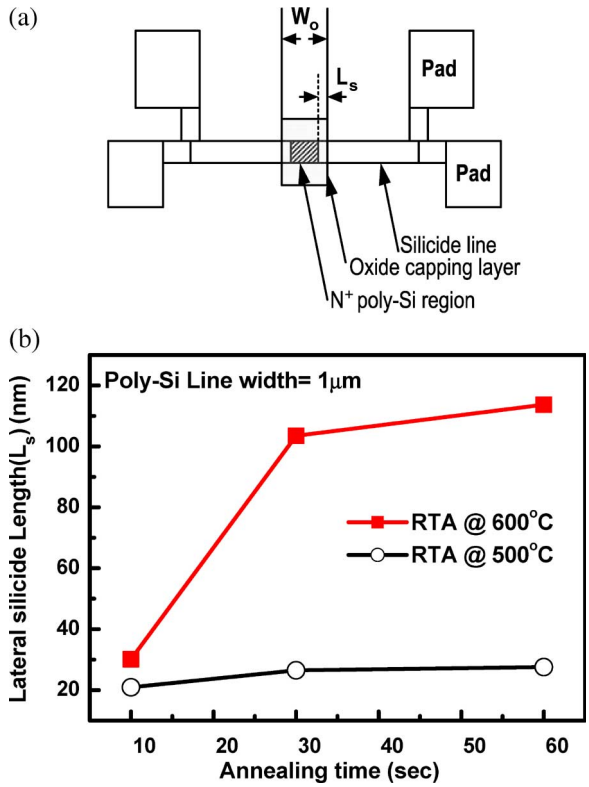

Fig. 3. (a) Schematic layout of the four-terminal sheet resistance (R_s) test structure. (b) The extracted silicide lateral-growth length (L_s) as a function of annealing time. The poly-Si linewidth is fixed at 1 μm.

cap layer was patterned to different widths (W_o) capping on the n^+-poly-Si line. Then, the exposed poly-Si regions were silicided at 500 °C and 600 °C for 10, 30, and 60 s in an RTA system. By measuring the R_s of the test structure with different W_o, the L_s could be extracted. The extracted results are shown in Fig. 3(b). It is noted that as the annealing time increases because of the limited Ni layer thickness the growth rate of L_s becomes slow. Then, after a 500-°C annealing at 30 s, the average L_s extracted from ten samples is about 26.3 nm. Moreover, Monte Carlo simulation also showed that the ions-straggle distribution of BF_2^+ and P^+ are only 8 and 9 nm at 30 and 35 KeV, respectively, which are extremely shorter than the lateral silicide length [16], [17]. Therefore, the ion-implantation process does not damage Si layer directly. Then, the junction would be almost free of implantation damage and low junction leakage current could be expected.

For comparison, CN TFTs were fabricated, as schematically shown in Fig. 4(a). The S/D was implanted after gate patterning followed by an activation annealing at 600 °C for 24 h without silicidation. Simple SB TFTs without the ITS process step were also fabricated. The schematically cross-sectional structure is shown in Fig. 4(b). In order to improve the current–voltage $(I$–$V)$ characteristics, NH_3 plasma treatment in a plasma-enhanced CVD system at 350 °C for 30 min was employed to effectively reduce trap-density and improve interface quality of channel region.

The I–V characteristics of the fabricated devices were measured using a semiconductor-parameter analyzer of model Agilent 4156C. Various device parameters, including the

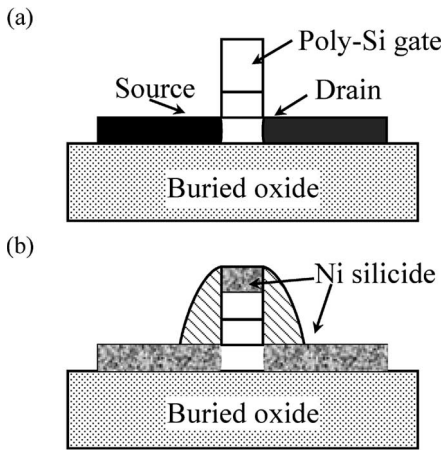

Fig. 4. Schematic cross-sectional drawings of (a) CN TFT and (b) SB TFT.

threshold voltage $(V_{\rm th})$, subthreshold swing (SS), and field-effect mobility $(\mu_{\rm FE})$ were extracted at a drain voltage of $|V_{\rm ds}| = 0.1$ V. The threshold voltage is defined as the gate voltage at which yields a drain current $(I_{\rm ds})$ of 1 nA/μm. The maximum and minimum values of $I_{\rm ds}$ at $|V_{\rm ds}| = 5$ V are designated as $I_{\rm on}$ and $I_{\rm off}$, respectively.

III. Results and Discussions

A. Basic Characteristics of FSD, CN, and SB TFTs

Fig. 5 compares the typical transfer characteristics of FSD and CN TFTs, both n- and p-channel. The nominal channel length (L) and channel width (W) are 4 and 1 μm, respectively. The key device parameters are summarized in Table I(a). Obvious improvement in device characteristics is obtained for FSD nTFTs in comparison with CN nTFTs. As listed in Table I, the SS decreases from 0.68 to 0.45 V/Dec, the $\mu_{\rm FE}$ increases from 16.9 to 141.5 cm^2/V-sec, and the $I_{\rm on}/I_{\rm off}$ ratio increases from 1.4×10^7 to 3.3×10^7. Excellent FSD pTFTs are also obtained after NH_3 plasma treatment. For the CN TFTs, the small driving current can be attributed to the parasitic resistance at nonsilicided S/D. On the other hand, the superior driving capability of the FSD devices is resulted from the low series resistance due to the FSD and the low contact resistance of the SDE region [18]. Since the ion-implantation process does not damage poly-Si layer directly, the junction would be free of crystalline defects. Therefore, the $I_{\rm off}$ of FSD TFTs is almost identical to (for n-channel) or smaller (for p-channel) than that of the CN TFTs; although a very low-thermal budget (600 °C, 30 s) was used in the ITS process. It has been reported that the reverse leakage current of a P^+/N diode is smaller than that of N^+/P diode with the same ITS process, which is attributed to the faster diffusion coefficient of Boron than that of Phosphorous in Si [10]–[14]. For the FSD pTFT, the SDE is wide enough and the SDE region is not damaged by S/D implantation so that the $I_{\rm off}$ of FSD pTFT is lower than that of the CN pTFT. For the FSD nTFT, the shorter SDE region due to the slower diffusion rate of Phosphorous may be depleted at high $V_{\rm ds}$ so that the $I_{\rm off}$ is higher than that of the CN ones.

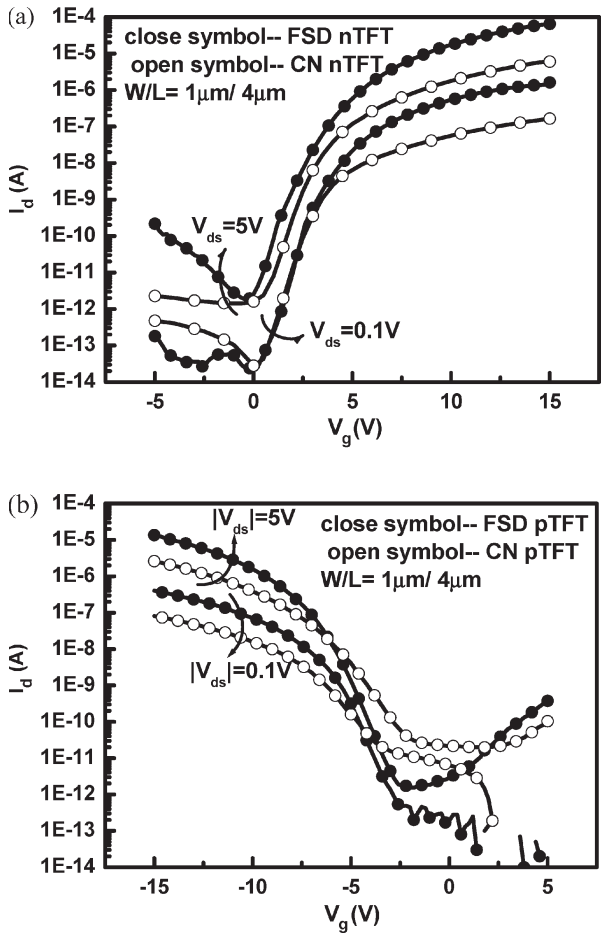

Fig. 5. Typical transfer characteristics of (a) n-channel and (b) p-channel FSD and CN TFTs after NH_3 plasma treatment.

TABLE I
EXTRACTED DEVICE PARAMETERS OF (a) FSD AND CN TFTS AND (b) SB TFTS

(a)

	$V_{th,lin}$ (V)	S.S. (V/Dec)	μ_{FE} (cm^2/ V-sec)	$I_{on}/I_{off}@V_{ds}$=5V
FSD nTFT	3.4	0.45	141.5	$3.3x10^7$
CN nTFT	3.6	0.68	16.9	$1.4 x10^7$
FSD pTFT	-6.3	0.72	55.2	$2.2 x10^7$
CN pTFT	-6.4	0.85	10.7	$1.3 x10^5$

(b)

	$V_{th,lin}$ (V)	S.S. (V/Dec)	μ_{FE} (cm^2/ V-sec)	$I_{on}/I_{off}@V_{ds}$=5V
SB nTFT	5.1	0.97	49.6	$3.1 x10^4$
SB pTFT	-9.3	0.55	21.4	$2.63 x10^6$

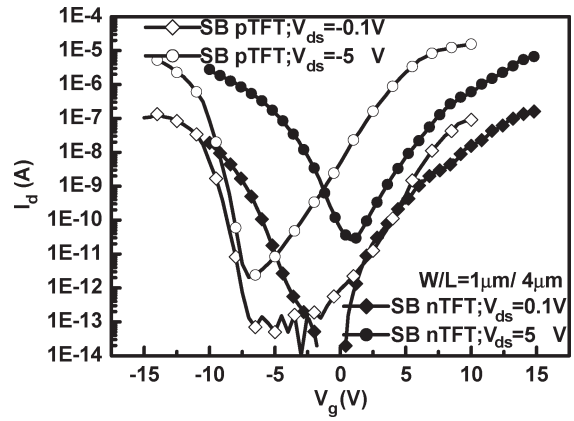

Fig. 6. Typical transfer characteristics of SB n- and p-channel TFTs after NH_3 plasma treatment.

Fig. 6 shows the transfer characteristics of SB nTFT and SB pTFT. The nominal channel length (L) and channel width (W) are 4 and 1 μm, respectively. For the SB TFTs, although the resistance of the S/D electrode can be effectively reduced by the FSD structure, low driving current is observed because of the abnormal high carrier-injection resistance between silicide and channel at onstate. Moreover, at offstate, abnormal high leakage current attributed to the field emission and thermionic emission of carriers from the drain is also predicted. For example, at SB nTFTs, at offstate, holes at drain will inject through the SB at interface of silicide/channel and then into channel. Similar phenomena could also be deduced at p-channel devices [19]. The measured devices parameters of the SB TFTs are summarized in Table I(b). To conclude briefly, the proposed FSD devices have superior characteristics to SB and CN ones.

B. S/D Parasitic Resistance

Fig. 7 shows the typical output characteristics (I_d–$V_{\rm ds}$) of the FSD and CN nTFTs at several different gate voltages with $W/L = 1$ μm/4 μm. Obviously, FSD TFTs exhibit a higher driving current than CN ones, especially under high gate bias. It is because that the channel resistance becomes smaller at high gate bias; hence, the dominant resistance is the S/D parasitic resistance (R_p) [9]. The linear-region parasitic resistance (R_p) can be extracted by plotting the width-normalized onstate resistance $(R_{\rm on})$ versus channel length (L) [19]. In Fig. 8(a), all of the $R_{\rm on} - L$ lines merge at about $L = 0.31$ μm and have a residual value of a gate-voltage independent R_p of 1.35 k$\Omega - \mu$m. In Fig. 8(b), the extracted R_p of CN TFTs is 17.63 k$\Omega - \mu$m, which is about 13 times larger than that of FSD TFTs. As a result, the FSD nTFTs have smaller R_p and better turn-on characteristics than the CN ones.

C. Effects of Activation Temperature

The activation temperature is the most important process parameters to form SDE and to activate dopants in the ITS process. To avoid the influence of dopants segregation, a heavy dose of 5×10^{15} cm^{-2} was used to study the effect of activation temperature [21]. The transfer characteristics of FSD nTFT and pTFT experienced different activation temperatures without NH_3 plasma treatment are shown in Fig. 9(a) and (b), respectively. The extracted device parameters of FSD n and pTFTs are listed in Table II(a) and (b), respectively.

The devices activated at 600 °C and 650 °C result in the best performance for both FSD n and pTFTs. The slight deviation of $V_{\rm th}$, SS, $\mu_{\rm FE}$, as well as $I_{\rm on}/I_{\rm off}$ current ratio may come

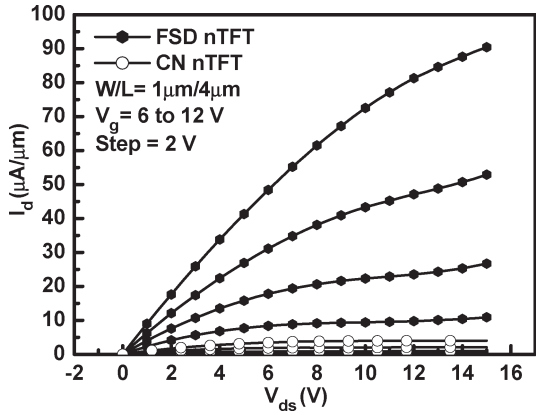

Fig. 7. Typical output characteristics of the FSD and CN nTFTs after NH_3 plasma treatment.

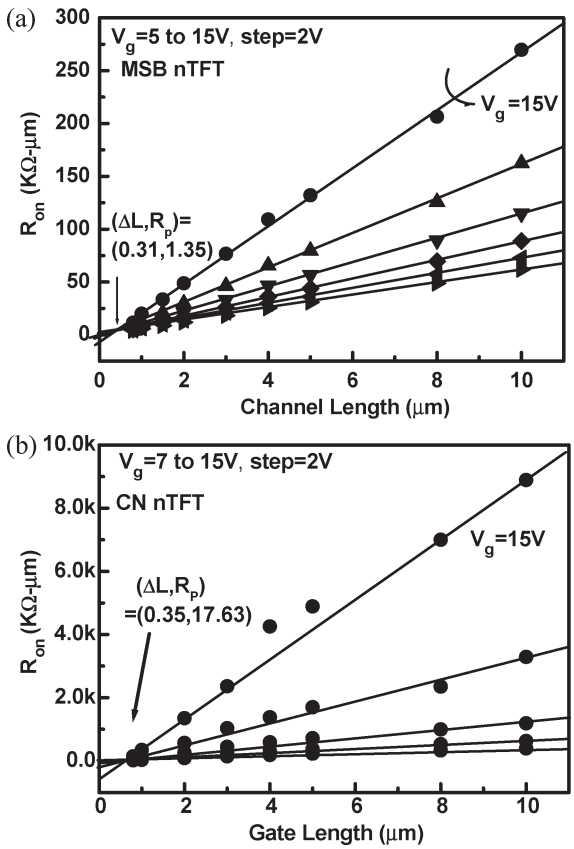

Fig. 8. Channel width-normalized onstate resistance $(R_{\rm on})$ as a function of channel length (L) of (a) FSD nTFTs and (b) CN nTFTs.

from the process deviation. By increasing the RTA temperature to higher than 650 °C, the degradation of absolute value of $V_{\rm th}$, SS, $\mu_{\rm FE}$, and N_t extracted using the modified Levinson's method are clearly observed [22], [23]. However, the offstate current $(I_{\rm off})$ slightly decreases with the increase of RTA temperature. It is well known that the $I_{\rm off}$ of the TFT device is dominated by the quality of the S/D junction [24]. The continuous reduction of $I_{\rm off}$ implies that the higher activation temperature results in longer diffusion length and higher dopant concentration of SDE.

In order to distinctly clarify the degradation mechanisms of devices with high annealing temperature, not only the effective

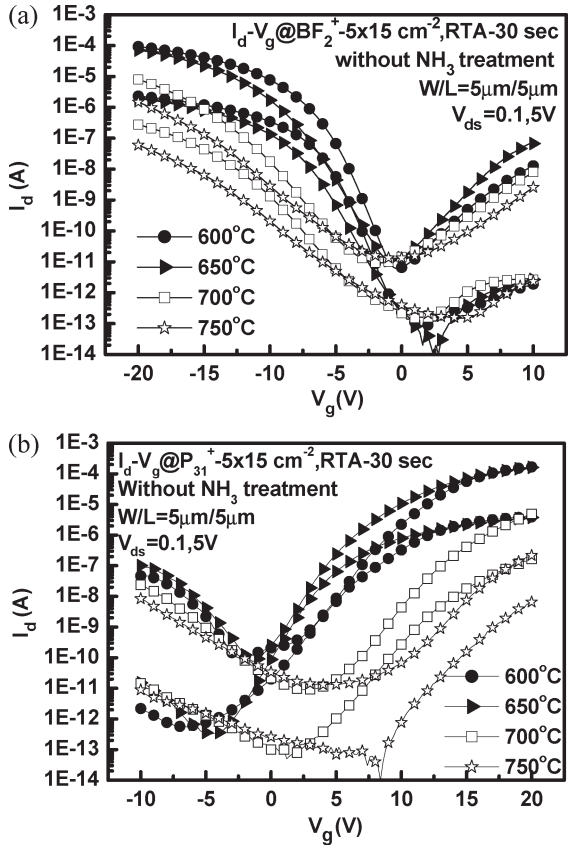

Fig. 9. Typical transfer characteristics of (a) n-channel and (b) p-channel FSD TFTs experienced different activation temperatures without NH_3 plasma treatment.

TABLE II
EXTRACTED DEVICE PARAMETERS OF (a) FSD nTFTs AND (b) FSD pTFTs AFTER DIFFERENT ANNEALING TEMPERATURES FROM 600 °C TO 750 °C FOR 30 S WITHOUT NH_3 PLASMA TREATMENT

(a)

RTA Temperature (°C)	$V_{th,lin}$ (V)	S.S. (V/Dec)	μ_{FE} (cm^2/ V-sec)	I_{on}/I_{off}@V_{ds}=5V
600°C	7.18	1.6	70.6	1.77×10^6
650°C	4.7	1.4	49.9	2.13×10^6
700°C	16.96	1.88	7.3	5.41×10^5
750°C	>20	2.18	0.4	1.66×10^4

(b)

RTA Temperature (°C)	$V_{th,lin}$ (V)	S.S. (V/Dec)	μ_{FE} (cm^2/ V-sec)	I_{on}/I_{off}@V_{ds}=5V
600°C	-6.7	1	33.6	1.52×10^7
650°C	-8.5	1	35	$6.8E \times 10^6$
700°C	-15.3	1.2	9.7	8.6×10^5
750°C	-19.5	2.8	2.9	1.1×10^5

trap-state density (N_t) but also the sheet resistance (R_s) of S/D and gate electrode with different activation temperatures are extracted and shown in Figs. 10 and 11, respectively. As shown in Fig. 10, at the gate electrode, as the annealing temperature increases from 600 °C to 750 °C, the R_s increases obviously

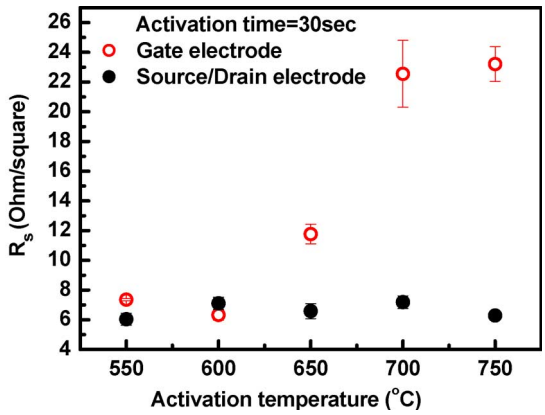

Fig. 10. Sheet resistance (R_s) of gate and S/D electrodes after annealing at different temperatures for 30 s.

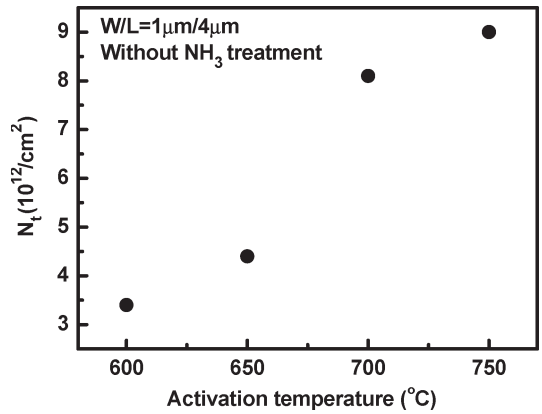

Fig. 11. Effective trap-state densities (N_t) of FSD nTFTs after annealing at different temperatures.

from ∼6.3 to 23.2 Ω/□. Oppositely, at the S/D electrode, the R_s remains stable at about 7 Ω/□ even after 750-°C annealing. Since the S/D integrity is maintained, the device degradation mechanism may be related to the gate electrode. According to the scanning electron microscope (SEM) images of silicide at gate region, as shown in Fig. 12(a)–(d), we also demonstrated that the silicide agglomeration occurs at gate electrode after 650-°C annealing.

The X-ray-diffraction (XRD) spectra of the silicide gate electrode after several annealing conditions are shown in Fig. 13. The main phase of Ni silicide is NiSi after 600-°C annealing. Nevertheless, after 750-°C annealing, both NiSi and $NiSi_2$ were detected. It is known that the thermal stability of Ni-silicide is not as good as that of Ti-silicide or Co-silicide [25]–[28]. Annealing at temperature higher than 700 °C usually results in agglomeration of Ni-silicide [10]. Especially for silicide/polysilicon-stack structure, to reduce the silicide surface energy and the grain boundary energy of the polysilicon, not only the agglomeration but the silicide inversion and intermixing phenomenon have also occurred at temperature lower than that of silicide on crystalline-Si substrate [29], [30]. It has been postulated that the layer inversion and intermixing of silicide at silicide/poly-Si gate electrode may degrade gate dielectric because of the difference in thermal expansion between silicide and polysilicon [31], [32]. Moreover, as the annealing temperature increases, the interface trap-state density of the proposed device also increases obviously, as shown in Fig. 11. Therefore, it is concluded that the gate oxide is damaged due to silicide agglomeration and then the device performance degrades after annealing at temperatures higher than 650 °C. That is why the absolute value of $V_{\rm th}$ increases for both n and pTFTs with the raising of activation temperature. The degradation of SS and $\mu_{\rm FE}$ can also be explained by the same reason.

We can have a short summary now. A 600-°C or 650-°C RTA is sufficient to form excellent FSD pTFTs and nTFTs simultaneously. The FSD region can sustain thermal annealing up to 750 °C. If gate electrode is also fully silicided, the sustainable process temperature is expected to be 750 °C at least. For the application of LTPS TFTs, 600 °C is chosen to be the annealing temperature of the ITS process.

D. Effects of Activation Time

Fig. 14(a) and (b) shows the transfer characteristics of FSD p and nTFTs with different activation times at 600 °C, respectively. The extracted parameters are listed in Table III. For the FSD pTFTs, an activation annealing at 600 °C for 30 s is sufficient to achieve excellent performance and the ON/OFF current ratio can be higher than 10^7 without using hydrogenation treatment. However, it should be noted that the device performance slightly degrades with the increase of activation time. Fig. 15 shows that the R_s of S/D/G electrode remains at about 6–7 Ω/□ after 600-°C annealing for 150 s. Hence, the most possible explanation of device degradation is dopant deactivation [33], [34]. In poly-Si, grain boundaries act as sinks for impurity segregation and also trap carriers at defects due to incomplete atomic bonding. The thermal-equilibrium concentration for dopants increases with the increase of activation temperature, and the major driving force for deactivation is dopant supersaturation. In the ITS process, the heavy dose not only forms an ultrashort SDE but also fills grain boundaries in the short activation time. More activated dopants fill grain boundaries with the longer activation time and dopants deactivate during cool down from activation temperature to room temperature. Dopant deactivation reduces the concentration of the SDE and, therefore, can explain the degradation of some device performances including $V_{\rm th}$, SS, $\mu_{\rm FE}$, and $I_{\rm on}$.

For the FSD nTFTs, similar to the FSD pTFTs, an ultrashort SDE is also formed after a short activation time of 30 s. Unlike boron, phosphorus has small diffusivity [35]. A 30-s activation may be insufficient to form an intact SDE. By increasing activation time, dopants diffuse out of silicide and all of the Ni-silicide grains are surrounded by SDE. Therefore, some device characteristics such as SS and $I_{\rm off}$ are improved. For the reduction of mobility and onstate current $(I_{\rm on})$, dopant deactivation is still a possible reason. Although $I_{\rm on}$ slightly reduces, the $I_{\rm on}/I_{\rm off}$ ratio increases with the increase of activation time. This is explained by the obvious reduction of $I_{\rm off}$. According to these discussions, a 30-s RTA is a suitable activation time for both FSD n and pTFTs.

E. Short-Channel Behavior

The SCE of the FSD and CN TFTs (both n- and p-channel) as evaluated by the threshold-voltage drop with channel-length reduction is shown in Fig. 16. The $\Delta V_{\rm th}$ here is defined as the differences between the $V_{\rm th}$ of short-channel devices and the $V_{\rm th}$ of a 10-μm device. Because of long dopant-diffusion length

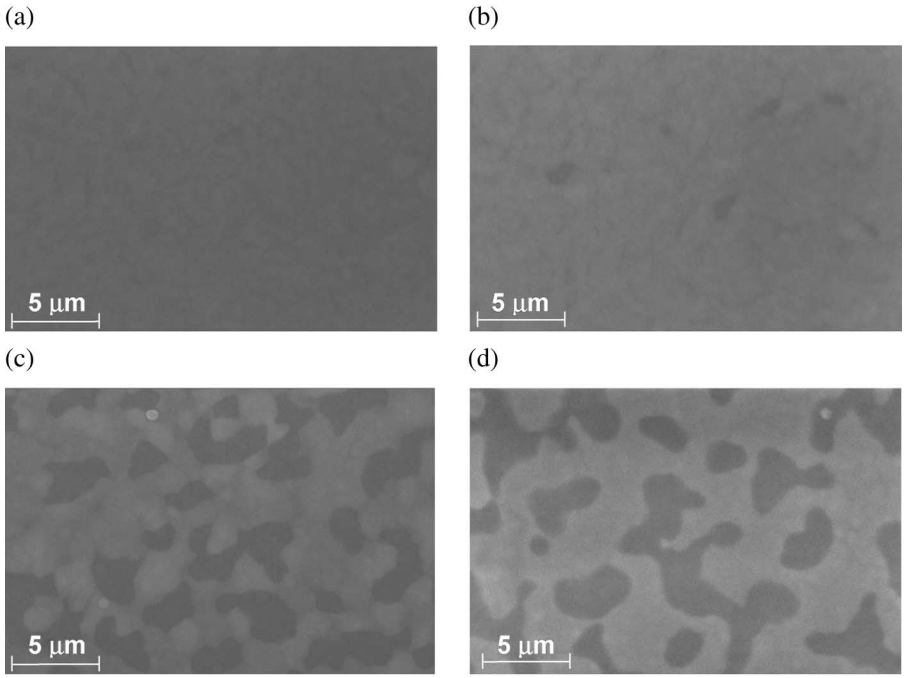

Fig. 12. Plane-view SEM micrographs of the silicided gate electrode of FSD TFTs after annealing at different temperatures: (a) 600 °C; (b) 650 °C; (c) 700 °C; and (d) 750 °C.

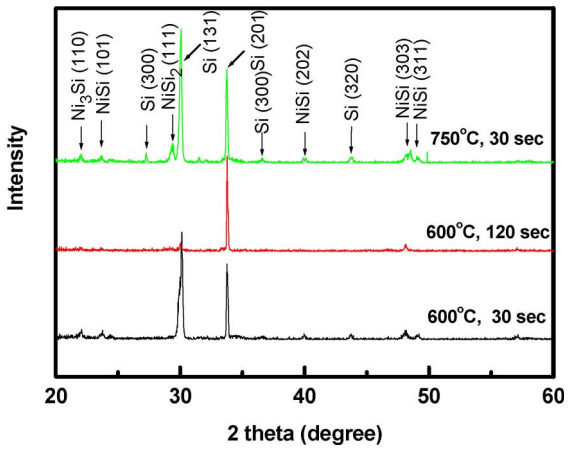

Fig. 13. XRD spectra of the silicided gate electrode of FSD TFTs after annealing at different temperatures and times.

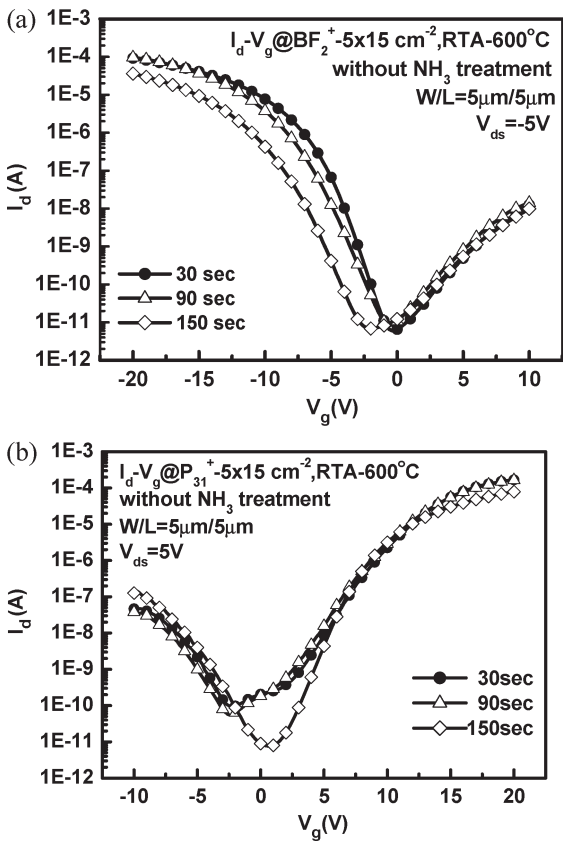

Fig. 14. Typical transfer characteristics of (a) p-channel and (b) n-channel FSD TFTs experienced different activation times without NH_3 plasma treatment.

ascribed to long activation time and fewer grain boundary in the short-channel devices, the $V_{\rm th}$ of CN nTFTs obviously reduces from 7.11 to 2 V and that of CN pTFT reduces from -8.1 to -3.9 V as channel length decreases from 10 to 1.2 μm [36]. On the contrary, in the FSD TFTs, the strongly resist of $V_{\rm th}$ roll off are found for both n and pTFTs. As channel length decreases from 10 to 1.2 μm, $V_{\rm th}$ of FSD nTFTs just slightly reduces from 5 to 4 V and that of FSD pTFTs reduces from -7.5 to -5 V. The excellent short-channel effect of FSD devices can be attributed to not only the shorten SDE by the low-thermal budget ITS process, but also the SDE/silicide effective trap-state density [37], [38].

IV. Conclusion

The concept of high-performance FSD poly-Si TFTs with ultralow parasitic resistance FSD and ultrashort SDE by a simple low-temperature ITS process has been proposed in pTFTs. In this paper, we reported that both FSD n and pTFTs can be fabricated simultaneously. Detailed fabrication process,

TABLE III
EXTRACTED DEVICE PARAMETERS OF (a) FSD nTFTs AND (b) FSD pTFTs AFTER DIFFERENT ACTIVATION TIMES FROM 30 TO 150 s AT 600 °C WITHOUT NH_3 PLASMA TREATMENT

(a)

RTA Time (sec)	$V_{th,lin}$ (V)	S.S. (V/Dec)	μ_{FE} (cm^2/ V-sec)	I_{on}/I_{off}@V_{ds}=5V
30	7.2	1.6	70.6	1.8×10^6
90	6.2	1.5	57.6	3×10^6
150	8.3	1.2	33.9	1×10^7

(b)

RTA Time (sec)	$V_{th,lin}$ (V)	S.S. (V/Dec)	μ_{FE} (cm^2/ V-sec)	I_{on}/I_{off}@V_{ds}=5V
30	-6.7	1	33.6	1.5×10^7
90	-7.1	1	40.1	1.2×10^7
150	-10.6	1.3	20.7	5.2×10^6

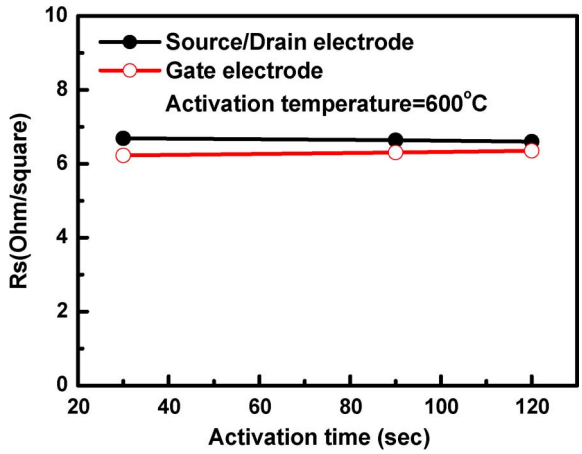

Fig. 15. Sheet resistance (R_s) of gate and S/D electrodes after annealing at 600 °C with different times.

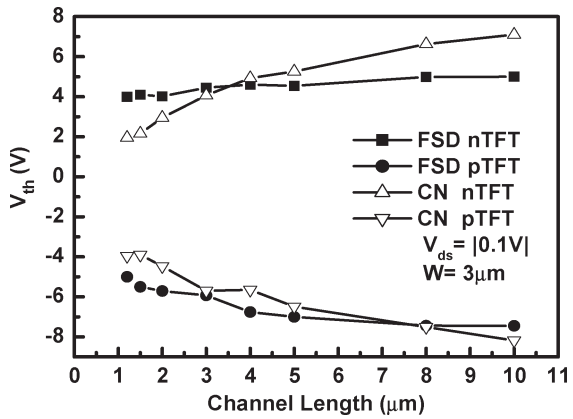

Fig. 16. Threshold voltage ($V_{\rm th}$) roll-off of FSD and CN TFTs. The channel width (W) is fixed at 3 μm.

basic device characteristics, as well as the impact of activation temperature and time of ITS process are all discussed. As the annealing temperature becomes higher than 700 °C, silicide agglomeration occurs at gate electrode and then the electrical characteristics of FSD TFTs degrade. Device degradation due to dopant deactivation of long activation time is also observed. Since the ITS process does not damage the active layer and most dopants are fast diffuser in Ni-silicide, an annealing at 600 °C for 30 s is sufficient to produce excellent FSD n and pTFTs. Therefore, the thermal budget can be suppressed effectively.

The experimental results also show that the proposed devices not only depict improved turn-on characteristics by successfully reducing the S/D parasitic resistance but also maintain the low offstate leakage current. Superior short-channel characteristics are also observed, which is explained by the ultrashort SDE. Therefore, the proposed FSD TFTs are ideally suitable for implementing high-density and high-performance driver circuits on the glass panel for AMLCD, AMOLED, and system-on-panel applications.

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