A Novel Self-Aligned Etch-Stopper Structure With Lower Photo Leakage for AMLCD and Sensor Applications

Chung-Yu Liang, Feng-Yuan Gan, Po-Tsun Liu, F. S. Yeh, Stephen Hsin-Li Chen, and Ting-Chang Chang

***Abstract*—In this letter, the authors introduce a novel self-aligned etch-stopper sidewall-contact hydrogenated amorphous silicon (a-Si : H) thin-film transistor (ESSC-TFT), which reduces the photo leakage current by more than one order of magnitude and increases the ON–OFF ratio to seven orders of magnitude under back light illumination. Such a TFT will enable high-resolution and high-brightness liquid-crystal displays (LCDs) for next-generation TV, monitor, notebook, and mobile-phone applications. This ESSC-TFT design reduces the volume of a-Si film in which the active region can totally be shielded by the gate metal resulting in the prevention from direct back light illumination. With the sidewall contact, the hole current is reduced due to the smaller contact area between drain/source and a-Si layer. As well as the source, drain parasitic intrinsic resistance of a-Si can be also lessened by the ESSC-TFT structure. Although the defects between etched a-Si and n^+ a-Si film may degrade the ON current, the ESSC-TFT still exhibits higher ON–OFF ratio and lower leakage than the one in traditional etch-stopper (ES)-TFT structure. The ESSC-TFT structure can be used not only for TFT-LCD application but also for the applications that demand high ON–OFF ratio and low-leakage device, such as X-ray image sensor.**

***Index Terms*—Hydrogenated amorphous silicon, light-shield, parasitic resistance, self-aligned, thin-film transistor (TFT).**

I. INTRODUCTION

HYDROGENATED amorphous silicon thin-film transistors (a-Si : H TFTs) receive extensive application in active-matrix liquid-crystal display (LCD) [1] and sensors [2] due to their low cost, low-temperature deposition, and ease of deposition across large-area substrates. There are four structures for a-Si : H TFTs: staggered; inverted staggered; coplanar; and inverted coplanar TFTs [3]. Among these four structures, the inverted staggered one is the most popular due to its simple process and acceptable electrical characteristics. Two types of the inverted staggered structures have been widely used as the switching elements to control the gray level in LCD, one is the back-channel-etched (BCE)-TFT structure, while the other one is the etch-stopper (ES)-TFT structure.

Under visible light illumination, the a-Si film will generate large quantities of electron-hole pairs that make a-Si film a well-known photoconductor [3], [4]. Because the working environment of a-Si : H TFT is always under back light illumination, inevitably, it results in high photo leakage and the charges stored in the pixels cannot be conserved during the a-Si : H TFTs are turned off. The conventional ES a-Si : H TFT (ES-TFT), as shown in Fig. 1, exhibits higher reliable electrical performance than conventional BCE structures due to its accurate control of a thinner a-Si film thickness over large-area glass substrates [3]. However, for conventional etch-stop structures, in spite of the bottom-gate metal light-shield, the edges of the a-Si film are still under direct illumination, which raises the photo leakage currents.

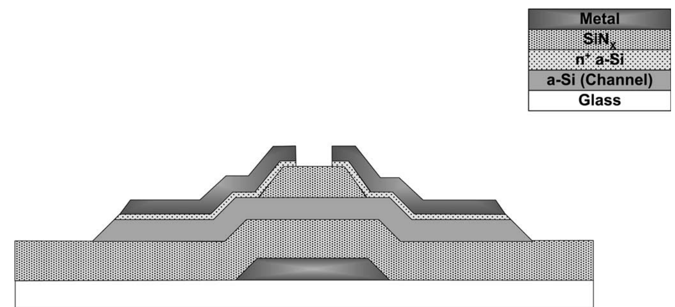

Fig. 1. Conventional ES-TFT structure.

Now, we present the new self-aligned ES sidewall-contact a-Si : H TFT (ESSC-TFT), a new a-Si : H transistor, which allows the conventional ES-TFT to avoid the edges of a-Si from direct back light illumination and reduce the contact area between n^+ a-Si and intrinsic a-Si by the island-in structure, therefore, the photo leakage of the ESSC-TFT structure is improved. Although we expect the reduced parasitic intrinsic a-Si resistance of the ESSC-TFT devices can improve the ON current, we do not see the improvement in this letter. The details will be discussed further in Section III.

II. DEVICE FABRICATION AND STRUCTURE

The fabrication steps for the ESSC-TFT are shown in Fig. 2. There are 40 identical chips that have been made on a

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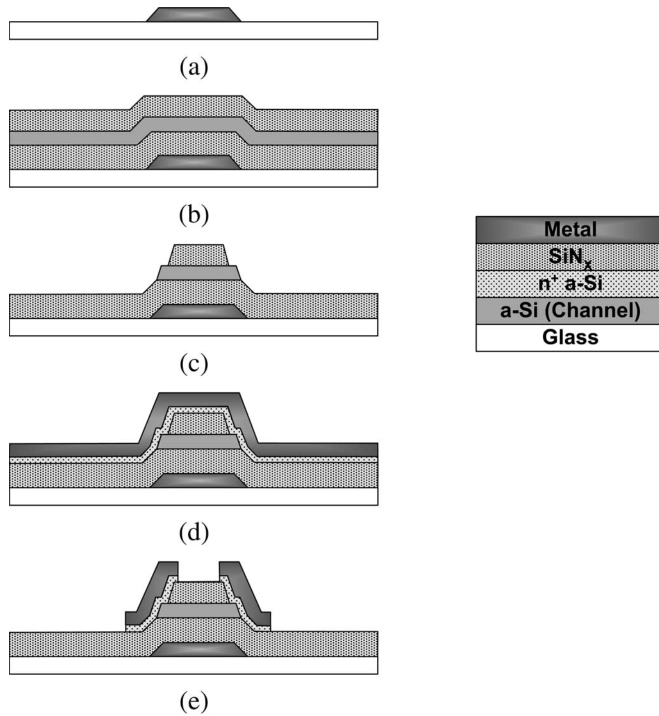

Fig. 2. (a) Gate formed. (b) SiNx/a-Si : H/SiNx(ES) three-layer deposition. (c) Top side (to define the channel width) and backside (to define the channel length) exposures to define the island, than using two-step etching recipes to form the step island. (d) n^+ a-Si and S/D metal deposition. (e) ESSC device formed.

TABLE I
DETAIL PARAMETERS FOR THREE-LAYER DEPOSITION

	Gate SiN_X	a-Si:H	n^+ a-Si:H
SiH_4(sccm)	950	600	600
NH_3(sccm)	4300		
N_2(sccm)	6000		
PH_3(sccm)			1200
H_2(sccm)		2000	4000
Pressure(mtorr)	1200	800	900
Power(W)	3000	2000	900

600×720 mm glass substrate and each chip includes various channel lengths and widths for statistic meanings. First, Mo/AlNd structure was deposited by sputtering technology and, then, patterned to form the gate electrodes [Fig. 2(a)] on a glass substrate. This is followed by the deposition of gate dielectric (400 nm), intrinsic a-Si : H layer (50 nm), and then top nitride (100 nm) consecutively [Fig. 2(b)] by AKT 4300 PECVD system at 350 °C, the detail conditions are shown in Table I. In the conventional ES-TFT structure, the top nitride is then patterned to form an island using the gate metal as a mask for backside exposure to define the channel length, while a-Si : H film remain on the whole substrate. However, in the ESSC-TFT structure, both top-nitride and a-Si : H films were patterned to form the island by dry-etch technology at the same time. A two-step etch process is used to form the step island, noting that the top-nitride layer shrinks into the a-Si layer by 80 nm (as shown in Fig. 3) to prevent the undercut of a-Si layer. The result of these steps is shown in Fig. 2(c). These steps were then followed by the deposition of the n^+ a-Si : H and top-metal

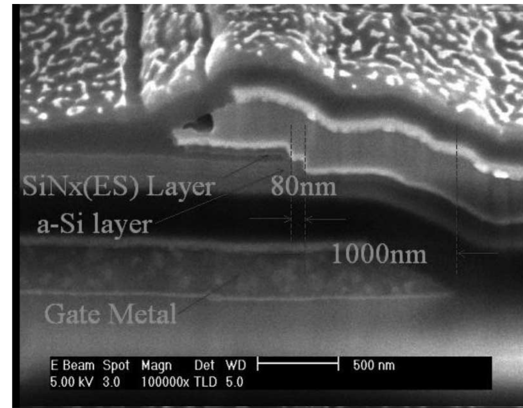

Fig. 3. Two-step etch process cause the top nitride to shrink back by 80 nm.

layers [Fig. 2(d)] and, then, patterned to form the source/drain contacts, as shown in Fig. 2(e).

In our proposal, a two-mask process is possible for the whole ESSC-TFT fabrication by half-tone technology. However, in the present discussion, we perform our ESSC-TFT devices by a three-mask process that is equal to the masks used in the conventional ES and BCE-TFT structures, excluding the passivation and ITO-patterned process.

III. RESULTS AND DISCUSSION

In order to compare the ESSC-TFT device to the conventional ES-TFT device, we fabricated these two-type devices with the same a-Si film thickness, gate insulator thickness, and channel length (L) and width (W). However, to prevent the process variation, we normalized the ON currents by the measured W/L and the capacitance of gate nitride (C_{SiNx}). All the current–voltage $(I–V)$ curves of the device are measured by Agilent 4156C, and the unit capacitance of C_{SiNx} are measured by Agilent 4284 at a fixed small-signal ac frequency of 100 KHz with a circular-shaped capacitor of radius 250 μm near our test devices, and the device dimensions are measured by a Nikon Optiphot 300. Fig. 4(a) shows the transfer characteristics of conventional ES-TFT and our proposed device under the back light of 6000-cd$/\mathrm{m}^2$ illumination.

The conventional ES-TFT device shows a higher photo leakage current under negative-gate-voltage operation. On the contrary, the ESSC-TFT [structure shown in Fig. 2(e)] exhibits extremely low photo leakage due to the ingenious island-in structure. The other reason for the extremely low photo leakage of ESSC-TFT could be due to smaller contact area of sidewall contacts than the one in conventional ES-TFT structures. We also noted that the ON–OFF current ratio is about one order larger than the one with conventional ES-TFT. Fig. 4(b) shows the two types of devices with $I–V$ characteristic curves both at $V_{\mathrm{DS}} = 15$ V. The ES-TFT structure shows higher hole current at higher negative voltage $(V_{\mathrm{GS}} < -15\ \mathrm{V})$ than the one with a novel device structure, the hole current is limited by field-enhanced generation of holes at gate-drain overlap vicinity [5]. In the current novel structure, with the small contact area, the hole current becomes smaller than the one measured in the conventional ES-TFT structure. Moreover, the mobility of the new device is $0.85\ \mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ in comparison to $0.81\ \mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ of

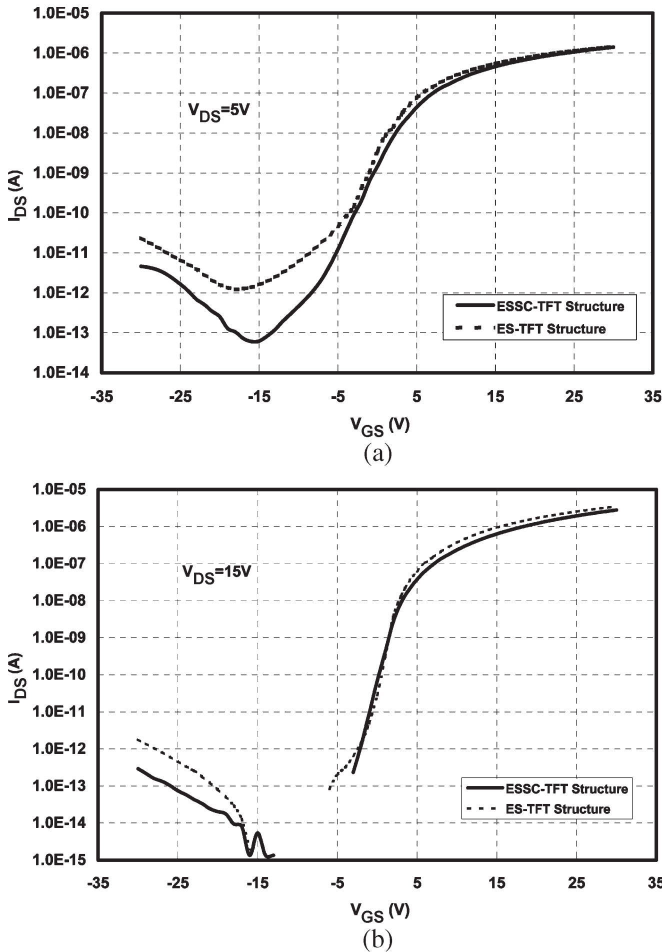

Fig. 4. (a) Normalized $I_{\mathrm{DS}} - V_{\mathrm{GS}}$ curves with the same W/L ratio under 6000-cd/m^2 back light illumination at $V_{\mathrm{DS}} = 5$ V. (b) Normalized $I_{\mathrm{DS}} - V_{\mathrm{GS}}$ curves with the same W/L ratio at $V_{\mathrm{DS}} = 15$ V.

ES-TFT structure, but the threshold voltage of ES- and ESSC-TFT structures are about 1.38 and 1.5 V, respectively, extracted at current density of 1 nA with normalized channel W/L ratio. Fig. 5 shows the $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ curves for ESSC-TFT and ES-TFT; we found that the ON currents and threshold voltages of ESSC-TFT were degraded in comparison to the one in the conventional ES-TFT structure. This is contrary to what we expected, suggesting that the parasitic resistance of ESSC-TFT is reduced by sidewall contacts, which can increase the ON current based on the new device structure [6], [7]. The possible reasons for the degraded ON currents and threshold voltages may be due to the defects created during sidewall-etching process. When doing the island-etching process, the edges of the a-Si film may be damaged by ion bombardment and, thus, degrading the threshold voltages and ON currents. Furthermore, although the parasitic resistance is reduced by sidewall contacts, the parasitic resistance of intrinsic a-Si film may not be so significant for a-Si film thickness below 100 nm [8], [9] comparing to the defective interface between a-Si and n$^+$ a-Si film.

IV. Conclusion

In this letter, we have introduced a new ESSC-TFT structure, which exhibits lower leakage current than that of conventional

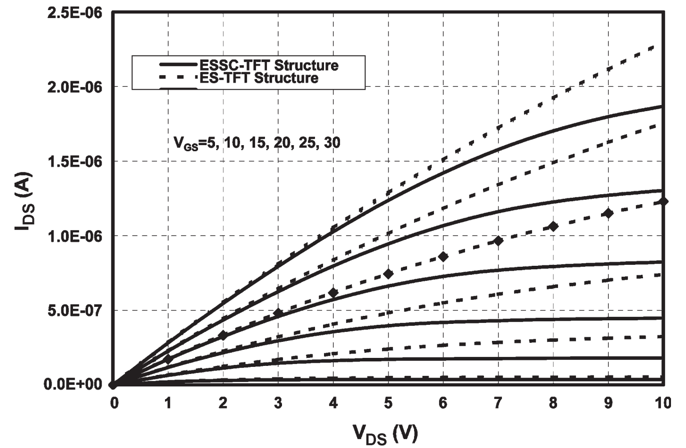

Fig. 5. Normalized $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ curves with $V_{\mathrm{GS}} = 5$, 10, 15, 20, 25, 30 V of ES and ESSC-TFT structures.

ES-TFT structure under back light illumination and dark environments, respectively. Although the ON currents may slightly be degraded by the etching process, the ON–OFF current ratio under back light illumination environment is still much larger than the one in the conventional ES-TFT structure. Such a new TFT device will enable high-resolution and high-brightness LCDs for next-generation applications; besides, the characteristics of lower leakage under dark environment also make ESSC-TFT device a suitable candidate for X-ray image-sensor applications.

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