ESD-Protection Design With Extra Low-Leakage-Current Diode String for RF Circuits in SiGe BiCMOS Process

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***Abstract*—Two low-leakage resistor-shunted diode strings are developed for use as power clamps in silicon–germanium (SiGe) BiCMOS technology. The resistors are used to bias the deep N-wells, significantly reducing the leakage current from the diode string. A methodology for selecting the values of the bias resistors is presented. For further reduction of the leakage current, an alternate design is presented: the resistor-shunted trigger bipolar power clamp. The power-clamp circuits presented herein may be used in cooperation with small double diodes at the I/O pins to achieve whole-chip electrostatic-discharge protection for RF ICs in SiGe processes.**

***Index Terms*—Electrostatic discharge (ESD), modified resistor-shunted diode string (MR diode string), MR trigger bipolar ESD power clamp, power-rail ESD clamp circuit, resistor-shunted diode string (RS diode string), RS trigger bipolar ESD power clamp.**

I. Introduction

The SILICON–GERMANIUM (SiGe) BiCMOS technology with great RF performance of SiGe HBT has been recognized as one of the best technology solutions for wireless applications. Electrostatic-discharge (ESD) protection [1], [2], which has been a very important reliability issue in IC production, should be taken into consideration during circuit design and chip layout. In order to protect internal circuits from ESD damage, the power-rail ESD clamp circuit needs to be designed with the ESD diodes at I/O pins to achieve whole-chip ESD protection [3]. Fig. 1 shows the typical on-chip RF ESD-protection scheme in which the ESD diodes at I/O pins are codesigned with the power-rail ESD clamp circuit [4]–[6]. ESD stress may have positive or negative voltages on an input or output pin with respect to the grounded VDD or VSS pins. For comprehensive ESD verification, the pin-to-pin ESD stress and VDD-to-VSS ESD stress had also been specified to verify the whole-chip ESD robustness. Thus, the ESD clamp circuit between the power rails is very helpful for protecting RF I/O pins and RF core circuits against ESD damage [6]. Diode string is one solution that has been applied in the power-rail ESD clamp circuits [7], [8], which is operated in forward-biased condition to discharge ESD current. Therefore, it can sustain a very high ESD level in a small silicon area.

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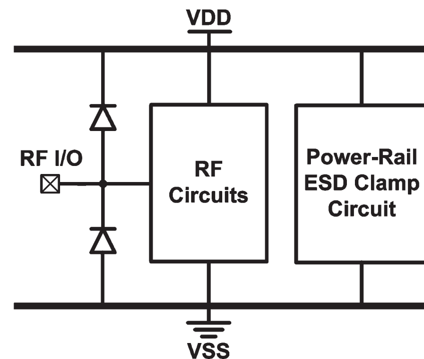

Fig. 1. Typical on-chip RF ESD-protection scheme with codesigned input ESD diodes and the power-rail ESD clamp circuit. The diode string has been applied in the power-rail ESD clamp circuit.

However, the main drawback for using diode string as power-rail ESD clamp circuit is leakage current, especially at high temperatures. A parasitic vertical p-n-p bipolar junction transistor (BJT) exists in the conventional P+/N-well diode with the common grounded P-type substrate. This parasitic vertical p-n-p BJT causes high leakage current along the diode string [7]–[9], especially at high temperatures. Some modified designs on the diode string to reduce leakage current had been reported in [8], which are referred to as the cladded diode string, boosted diode string, and cantilever diode string. However, those designs, which have been verified in a bulk CMOS technology, still have high leakage current (~mA) at the temperature of 125 °C [9]. In SiGe processes, deep trench (DT) has been used to reduce substrate leakage current of diode string [10], [11]. With the DT and N+ buried layer in SiGe process, the parasitic vertical open-base p-n-p BJT can be formed in the diode string because the N+ buried layer is floating [11]. As a result, the substrate leakage current is lower than that of the conventional P+/N-well diode string in CMOS processes.

Although Fig. 1 is applicable not only to RF circuits, this paper focuses on power-rail ESD clamp-circuit design in SiGe BiCMOS process, which is always dedicated to RF applications. The importance of effective power-rail ESD clamp circuits for RF ESD-protection design in SiGe BiCMOS processes has been demonstrated in [1], [2], [12], and [13]. Moreover, the study on diode strings used in power-rail ESD clamp circuits with reduced leakage current has been reported for RF ESD-protection applications [10], [11]. With the effective power-rail

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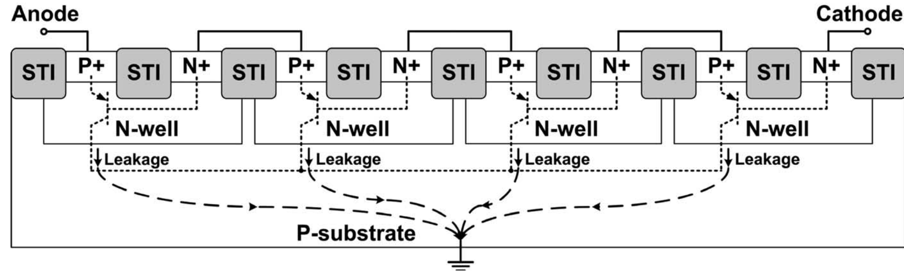

Fig. 2. Cross-sectional view of the conventional diode string with four stacked diodes in CMOS technology.

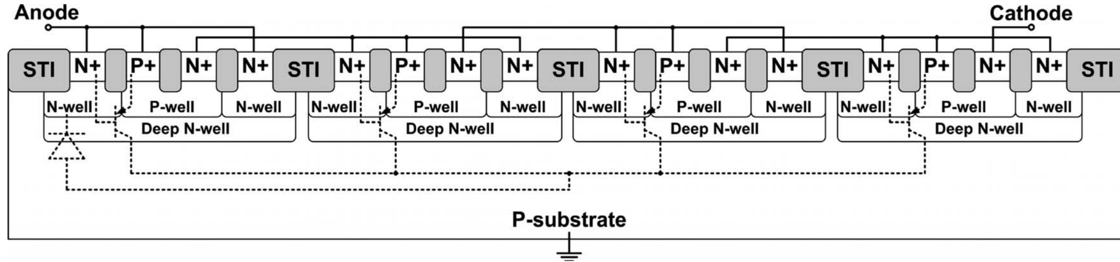

Fig. 3. Cross-sectional view of the four-stage diode string and its parasitic base–emitter tied p-n-p BJTs in a triple-well CMOS process.

ESD clamp circuits, the sizes of ESD-protection devices at the RF input node can be further reduced without sacrificing ESD robustness. Therefore, the impact of the ESD-protection circuit on the RF performance can be minimized. However, the main concern on the effective power-rail ESD clamp circuits designed with diode strings is the leakage issue in circuit normal operations, especially under a high-temperature environment.

In this paper, four power-rail ESD clamp circuits for RF ESD-protection design in SiGe BiCMOS technology are proposed, which are the resistor-shunted diode string (RS diode string), RS trigger bipolar ESD power clamp [14], modified resistor-shunted diode string (MR diode string), and MR trigger bipolar ESD power clamp. In the new proposed RS and MR diode strings, extra biases are applied to the deep N-well regions of the RS and MR diode strings to reduce leakage current. The characteristics of these new proposed power-rail ESD clamp circuits are also compared with those of the conventional diode string in a 0.18-μm SiGe BiCMOS process.

II. Review on Diode Strings

A. Conventional Diode String in CMOS Technology

The cross-sectional view of the conventional four-stage diode string is shown in Fig. 2. Because of the parasitic vertical p-n-p BJTs in the forward-biased diodes, holes are injected from the P+ emitter into the N-well base, and part of holes are swept to the P-substrate collector. Consequently, the substrate leakage current in the conventional diode string is formed. If the current gain of the parasitic vertical p-n-p BJT is greater than unity, the total blocking voltage across the diode string cannot be linearly increased by increasing the number of stacked diodes in the diode string. This implies that more diodes would be needed to provide the desired blocking voltage. To reduce the leakage current of the conventional diode string, three modified designs had been reported in [7] and [8].

B. Modified Diode String to Reduce Leakage Current

A modified design to reduce leakage current by using triple-well technologies had been reported in [10]. Fig. 3 shows the cross-sectional view of the four-stage diode string with its parasitic base–emitter tied p-n-p BJTs in a triple-well CMOS process. The base–emitter junction cannot be forward-biased because the base and emitter are tied together. As a result, holes will not be injected into the base region of the parasitic vertical p-n-p BJT, and the current will flow through the P-well region to the next diode. Thus, the base–emitter tied configuration can effectively suppress the substrate leakage current. The substrate leakage current can be kept very small before the triple-well diode string is turned on.

III. New Proposed RS Diode String and RS Trigger Bipolar ESD Power Clamp

A. RS Diode String

The cross-sectional view of the new proposed RS diode string in a SiGe BiCMOS process is shown in Fig. 4. Compared with the conventional P+/N-well diode string, the new proposed RS diode string uses deep N-wells to isolate the P-wells from the common grounded P-substrate. An extra bias through the resistor R is applied through the N-well to the deep N-well to reduce leakage current into substrate. The structure and equivalent circuit of the RS diode string with its parasitic n-p-n BJTs are shown in Fig. 5.

In the new proposed RS diode string, each deep N-well is connected to the anode through a bias resistance R. The connection of deep N-wells to the anode causes the parasitic n-p-n BJTs in the RS diode string to be slightly turned on. The current generated from the slightly turned-on n-p-n BJT in the diode will flow into the next diode in the RS diode string rather than into the common grounded P-substrate. Therefore, the leakage current into the substrate is not increased in this new design.

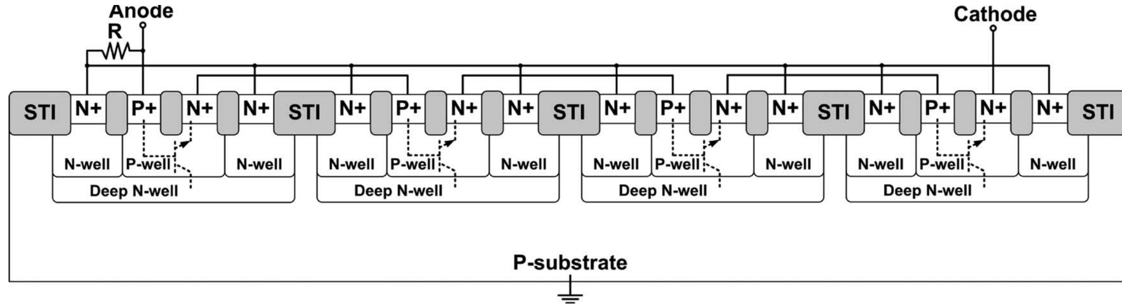

Fig. 4. Cross-sectional view of the new proposed RS diode string with four stacked diodes.

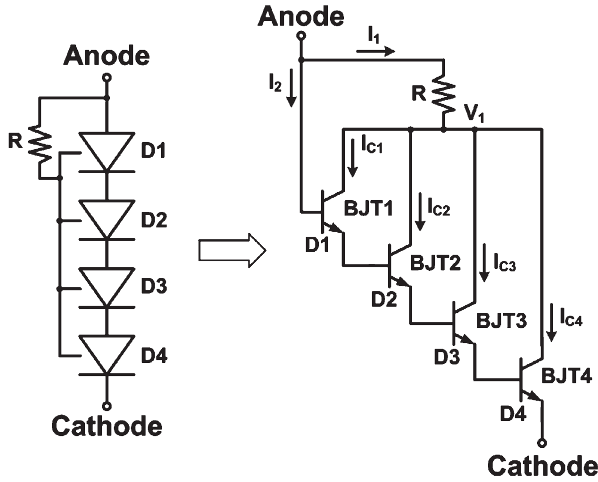

Fig. 5. Structure and equivalent circuit of the new proposed RS diode string with four stacked diodes. When the RS diode string is used as the power-rail ESD clamp circuit, the anode is connected to VDD, and the cathode is grounded.

When the RS diode string is used as the power-rail ESD clamp circuit, the anode is connected to VDD, and the cathode is grounded. The total current flowing into the RS diode string should equal to that flowing out from the RS diode string. The total leakage current of the RS diode string is

$$I_{\text{total leakage}} = I_{C1} + I_{C2} + I_{C3} + I_{C4} + I_2 \tag{1}$$

where all currents have been indicated in Fig. 5. Under normal circuit operating conditions, the RS diode string was designed so as to minimize its leakage current. In the new proposed RS diode string, the parasitic BJT1 was designed to be operated in the saturation mode while the parasitic BJT2, BJT3, and BJT4 were designed to be operated in the forward-active mode under normal circuit operating conditions. The emitter current (I_{E}) and collector current (I_{C}) of each BJT can be expressed in terms of its base–emitter voltage (V_{BE}) and base–collector voltage (V_{BC}) as

$$I_{\text{E}} = \left(\frac{I_{\text{S}}}{\alpha_{\text{F}}}\right)(e^{V_{\text{BE}}/V_{\text{T}}} - 1) - I_S(e^{V_{\text{BC}}/V_{\text{T}}} - 1) \tag{2}$$

and

$$I_{\text{C}} = I_{\text{S}}(e^{V_{\text{BE}}/V_{\text{T}}} - 1) - \left(\frac{I_{\text{S}}}{\alpha_{\text{R}}}\right)(e^{V_{\text{BC}}/V_{\text{T}}} - 1). \tag{3}$$

The base–collector voltage (V_{BC}) of BJT1, base–emitter voltage (V_{BE}) of each BJT, and VDD are derived as

$$V_{\text{BC1}} = R \times I_1 \tag{4}$$

$$V_{\text{BE}n} = V_{\text{T}}\left[\ln(I_{\text{En}} + 1) - \ln(I_{\text{S}})\right], \qquad \text{for } n = 1 \sim 4 \tag{5}$$

and

$$V_{\text{DD}} = \sum_{n=1}^{4} V_{\text{T}}\left[\ln(I_{\text{En}} + 1) - \ln(I_{\text{S}})\right] \tag{6}$$

where I_{S} is the saturation current, V_{T} is the thermal voltage, α_{F} is the common base current gain in the forward-active mode, α_{R} is the common base current gain in the reverse-active mode, and I_{E} and I_{C} are the emitter and collector current, respectively [15]. According to (4)–(6), the emitter and collector currents of BJT1 become

$$I_{E1} = \left(\frac{I_{\text{S}}}{\alpha_{\text{F}}}\right)\left[\frac{(I_{E1}+1)}{I_{\text{S}}} - 1\right] - I_{\text{S}}(e^{RI_1/V_{\text{T}}} - 1) \tag{7}$$

and

$$I_{C1} = I_{\text{S}}\left[\frac{(I_{E1}+1)}{I_{\text{S}}} - 1\right] - \left(\frac{I_{\text{S}}}{\alpha_{\text{R}}}\right)(e^{RI_1/V_{\text{T}}} - 1). \tag{8}$$

It is straightforward that

$$I_{E1} = \frac{\left(\frac{1-I_{\text{S}}}{\alpha_{\text{F}}}\right) - I_{\text{S}}(e^{RI_1/V_{\text{T}}} - 1)}{1 - \frac{1}{\alpha_{\text{F}}}}. \tag{9}$$

From the equivalent circuit, the collector current of BJT2 has current-gain relationship with the emitter current of BJT1, since the emitter current of BJT1 is the base current of BJT2, and BJT2 is in the forward-active mode. Therefore, I_{C2} is given by

$$I_{C2} = \beta_2 I_{B2} = \beta_2 I_{E1} \tag{10}$$

where β_2 is the common emitter current gain of BJT2. Similarly, the collector currents of the BJT3 and BJT4 are

$$I_{C3} = \beta_3 I_{B3} = \beta_2\beta_3 I_{E1} \tag{11}$$

and

$$I_{C4} = \beta_4 I_{B4} = \beta_2\beta_3\beta_4 I_{E1} \tag{12}$$

where β_3 and β_4 are the common emitter current gain of BJT3 and BJT4, respectively. The current that flows through the bias

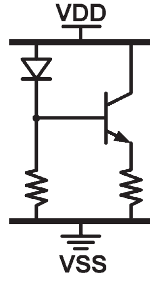

Fig. 6. Power-rail ESD clamp circuit with the diode-triggered HBT in a SiGe BiCMOS process [16].

resistance R is the sum of the four collector currents, which can be derived as

$$I_1 = I_{C1} + I_{C2} + I_{C3} + I_{C4} = I_{C1} + (\beta_2 + \beta_2\beta_3 + \beta_2\beta_3\beta_4)I_{E1}. \quad (13)$$

Therefore, the total leakage current of the RS diode string becomes

$$\begin{aligned} I_{\text{total leakage}} &= (1 + \beta_2 + \beta_2\beta_3 + \beta_2\beta_3\beta_4)I_{E1} \\ &= (1 + \beta_2 + \beta_2\beta_3 + \beta_2\beta_3\beta_4) \\ &\times \frac{\left(\frac{1-I_S}{\alpha_F}\right) - I_S(e^{RI_1/V_T} - 1)}{1 - \frac{1}{\alpha_F}} \\ &= f(R). \end{aligned} \quad (14)$$

The total leakage current of the RS diode string is a function of the bias resistance R and the common emitter current gain β of each BJT. The minimum leakage current can be found by equaling the differentiated expression of the total leakage with respect to R to zero. With this method, the optimized bias resistance to achieve the minimized leakage current can be found from (14).

B. RS Trigger Bipolar ESD Power Clamp

The power-rail ESD clamp circuit with the diode-triggered HBT in a SiGe BiCMOS process had been reported [16], as shown in Fig. 6. However, the leakage (or standby) current of this power-rail ESD clamp circuit is the main concern for low-power or portable applications. To further reduce the leakage current, the new proposed RS trigger bipolar ESD power clamp is shown in Fig. 7 with its equivalent circuit.

The leakage current of the RS trigger bipolar ESD power clamp can be derived in the same way. For the SiGe HBT, the base and collector current can be expressed as functions of V_{BE}. In the RS trigger bipolar ESD power clamp, the parasitic BJT1 is in the saturation mode while the parasitic BJT2, BJT3, and BJT4 are in the forward-active mode under normal circuit operating conditions. The collector and emitter currents of each parasitic BJT are the same as (2) and (3), respectively. The voltage equations in the equivalent circuit of Fig. 7 are given by

$$V_{\text{BC1}} = R \times I_1 \quad (15)$$

$$V_{\text{BE}n} = V_T\left[\ln(I_{\text{E}n} + 1) - \ln(I_S)\right], \qquad \text{for } n = 1 \sim 4 \quad (16)$$

$$V_{\text{DD}} - \sum_{n=1}^{4} V_T\left[\ln(I_{\text{En}} + 1) - \ln(I_S)\right] = V_{\text{BE_HBT}}. \quad (17)$$

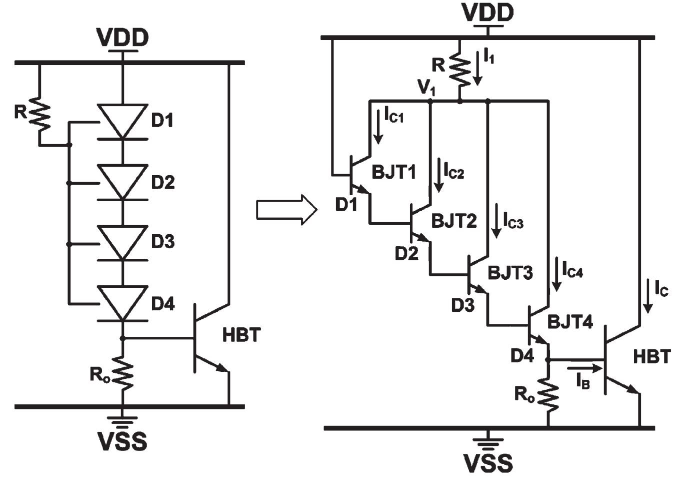

Fig. 7. New proposed RS trigger bipolar ESD power clamp and its corresponding equivalent circuit.

Equation (17) is different from that of the aforementioned RS diode string because the cathode of the RS diode string, which is connected to ground in the pure RS diode string, is now connected to the base of HBT in this design. All currents of the RS diode string will finally flow into the base of HBT and the resistance R_o in this circuit configuration. The total leakage current along the RS trigger bipolar ESD power clamp can be expressed by

$$I_{\text{total leakage}} = \frac{V_{\text{BE_HBT}}}{R_o} + I_B + I_C. \quad (18)$$

The base and emitter currents of the SiGe HBT are given by

$$I_B = \frac{qAD_{\text{pe}}n_i^2}{W_E N_{\text{de}}} e^{V_{\text{BE_HBT}}/V_T} \quad (19)$$

and

$$I_C = \frac{qAD_{nb}n_i^2}{W_B N_{ab}} e^{V_{\text{BE_HBT}}/V_T} \quad (20)$$

where D_{pe} is the diffusion coefficient of holes in the emitter, N_{de} is the donor concentration in the emitter, W_E is the depth of the emitter, D_{nb} is the diffusion coefficient of electrons in the base, N_{ab} is the acceptor concentration in the base, W_B is the basewidth, n_i is the intrinsic carrier concentration, q is the charge on an electron, and A is the area of the emitter/base junction [17].

The resistance R_o between the base of SiGe HBT and ground will affect the total leakage current. Thus, there are two design parameters, R and R_o, in the RS trigger bipolar ESD power clamp for minimizing leakage current.

IV. Modified Design of MR Diode String and MR Trigger Bipolar ESD Power Clamp

A. MR Diode String

The cross-sectional view of the new proposed MR diode string in a SiGe BiCMOS process is shown in Fig. 8. Similar to the RS diode string proposed in last section, the new proposed MR diode string uses deep N-wells to isolate the P-wells

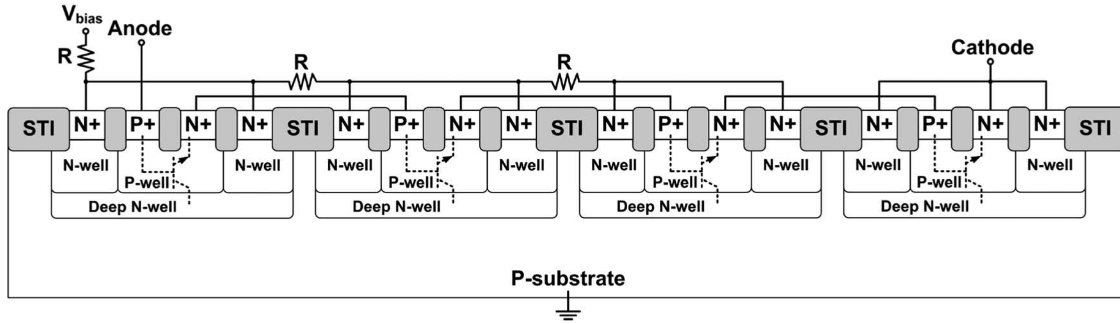

Fig. 8. Cross-sectional view of the new proposed MR diode string with four stacked diodes.

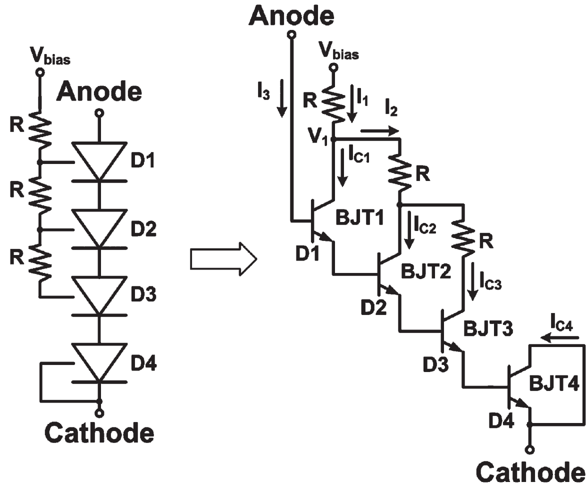

Fig. 9. Equivalent circuit of the MR diode string with four stacked diodes in a SiGe BiCMOS process. When the MR diode string is used as the power-rail ESD clamp circuit, the anode and $V_{\rm bias}$ are connected to VDD, and the cathode is grounded.

from the common grounded P-substrate. Several extra biases through the biasing resistances are applied to the deep N-wells to reduce the leakage current into substrate. The structure and equivalent circuit of the MR diode string with parasitic n-p-n BJTs is shown in Fig. 9.

In the new proposed MR diode string, each deep N-well is connected to the anode through the bias resistances. The common emitter current gain (β) of the parasitic BJT whose collector is connected to a bias resistance can be further reduced in this configuration because each bias resistance connects the collector of a parasitic BJT and the collector of the next one. When current flows through the bias resistance, the voltage drop across it reduces the collector–emitter voltage of the parasitic BJT. As a result, the common emitter current gains of BJT1, BJT2, and BJT3 can be reduced. When the MR diode string is used as the power-rail ESD clamp circuit, the anode and $V_{\rm bias}$ are connected to VDD, and the cathode is grounded.

The total leakage current and the BJT1's collector voltage are given by

$$I_{\text{total leakage}} = I_1 + I_3 \tag{21}$$

$$I_3 = I_{B1} \tag{22}$$

and

$$V_1 = V_{\rm bias} - R \times I_1. \tag{23}$$

In the new proposed MR diode string, the parasitic BJT1, BJT2, and BJT4 were designed to be operated in the saturation mode, while the parasitic BJT3 was designed to be operated in the forward-active mode under normal circuit operating conditions. The following inequality has been demonstrated by the experimental result to validate this design:

$$R \times I_1 < V_{\rm BE1}. \tag{24}$$

The emitter and collector currents of the parasitic BJTs are the same as those in the RS diode string, which are given in (2) and (3). The current I_1 in Fig. 9 is given by

$$I_1 = I_{C1} + I_2 \tag{25}$$

and

$$I_2 = I_{C2} + I_{C3}. \tag{26}$$

Based on (25) and (26), I_1 becomes

$$I_1 = I_{C1} + I_{C2} + I_{C3}. \tag{27}$$

The base–emitter voltage $(V_{\rm BE})$ of each parasitic BJT is given by

$$V_{{\rm BE}n} = V_{\rm T}[\ln(I_{\rm En} + 1) - \ln(I_{\rm S})], \qquad \text{for} \quad n = 1 \sim 4. \tag{28}$$

The base–collector voltage $(V_{\rm BC})$ of BJT1 is

$$V_{\rm BC1} = R \times I_1. \tag{29}$$

The emitter and collector currents of BJT1 can be obtained with similar derivation as in the RS diode string and are given by

$$I_{\rm E1} = \left(\frac{I_{\rm S}}{\alpha_{\rm F}}\right)\left[\frac{(I_{\rm E1}+1)}{I_{\rm S}} - 1\right] - I_{\rm S}(e^{RI_1/V_{\rm T}} - 1) \tag{30}$$

and

$$I_{C1} = I_{\rm S}\left[\frac{(I_{E1}+1)}{I_{\rm S}} - 1\right] - \left(\frac{I_{\rm S}}{\alpha_{\rm R}}\right)(e^{RI_1/V_{\rm T}} - 1). \tag{31}$$

The base–collector voltage $(V_{\rm BC})$ and base–emitter voltage $(V_{\rm BE})$ of BJT2 are

$$\begin{aligned} V_{\rm BC2} &= R \times I_1 + R \times I_2 - V_{\rm BE1} \\ &= R(I_1 + I_2) - V_{\rm T}\ln\left(\frac{I_{E1}+1}{I_{\rm S}}\right) \end{aligned} \tag{32}$$

and

$$V_{\mathrm{BE2}} = V_{\mathrm{T}}\left[\ln(I_{E2}+1) - \ln(I_{\mathrm{S}})\right]. \tag{33}$$

The emitter and collector currents of BJT2 are given by

$$I_{E2} = \left(\frac{I_{\mathrm{S}}}{\alpha_{\mathrm{F}}}\right)\left[\frac{(I_{E2}+1)}{I_{\mathrm{S}}} - 1\right] - I_{\mathrm{S}}\left(\frac{I_{\mathrm{S}}e^{\frac{R(I_1+I_2)}{V_{\mathrm{T}}}}}{I_{E1}+1} - 1\right) \tag{34}$$

and

$$I_{C2} = I_{\mathrm{S}}\left[\frac{(I_{E2}+1)}{I_{\mathrm{S}}} - 1\right] - \left(\frac{I_{\mathrm{S}}}{\alpha_{\mathrm{R}}}\right)\left(\frac{I_{\mathrm{S}}e^{\frac{R(I_1+I_2)}{V_{\mathrm{T}}}}}{I_{E1}+1} - 1\right). \tag{35}$$

Since BJT3 is in the forward-active mode, its collector current can be derived as

$$\begin{aligned} I_{C3} &= \beta_3 I_{B3} = \beta_3 I_{E2} \\ &= \beta_3\left\{\left(\frac{I_{\mathrm{S}}}{\alpha_{\mathrm{F}}}\right)\left[\frac{(I_{E2}+1)}{I_{\mathrm{S}}} - 1\right] - I_{\mathrm{S}}\left(\frac{I_{\mathrm{S}}e^{\frac{R(I_1+I_2)}{V_{\mathrm{T}}}}}{I_{E1}+1} - 1\right)\right\}. \end{aligned} \tag{36}$$

With its collector shorted to the emitter, BJT4 is in the saturation mode. The anode is connected to VDD, and the cathode is grounded when the MR diode string is used as the power-rail ESD clamp circuit. In this case, the base–collector voltage (V_{BC}) and base–emitter voltage (V_{BE}) of BJT4 are equal. Therefore, the emitter and collector currents of BJT4 can be simplified as

$$I_{E4} = \left(\frac{I_{\mathrm{S}}}{\alpha_{\mathrm{F}}} - I_{\mathrm{S}}\right)\left[\frac{(I_{E4}+1)}{I_{\mathrm{S}}} - 1\right] \tag{37}$$

and

$$I_{C4} = \left(I_{\mathrm{S}} - \frac{I_{\mathrm{S}}}{\alpha_{\mathrm{R}}}\right)\left[\frac{(I_{E4}+1)}{I_{\mathrm{S}}} - 1\right]. \tag{38}$$

After considering all parasitic BJTs, the total leakage current of the MR diode string is given by

$$I_{\text{total leakage}} = I_1 + I_3 = I_3 + I_{C1} + I_{C2} + I_{C3} = I_{E1} + I_{C2} + I_{C3}. \tag{39}$$

According to (30), (35), and (36), the total leakage can be calculated. The common emitter current gain (β) of the parasitic BJT is reduced by the bias resistances in the MR diode string. As a result, the total leakage current of the MR diode string can be further reduced. Substituting (30), (35), and (36) for I_{E1}, I_{C2}, and I_{C3} in (39) yields

$$\begin{aligned} &I_{\text{total leakage}} \\ &= \left(\frac{I_{\mathrm{S}}}{\alpha_{\mathrm{F}}}\right)\left[\frac{(I_{E1}+1)}{I_{\mathrm{S}}} - 1\right] - I_{\mathrm{S}}(e^{RI_1/V_{\mathrm{T}}} - 1) \\ &\quad + I_{\mathrm{S}}\left[\frac{(I_{E2}+1)}{I_{\mathrm{S}}} - 1\right] - \left(\frac{I_{\mathrm{S}}}{\alpha_{\mathrm{R}}}\right)\left(\frac{I_{\mathrm{S}}e^{\frac{R(I_1+I_2)}{V_{\mathrm{T}}}}}{I_{E1}+1} - 1\right) \\ &\quad + \beta_3\left\{\left(\frac{I_{\mathrm{S}}}{\alpha_{\mathrm{F}}}\right)\left[\frac{(I_{E2}+1)}{I_{\mathrm{S}}} - 1\right] - I_{\mathrm{S}}\left(\frac{I_{\mathrm{S}}e^{\frac{R(I_1+I_2)}{V_{\mathrm{T}}}}}{I_{E1}+1} - 1\right)\right\} \\ &= f(R). \end{aligned} \tag{40}$$

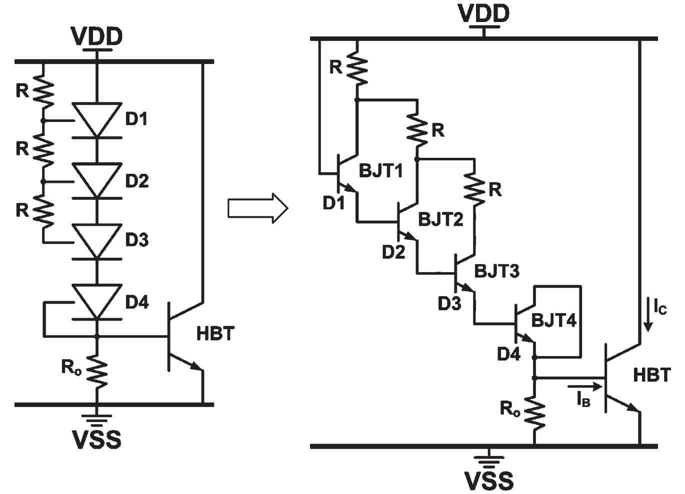

Fig. 10. New proposed MR trigger bipolar ESD power clamp and its equivalent circuit.

The minimum total leakage current of the MR diode string can be found by choosing an appropriate bias resistance with the aid of (40). The total leakage current can be further reduced by using more diodes and bias resistances in the MR diode string.

As shown in (14) and (40), the expressions for the leakage current of the two proposed diode strings are functions of the bias resistance (R), saturation current (I_{S}), common emitter current gain (β), common base current gain (α), emitter current of each BJT, and the current flows through each resistor. Each aforementioned parameter is also a function of the bias resistor (R). Moreover, the aforementioned parameters are dependent to each other. Therefore, it is very complicated to directly derive a simple expression on the optimum resistance, which can minimize the leakage current by hand calculation. To obtain the optimum resistance, methods such as numerical analysis by computer calculation should be resorted. If the exact parasitic n-p-n device parameters can be given, the optimal resistance to have a minimal leakage current can be obtained by HSPICE simulation.

B. MR Trigger Bipolar ESD Power Clamp

The fourth new proposed power-rail ESD clamp circuit is the MR trigger bipolar ESD power clamp, which is shown in Fig. 10 along with its equivalent circuit. The MR trigger bipolar ESD power clamp is also believed to have lower leakage current than the conventional diode string. The total leakage current of the MR trigger bipolar ESD power clamp can be obtained with similar derivation as that in the RS trigger bipolar ESD power clamp. The total leakage current along the MR trigger bipolar ESD power clamp is given by

$$I_{\text{total leakage}} = \frac{V_{\mathrm{BE_HBT}}}{R_o} + I_B + I_{\mathrm{C}} \tag{41}$$

where $V_{\mathrm{BE_HBT}}$, I_B, and I_{C} are expressed in (17), (19), and (20), respectively.

The resistance R_o between the base of SiGe HBT and ground will affect the total leakage current. Similar to the RS trigger

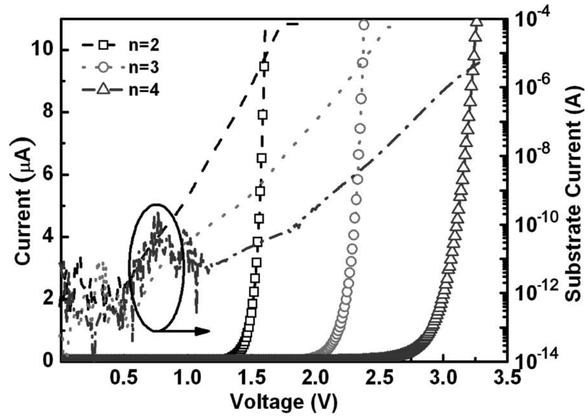

Fig. 11. DC I–V characteristics of the conventional diode string with different numbers ($n = 2, 3,$ and 4) of stacked diodes under the temperature of 25 °C.

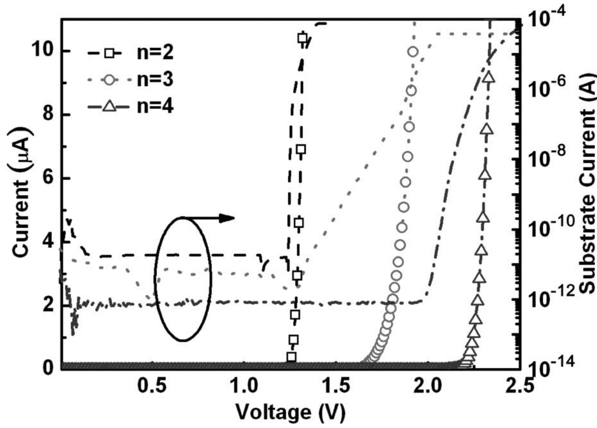

Fig. 12. DC I–V characteristics of the RS diode string with different numbers ($n = 2$, 3, and 4) of stacked diodes under the temperature of 25 °C and the bias resistance of 10 kΩ.

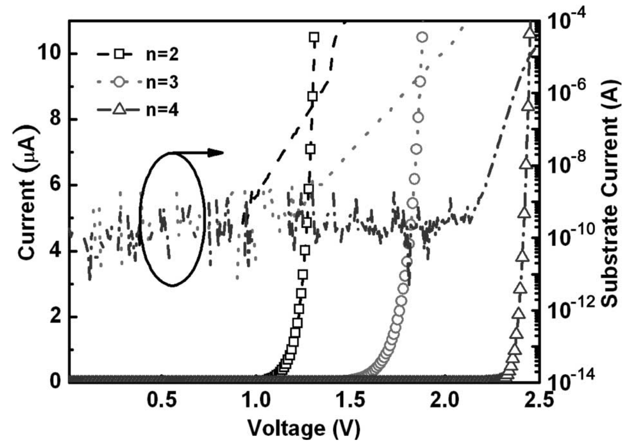

Fig. 13. DC I–V characteristics of the MR diode string with different numbers ($n = 2$, 3, and 4) of stacked diodes under the temperature of 25 °C and the bias resistance of 10 kΩ. The V_{bias} and anode of the MR diode string were shorted in dc I–V measurement.

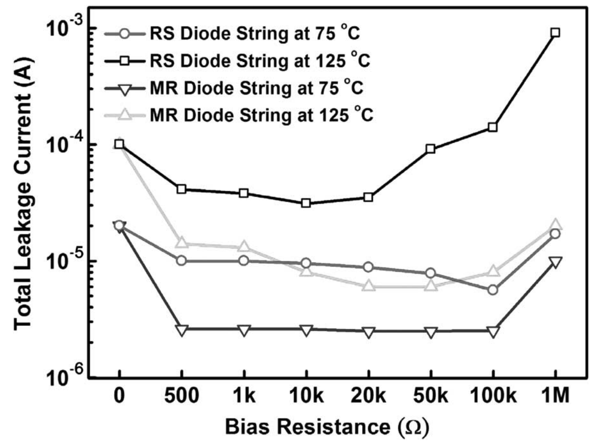

Fig. 14. Relationship between bias resistance (R) and total leakage current of RS and MR diode strings with four stacked diodes and the bias condition of VDD = V_{bias} = 1.8 V, which were measured at the temperatures of 75 °C and 125 °C, respectively.

bipolar ESD power clamp, there are two design parameters R and R_o in the MR trigger bipolar ESD power clamp for minimizing leakage current.

V. Experimental Results

The four new proposed on-chip power-rail ESD clamp circuits had been fabricated in a 0.18-μm SiGe BiCMOS process. The conventional diode string shown in Fig. 2 had also been fabricated in the same process with the same diode layout dimensions for comparison. During the measurement, the cathodes of the RS diode string/MR diode string and the p-substrate were grounded by two separated channels, so that the cathode current and substrate current can be monitored separately. Each diode in this paper has the same device dimension of $W/L = 40\ \mu\text{m}/12\ \mu\text{m}$ in layout pattern. The dc characteristics of the conventional diode string, RS diode string, and MR diode string with different numbers ($n = 2, 3,$ and 4) of stacked diodes are shown in Figs. 11–13, respectively. The V_{bias} and anode of the MR diode string were shorted in the dc current–voltage (I–V) measurement.

The RS and MR diode strings have lower substrate leakage current than that of the conventional diode string, because there are biases applied through the bias resistances into the deep N-well. For the circuit applications with VDD of 1.8 V, the substrate leakage current in the RS diode string (shown in Fig. 12) with four stacked diodes can be two orders of magnitude lower than that of the conventional diode string, as shown in Fig. 11.

The relationship between bias resistance (R) and the total leakage current through the RS diode string and MR diode string with four stacked diodes ($n = 4$) and the bias condition of VDD = V_{bias} = 1.8 V at different temperatures is shown in Fig. 14. The total leakage current through the RS diode string or MR diode string ($n = 4$) is increased when the temperature is increased from 75 °C to 125 °C. As shown in Fig. 14, the total leakage current of the MR diode string is about one order of magnitude lower than that of the RS diode string under the condition of the same bias resistance and temperature. The total leakage current of the RS diode string and MR diode string can be minimized by selecting the appropriate bias resistance with the aid of (14) and (40), respectively. From the measured results of the test chip fabricated in a 0.18-μm SiGe BiCMOS process, the RS and MR diode strings with four stacked diodes have the minimized leakage current at 125 °C by using the

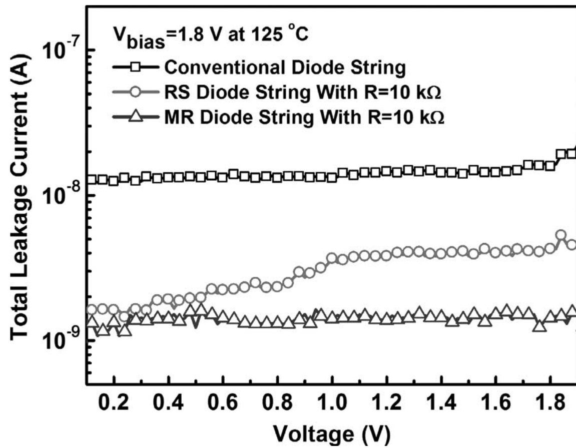

Fig. 15. Comparison on total leakage currents of the conventional diode string, RS diode string, and MR diode string with four stacked diodes ($n = 4$) and $R = 10$ kΩ at 125 °C.

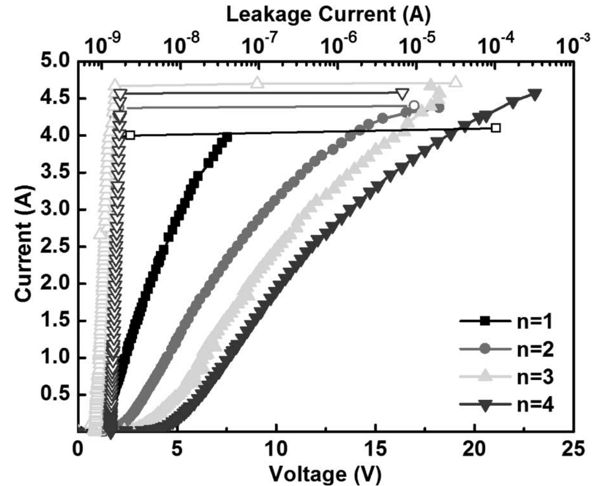

Fig. 17. TLP-measured I–V characteristics of the RS diode string with different numbers (n = 1, 2, 3, and 4) of stacked diodes.

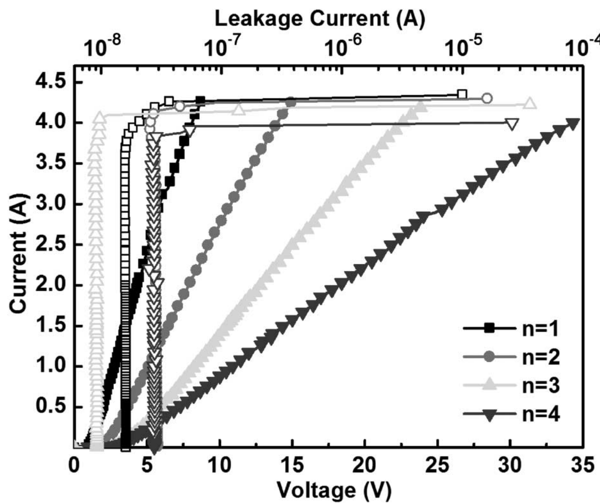

Fig. 16. TLP-measured I–V characteristics of the conventional diode string with different numbers (n = 1, 2, 3, and 4) of stacked diodes.

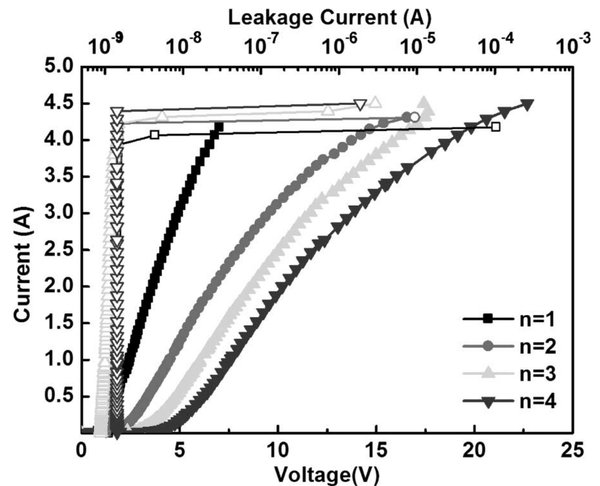

Fig. 18. TLP-measured I–V characteristics of the MR diode string with different numbers (n = 1, 2, 3, and 4) of stacked diodes.

bias resistance of 10 and 20 kΩ, respectively. The relationships between the voltage across the conventional diode string, RS diode string, and MR diode string with four stacked diodes and their total leakage current at 125 °C are compared in Fig. 15. The V_{bias} in the MR diode string is 1.8 V in this measurement. All bias resistances used in this comparison is 10 kΩ for the RS and MR diode strings. The MR diode string has the lowest leakage current, while the conventional diode string has the highest leakage current. As illustrated in Fig. 15, the total leakage current of the MR diode string is about one order of magnitude lower than that of the conventional diode string in the voltage range from 0.1 to 1.9 V.

With a bias resistance of 10 kΩ, the ESD robustness of the conventional diode string, RS diode string, and MR diode string with different numbers of stacked diodes has been investigated by using the transmission-line-pulse (TLP) generator with a pulsewidth of 100 ns. The TLP-measured I–V characteristics of the conventional diode string, RS diode string, and MR diode string with different numbers (n = 1, 2, 3, and 4) of stacked diodes are shown in Figs. 16–18, respectively. The dependence of the secondary breakdown current (It2) of the conventional diode string, RS diode string, and MR diode string on the number (n) of stacked diodes is shown in Fig. 19. The V_{bias} and anode of the MR diode string were shorted together in the It2 measurement. The It2 of the RS diode string and MR diode string are larger than that of the conventional diode string when the number of stacked diodes exceeds two. This implies that the new proposed RS diode string and MR diode string have not only lower leakage current but also higher ESD robustness, as compared to the conventional diode string. With an It2 of greater than 4 A, the new proposed RS diode string and MR diode string with four stacked diodes can sustain the human-body-model ESD stress of ∼6 kV. As shown in Fig. 19, the It2 of the RS diode string and MR diode string does not decrease as the number of stacked diodes increases. Consequently, the number of stacked diodes in the RS and MR diode strings can be reasonably increased to get a higher blocking voltage without degradation in ESD robustness.

A comparison of the total leakage current among the SiGe HBT triggered by the conventional diode string, RS diode string, and MR diode string with four stacked diodes at 125 °C under different R_o resistances is shown in Fig. 20, where all

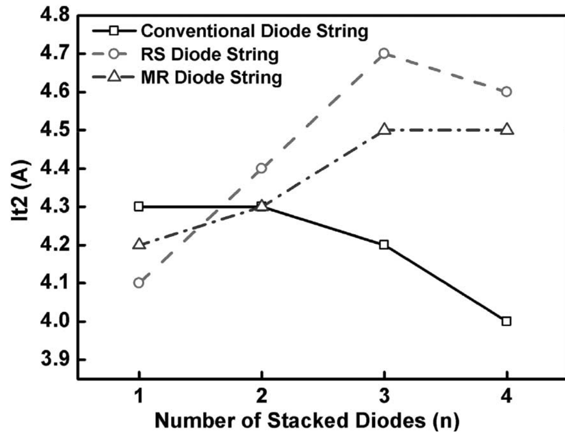

Fig. 19. Dependence of secondary breakdown current (It2) of the conventional diode string, RS diode string, and MR diode string on the number of stacked diodes. The V_{bias} and anode of MR diode string were shorted in the It2 measurement.

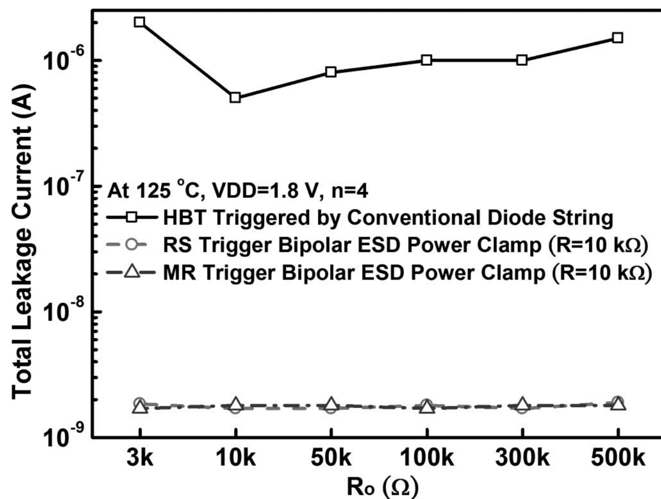

Fig. 20. Comparison on the total leakage currents of the SiGe HBT triggered by the conventional diode string, RS trigger bipolar ESD power clamp, and MR trigger bipolar ESD power clamp under different R_o resistances. All the bias resistances are 10 kΩ with four stacked diodes, bias condition of VDD = 1.8 V, and temperature of 125 °C.

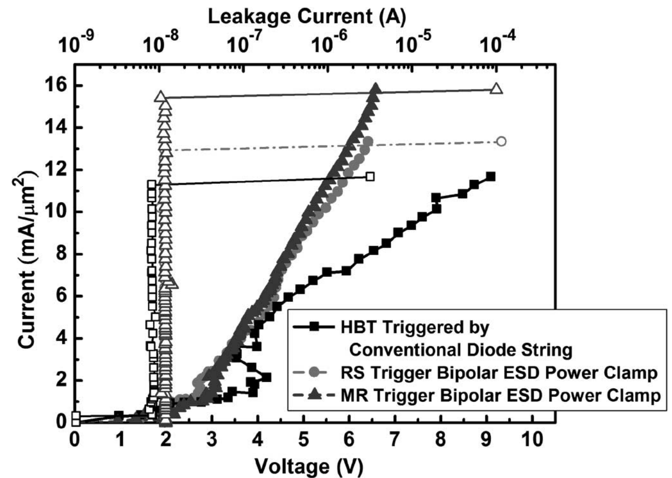

Fig. 21. TLP-measured I–V curves of the SiGe HBT triggered by the conventional diode string, RS trigger bipolar ESD power clamp, and MR trigger bipolar ESD power clamp with four stacked diodes and $R = R_o = 10$ kΩ.

the bias resistances are 10 kΩ, and VDD is 1.8 V. As shown in Fig. 20, The total leakage current of the new proposed RS trigger bipolar ESD power clamp and MR trigger bipolar ESD power clamp is about two orders of magnitude lower than that of the HBT triggered by the conventional diode string with the same number of stacked diodes and the same HBT device dimension.

As compared with the conventional string, the leakage current is reduced by using the RS diode string. According to Fig. 5, the potentials at the collector electrodes of the four parasitic BJTs are equal. Each base in the parasitic BJT is connected to the emitter of the preceding parasitic BJT, and the base of the parasitic BJT1 is connected to the anode. As a result, the parasitic BJT1 is in the saturation mode while the parasitic BJT2, BJT3, and BJT4 are in the forward-active mode under normal circuit operating conditions. Therefore, the BJT current will be amplified by a factor of $\beta + 1$ through each forward-active parasitic BJT. Consequently, the leakage current increases as the number of forward-active parasitic BJTs increases. For the purpose of decreasing the number of forward-active parasitic BJTs, the modified design of the MR diode string is proposed and shown in Fig. 9. The common emitter current gain (β) of the parasitic BJT whose collector is connected to a bias resistance can be further reduced in this configuration, because the voltage drop across the bias resistance reduces the collector–emitter voltage of the parasitic BJT. In the MR diode string, the parasitic BJT1, BJT2, and BJT4 are in the saturation mode while only the parasitic BJT3 is in the forward-active mode under normal circuit operating conditions. With only one forward-active parasitic BJT, the leakage current is minimized by the new proposed MR diode string.

When the SiGe HBT is applied as the ESD clamp device, the HBT should be taken into consideration to evaluate the leakage current. Because the leakage current of the RS diode string is not minimized, the SiGe HBT forms the fifth base–emitter junction in series with the existing four base–emitter junctions between VDD and VSS. Thus, the leakage current of the RS diode string can be further reduced by using the RS trigger bipolar ESD power clamp. On the other hand, since the leakage current of the MR diode string is already minimized, applying the SiGe HBT cannot further reduce the leakage current significantly. Therefore, as shown in Figs. 15 and 20, the leakage current of the MR diode string, RS trigger bipolar ESD power clamp, and MR trigger bipolar ESD power clamp is almost the same, which is around 1.5–2 nA.

The TLP-measured I–V curves of the SiGe HBT triggered by the conventional diode string, RS trigger bipolar ESD power clamp, and MR trigger bipolar ESD power clamp with four stacked diodes and $R = R_o = 10$ kΩ are compared in Fig. 21, where the current is normalized to the emitter area of the SiGe HBT. As shown in Fig. 21, the MR trigger bipolar ESD power clamp has the lowest turn-on resistance, while the HBT triggered by the conventional diode string has the highest turn-on resistance. ESD clamp device with lower turn-on resistance would have lower voltage across itself during ESD stress. Thus, the voltage on the input node of the circuit to be protected would be lower during ESD stress. Accordingly, the MR trigger

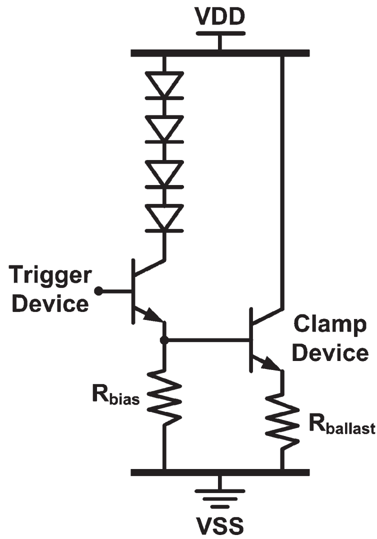

Fig. 22. Power-rail ESD clamp circuit designed with diode string for mixed-voltage applications [12].

bipolar ESD power clamp can sustain the highest It2 per unit emitter area, which implies to have the highest ESD robustness among these three designs. To sustain a higher ESD level, the SiGe HBT with a larger device dimension should be used in power-rail ESD clamp circuits.

VI. Comparison With Previously Reported Diode Strings

A recently reported power-rail ESD clamp circuit designed with diode string for mixed-voltage applications is shown in Fig. 22 [12]. According to Fig. 22, the power-rail ESD clamp circuit consists of a two-stage Darlington clamp network using a SiGe HBT trigger with base open and SiGe HBT clamp element. In a power-rail ESD clamp circuit, the clamp device must have a high breakdown voltage to sustain the voltage between VDD and VSS, while the trigger device should have a low breakdown voltage to immediately initiate the base current into the clamp device before the voltage across the power-rail ESD clamp circuit damages the core circuits. Thus, the trigger HBT with low breakdown voltage and high cutoff frequency (f_T) and the ESD clamp HBT with high breakdown voltage and low cutoff frequency (f_T) are used in this power-rail ESD clamp circuit.

When the collector-to-emitter voltage of the HBT is below the breakdown voltage, no current flows through the trigger HBT. Therefore, with base grounded, the clamp HBT is not turned on under normal circuit operating conditions. Under ESD condition, the voltage on VDD exceeds the collector-to-emitter breakdown voltage $(\mathrm{BV_{CEO}})$, and current flows into the base of the ESD clamp HBT to discharge the ESD current from VDD to VSS. The resistor R_{ballast} is used for resistor ballasting to improve ESD robustness. The trigger voltage of the power-rail ESD clamp circuit can be varied by changing the number of series varactors.

Another ESD-protection circuit designed with diode string for mixed-voltage interface, which is referred to as the snubber-clamped diode string, is shown in Fig. 23 [13]. In this mixed-voltage interface ESD-protection circuit, the diode string is placed between the I/O pad and VDD to protect the 3.3-V/5-V mixed-voltage interface circuit. The diode string forms a multi-stage BJT amplifier in a Darlington configuration. The bipolar base current is amplified by each successive stage when each stage is in the forward-active mode. To break the Darlington effect of amplifying the leakage current, three additional snubber diodes are placed on the base electrodes of the parasitic BJTs. With the snubber diodes, the base voltage of the parasitic BJT is clamped, and the leakage current amplification is limited. Any elements, such as resistors, p-channel MOSFETs, or diodes, which can prevent a forward-active condition of the parasitic BJT, can be used to limit the Darlington amplification. The snubber-clamped diode string, RS diode string, and MR diode string proposed in this paper utilize the same concept to reduce the leakage current, which is preventing the parasitic BJTs of the diode string from being in the forward-active mode to amplify the leakage current. In the snubber-clamped diode string, the base potential is boosted by the snubber diodes, while in the RS diode string and MR diode string, the collector potential is lowered by the voltage drop of the bias resistor.

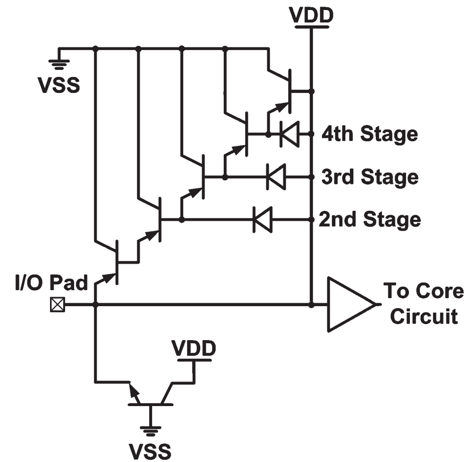

Fig. 23. ESD-protection circuit designed with diode string for mixed-voltage interface [13].

VII. Conclusion

Four new designs to minimize the leakage current of the power-rail ESD clamp circuit realized by diode string for RF circuits had been proposed and verified in a 0.18-μm SiGe BiCMOS process. With an additional extra bias circuit to supply current into the N-well of the diodes in the RS diode string, the overall leakage current of the RS diode string can be reduced. The leakage current can be further reduced and minimized by using the new proposed MR diode string, which is introduced by the similar idea. The design equations to minimize the leakage current in the RS diode string and MR diode string have also been derived in this paper. By selecting the appropriate bias resistance, the total leakage current of the RS diode string and MR diode string can be kept much smaller than that of the conventional diode string. This makes the RS diode string and MR diode string more promising as the on-chip power-rail ESD clamp circuit. Moreover, the RS diode

string and MR diode string have higher ESD robustness than the conventional diode string when the number of stacked diodes exceeds two. Therefore, the new proposed RS diode string, MR diode string, RS trigger bipolar ESD power clamp, and MR trigger bipolar ESD power clamp are very suitable for power-rail ESD clamp circuits in cooperation with the small input ESD diodes to achieve high ESD robustness for RF circuits in the SiGe BiCMOS technology.

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REFERENCES

[1] S. Voldman, *ESD: Circuits and Devices*. New York: Wiley, 2006.
[2] ——, *ESD: RF Technology and Circuits*. New York: Wiley, 2006.
[3] M. D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI," *IEEE Trans. Electron Devices*, vol. 46, no. 1, pp. 173–183, Jan. 1999.
[4] S. Voldman, A. Botula, D. Hui, and P. Juliano, "Silicon germanium heterojunction bipolar transistor ESD power clamps and the Johnson limit," in *Proc. EOS/ESD Symp.*, 2001, pp. 326–336.
[5] M.-D. Ker, W.-Y. Lo, C.-M. Lee, C.-P. Chen, and H.-S. Kao, "ESD protection design for 900-MHz RF receiver with 8-kV HBM ESD robustness," in *Proc. IEEE Radio Freq. Integr. Circuit Symp.*, 2002, pp. 427–430.
[6] M.-D. Ker, T.-Y. Chen, and C.-Y. Chang, "ESD protection for CMOS RF integrated circuits," in *Proc. EOS/ESD Symp.*, 2001, pp. 346–354.
[7] S. Dabral, R. Aslett, and T. Maloney, "Designing on-chip power supply coupling diodes for ESD protection and noise immunity," in *Proc. EOS/ESD Symp.*, 1993, pp. 239–249.
[8] T. Maloney and S. Dabral, "Novel clamp circuits for IC power supply protection," in *Proc. EOS/ESD Symp.*, 1995, pp. 1–12.
[9] M.-D. Ker and W.-Y. Lo, "Design on the low-leakage diode string for using in the power-rail ESD clamp circuits in 0.35-μm silicided CMOS process," *IEEE J. Solid-State Circuits*, vol. 35, no. 4, pp. 601–611, Apr. 2000.
[10] S.-S. Chen, T.-Y. Chen, T.-H. Tang, J.-L. Su, T.-M. Shen, and J.-K. Chen, "Low-leakage diode string designs using triple-well technologies for RF-ESD applications," *IEEE Electron Device Lett.*, vol. 24, no. 9, pp. 595–597, Sep. 2003.
[11] S.-S. Chen, T.-Y. Chen, T.-H. Tang, J.-K. Chen, and C.-H. Chou, "Characteristics of low-leakage deep-trench diode for ESD protection design in 0.18-μm SiGe BiCMOS process," *IEEE Trans. Electron Devices*, vol. 50, no. 7, pp. 1683–1689, Jul. 2003.
[12] S. Voldman, "Variable-trigger voltage ESD power clamps for mixed voltage applications using a 120 GHz/100 GHz (f_T/f_{MAX}) silicon germanium heterojunction bipolar transistor with carbon incorporation," in *Proc. EOS/ESD Symp.*, 2002, pp. 52–61.
[13] S. Voldman, G. Gerosa, V. Gross, N. Dickson, S. Furkay, and J. Slinkman, "Analysis of snubber-clamped diode-string mixed voltage interface ESD protection network for advanced microprocessors," in *Proc. EOS/ESD Symp.*, 1995, pp. 43–61.
[14] M.-D. Ker and W.-L. Wu, "ESD protection design with the low-leakage-current diode string for RF circuits in BiCMOS SiGe process," in *Proc. EOS/ESD Symp.*, 2005, pp. 18–24.
[15] P. Gray, P. Hurst, S. Lewis, and R. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York: Wiley, 2001.
[16] S. Voldman and E. Gebreselasie, "Low-voltage diode-configured SiGe:C HBT triggered ESD power clamps using a raised extrinsic base 200/285 GHz (fT/fMAX) SiGe:C HBT device ESD protection for CMOS RF integrated circuits," in *Proc. EOS/ESD Symp.*, 2004, pp. 57–66.
[17] P. Ashburn, *SiGe Heterojunction Bipolar Transistors*. New York: Wiley, 2003.

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