Analysis of Poly-Si TFT Degradation Under Gate Pulse Stress Using the Slicing Model

Ya-Hsiang Tai, Shih-Che Huang, and Chien-Kwen Chen

***Abstract*—The device degradation of polycrystalline-silicon thin-film transistors stressed with different gate pulse waveforms is investigated. It is first observed that the degradation is dependent on the rising time of the gate pulses for the gate voltage swing below the threshold voltage. The degradation ratio of the mobility is analyzed with respect to two factors, namely, the magnitude of the lateral transient electric field and the change in the numbers of the carrier near the edges of the channel. A new index considering these two factors is proposed to depict the device degradation. It shows good linearity between the degradation in mobility and the proposed index.**

***Index Terms*—AC stress, dynamic stress, poly-Si thin-film transistors (TFTs), reliability.**

I. Introduction

POLYCRYSTALLINE-SILICON (poly-Si) thin-film transistors (TFTs) have been widely used in active-matrix displays [1]. The higher mobility of poly-Si TFTs allows the fabrication of the pixel array and peripheral circuits on the same glass substrate. TFTs in driver circuits, unlike those in the pixels, are subjected to high-frequency voltage pulses [2], [3]. Therefore, the degradation mechanism under dynamic operation should be understood in detail. However, the studies about ac stress of the poly-Si TFTs are very few. In this letter, correlations between experiments and simulation results were made to evaluate the degradation of poly-Si TFTs under ac stress.

II. Experiments

Top-gate n-type poly-Si TFTs with lightly doped drain (LDD) were used in this letter. First, the buffer oxide and a-Si:H film with a thickness of 50 nm were deposited on glass substrates with plasma enhanced chemical vapor deposition (PECVD). The samples were then put in the oven for dehydrogenation. The XeCl excimer laser with a wavelength of 308 nm and energy density of 400 mJ/cm^2 was applied. The laser scanned the a-Si:H film with the beam width of 4 mm and 98% overlap to recrystallize the a-Si:H film to poly-Si. The average grain size of the poly-Si film is about 0.5 μm. After poly-Si active area definition, 80-nm SiO_2 and 40-nm SiN_x was deposited with PECVD as the gate insulator. Next, the metal gate was formed by sputter and then defined. The LDD and the n^+ source/drain doping were formed by PH_3 implantation with a dosage of 2×10^{13} cm^{-2} and 2×10^{15} cm^{-2} of PH_3, respectively. The LDD implantation was self-aligned, and the n^+ regions were defined with a separate mask. Then, the interlayer of SiN_x was deposited. Subsequently, the rapid thermal annealing was conducted to activate the dopants. Meanwhile, the poly-Si film was hydrogenated. Finally, contact hole formation and metallization were performed to complete the fabrication work. The typical values of the threshold voltage and the mobility of the samples are 1.68 V and 77.8 cm^2/V $\cdot$ s. In this letter, the TFTs having a channel width of 20 μm and a channel length of 5 μm with an LDD structure length of 1.2 μm are stressed and measured.

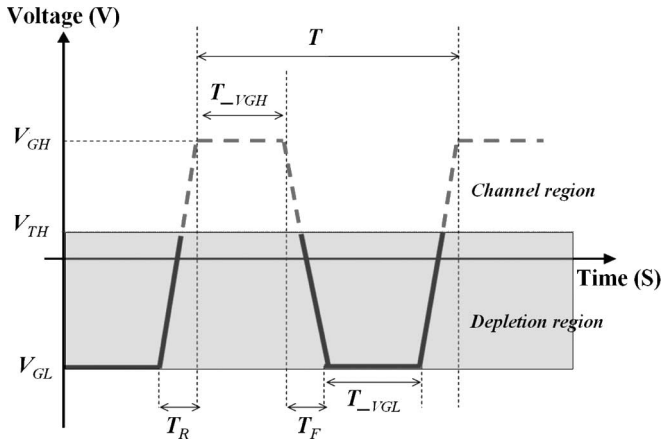

Fig. 1. Waveform of the ac signal applied to the gate electrode of the TFTs, where $V_{\rm GH}$, $V_{\rm GL}$, $V_{\rm TH}$, T, $T_{\rm \_VGH}$, $T_{\rm \_VGL}$, T_R, and T_F are, respectively, the high and low voltages of the pulse, the threshold voltage of the TFT, the period of the pulse, the duration of the high and low voltages, and the rising time and falling time of the gate pluses.

Waveform of the ac signal applied to the gate electrode of TFTs is shown in Fig. 1. Pulses with high-voltage $V_{\rm GH}$ of 15 and 0 V, low-voltage $V_{\rm GL}$ of 0 and -15 V, and period T of about 2–3 μs were applied to the gate electrode. The source and drain were grounded to avoid the dc effect [4].

III. Result and Discussion

The rising and falling time dependences for the mobility degradation of the device after dynamic stress are shown in Fig. 2(a) and (b), respectively. The mobility degradation is

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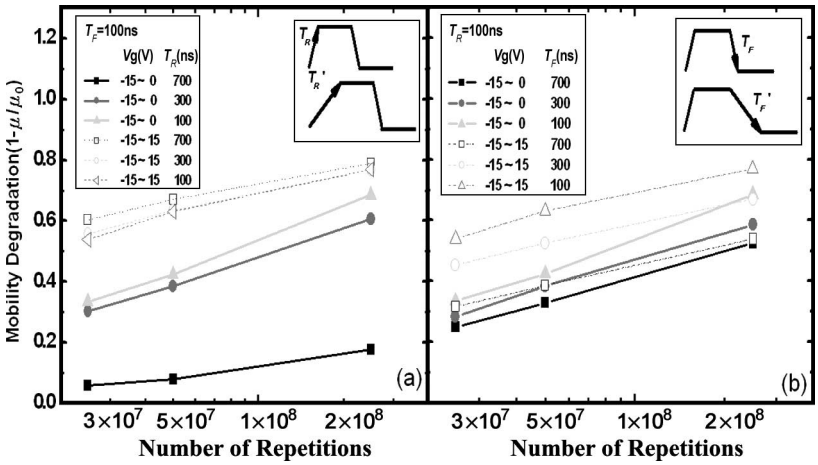

Fig. 2. Mobility degradation versus the number of repetitions of the gate pulses for: (a) different rising time T_R for a fixed T_F and (b) different falling time T_F for a fixed T_R, with the gate voltage swing from -15 to 15 V (dash lines) and -15 to 0 V (solid lines).

defined as $(1-\mu/\mu_0)$, where μ_0 and μ are the field-effect mobility derived from the maximum transconductance at the drain voltage of 0.1 V before and after stress. For the gate voltage swing from -15 to 15 V, the rising time T_R exhibits no significant effect on the degradation, as shown in the dash lines in Fig. 2(a). On the other hand, the mobility degradation depends strongly on the falling time T_F, as shown in the dash lines in Fig. 2(b). The shorter T_F the gate pulse applied, the worse degradation the device would suffer. A previous reported model claimed that, as the gate voltage swung from the ON region to the OFF region, the induced electrons in the channel would rush to the source and drain regions [5]–[7]. At this time, there would be some trapped electrons, and they are exposed to the high electric field. For shorter pulse fall times, more electrons are exposed to the high electric field and become hot carriers [7].

However, for the gate voltage swings from -15 to 0 V, it is first observed that the degradation is obviously dependent on both the rising time and falling time, as shown by the solid lines in Fig. 2(a) and (b). Since there are no induced electrons for these applied gate voltages, it reveals that the previously proposed model may be incomplete.

In order to universally describe the aforementioned phenomena, two factors are taken into consideration, that is, the transient electric field in the lateral direction and the changes in the number of the channel electrons under the lateral voltage difference. To understand the transient fields and charge distributions in the channel, a slicing method is used on the device for simulation. A whole TFT is sliced into many shorter ones in series, as shown in the inset of Fig. 3. In this letter, the original TFT with a channel length of 5 μm is sliced into ten TFTs in series, with a channel length of 0.5 μm. The ten TFTs are of the same model, and the model parameters of the sliced TFTs are carefully adjusted such that the simulated transfer characteristics of the sliced devices are very similar to that of the original unstressed device. Using a commercially available circuit simulator SPECTRE, the transient voltage distribution of different nodes under dynamic stress can be calculated. The voltage difference between the edge node and the grounded source/drain of the sliced TFT V_e is found to be the largest for all stages of the applied gate voltage. Referring to the previous report, the emission image of the TFT under dynamic stress indicates that the degradation is the worst at the edges of the channel [7]. It also accords with the simulation results that V_e is the largest voltage difference than the voltage differences for other nodes in the channel. Therefore, in the following discussion, only the voltage difference V_e is taken into consideration.

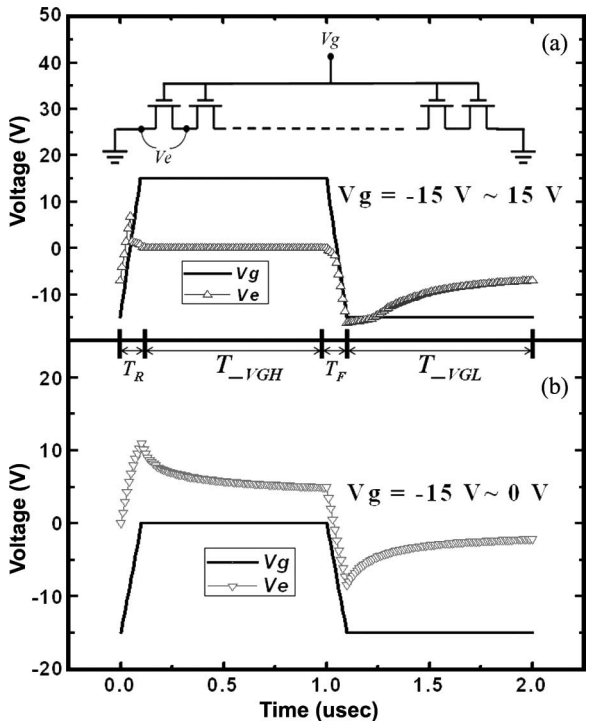

Fig. 3. Lateral voltage difference V_e for: (a) $V_g = -15 \sim 15$ V and (b) $V_g = -15 \sim 0$ V, respectively, wherein V_g is the applied gate voltage and V_e is the voltage difference of the sliced TFT at the edge.

For V_g swinging from -15 to 15 V, the simulation result of V_e is shown in Fig. 3(a). The operation of TFT can roughly be separated into the channel and the depletion regions by threshold voltage $V_{\rm TH}$, as shown in Fig. 1. When V_g rises in the depletion region, V_e follows the change of V_g owing to coupling effect, reflecting the scarce change in the channel

carrier number. As the gate voltage goes above $V_{\rm TH}$, the channel is formed, and V_e is quickly discharged to zero, such that the lateral field is too low to speed up the carriers. Therefore, although for different T_R the coupling effect would lead to the different V_e in the channel, once the gate voltage goes above $V_{\rm TH}$, the voltage in the channel would be quickly discharged regardless of the value of T_R. Hence, the mobility degradation is independent of T_R. For the period of gate voltage above $V_{\rm TH}$, the channel is of low resistance, and thus, V_e remains zero. As the gate voltage falls to the depletion region, V_e is coupled to a large negative value by V_g. The negative V_e is then slowly charged toward the ground during $T\_{\rm VGL}$. The lateral voltage difference at the TFT edge may be so high that the carriers can gain energy to become hot carriers, resulting in the mobility degradation. The coupling magnitude of this transient electrical field becomes larger with shorter T_F, resulting in the T_F dependence of the mobility degradation.

On the other hand, for the gate voltage swinging from -15 to 0 V, since the gate voltage is all below $V_{\rm TH}$, TFT is always in the depletion region. Consequently, as the gate voltage swings for both rise and fall, V_e is coupled by V_G, as shown in Fig. 3(b). Because the gate voltage is always below $V_{\rm TH}$ and the channel voltage cannot be quickly discharged, this coupled V_e would be discharged slowly during $T\_{\rm VGH}$ and $T\_{\rm VGL}$, such that carriers may obtain high energy and cause the device degradation. Since the coupled magnitude of V_e is concerned with the changing speed of V_g, the mobility degradation is accordingly dependent on T_R and T_F.

The aforementioned discussion takes two factors into consideration: the transient lateral electrical field at the edge of the sliced TFT V_e and the current flow through the edge of the sliced TFT under the voltage difference V_e. In order to describe the degree of the degradation, a new index Π calculated from the simulation result is further introduced, which is given as

$$\Pi = \sum \frac{1}{\rm Ti} \int_{\rm Ti} V_e \bullet \left[\frac{\rm Cox \bullet d(V_g - V_e)}{dt} \right] \bullet dt$$

where Ti corresponds to T_R, T_F, $T\_{\rm VGH}$, and $T\_{\rm VGL}$, and Cox is the gate capacitance per unit area. This index accounts for two factors mentioned above. The term $\rm Cox^* d(V_g - V_e)/dt$ represents the displacement current of the capacitor. Because the devices are fabricated on the glass substrate, the current could not flow to the bulk electrode and may only therefore flow to the source/drain region, becoming the lateral current along the channel. For T_R and T_F in the depletion region, V_e follows the change of V_g; thus, $V_g - V_e$ is kept constant, and its time differentiation is zero. Therefore, in the time $T\_{\rm VGH}$ and $T\_{\rm VGL}$, the coupling magnitude of V_e and its duration dominate the value of Π. The mobility degradation $(1 - \mu/\mu_0)$ versus the index Π under different ac stress conditions are plotted in Fig. 4. The fair linearity exhibits the validity of the proposed mechanism.

IV. Conclusion

For ac stress with the gate voltage toggling between -15 and 15 V, it is observed that the degradation depends on the falling time T_F of the gate pulse but does not depend on the rise time T_R. However, for the gate voltage swinging from -15 to 0 V, it is observed that the degradation is both influenced by T_R and T_F. A slicing method is used for the simulation of channel voltage distribution and charge change at the edge to explain the degradation behaviors. A new index Π is introduced to estimate the degree of the degradation. The mobility degradation and the index Π show linear dependence universally for various gate pulse stress conditions. The linear dependence gives the index Π a potential modeling for reliability simulation and lifetime prediction of poly-Si TFT circuitry.

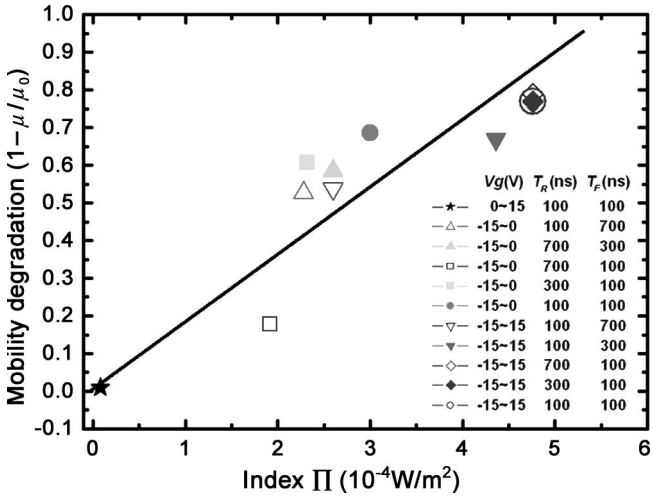

Fig. 4. Mobility degradation $(1 - \mu/\mu_0)$ versus the proposed index Π.

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