Study on electrical degradation of p-type low-temperature polycrystalline silicon thin film transistors with $C-V$ measurement analysis

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Abstract

Laser recrystallized low-temperature poly-silicon (LTPS) films have attracted attention for their application in thin-film transistors (TFTs), which are widely used in active matrix display. However, the degradation behavior of p-type LTPS TFTs is not quite clarified yet. In this paper, the instability mechanisms of p-channel LTPS TFTs under DC bias stress have been investigated. From the IV transfer curves, it was observed that LTPS TFT's mobility increases after stress at some bias conditions. This degradation is most likely caused by interface traps between the poly-Si thin film and the gate insulator, as well as the damaged junction of the drain from stress. In this work, the assumption is examined via $C-V$ measurement. It is found that the C_{GD} curves of the stressed TFT slightly increase for the gate voltage smaller than the flat band voltage V_{FB}. However, the C_{GS} curves of the stressed device are almost the same as those before stress. By employing simulation, it is found that the degradation of p-type TFTs under this stress condition is mainly caused by the trapped charges at the interface between the gate and the drain region, which is generated by the high voltage difference applied during DC bias stress.
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1. Introduction

Low-temperature poly-Si (LTPS) thin film transistors (TFTs) have attracted much attention for AMLCD and AMOLED applications due to their high mobility and the capability of realizing integrated circuits on glass [1]. The reliability issues of the LTPS TFTs are of special importance in practical application. It was reported that poly-Si TFTs suffer from several degradation mechanisms, such as hot carrier effects [2–4], self-heating effects [5,6], water [7], and photon-induced leakage current [8,9]. For the reliability issues mentioned above, most of the previous works focused on the current transfer characteristics to investigate the mechanism of degradation after DC stress. Since the $I-V$ transfer curves show the overall behavior of the channel, it would be difficult to identify the degradation mechanism as well as the location of the damaged regions in the device. In this work, the DC bias tests were performed and the stressed TFT were examined with $C-V$ (capacitance–voltage) measurement. The capacitance C_{GS} between the source and the gate, as well as the capacitance C_{GD} between the drain and the gate, can be measured. The difference between C_{GS} and C_{GD} can reveal the locations of the damaged regions [10]. Besides, the frequency dependence of the $C-V$ curves help to identify whether the dominant mechanism of degradation is the increase of fixed charges or trap states.

2. Experiments

The process flow of TFTs is described below. First of all, the buffer oxide and a-Si:H film with thickness of 50 nm were deposited on glass substrates with PECVD. The samples were then put in the oven for dehydrogenation. The XeCl excimer laser of wavelength 308 nm and energy density of 400 mJ/cm^2 was applied. The laser scanned the a-Si:H film with a beam width of 4 mm and 98% overlap to recrystallize the a-Si:H film to poly-Si. After poly-Si active area definition, 100 nm SiO$_2$ was deposited with PECVD as the gate insulator. Next, the metal gate was formed by sputter and then defined. The p$^+$ source/drain doping was done by B$_2$H$_6$ self-align implantation with a dosage of 2×10^{15} cm^{-2}. Then, the interlayer of SiN$_x$ was deposited. Subsequently, the rapid thermal annealing was

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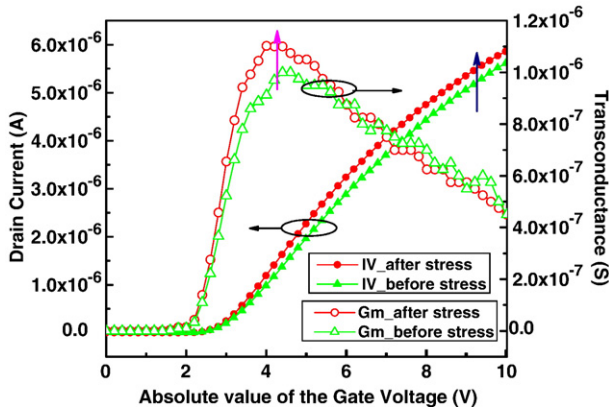*E-mail address:* hansley.eo92g@nctu.edu.tw (S.-C. Huang).

Fig. 1. I_d–V_g and transconductance curves before and after DC stress condition of V_g=−2 V and V_d=−20 V.

conducted to activate the dopants. Meanwhile, the poly-Si film was hydrogenated. Finally, the contact hole formation and metallization were performed to complete the fabrication work.

The Agilent 4156A semiconductor parameter analyzer was used to measure the I–V curve and stress the device at different conditions. The C–V curves of the gate-to-source capacitance (C_{GS}) and gate-to-drain capacitance (C_{GD}) before and after stress at different frequencies were measured with the Agilent 4284A precision LCR meter.

3. Results and discussion

In this study, the p-type TFTs with a channel width of 20 μm and a channel length of 5 μm were fabricated. These devices
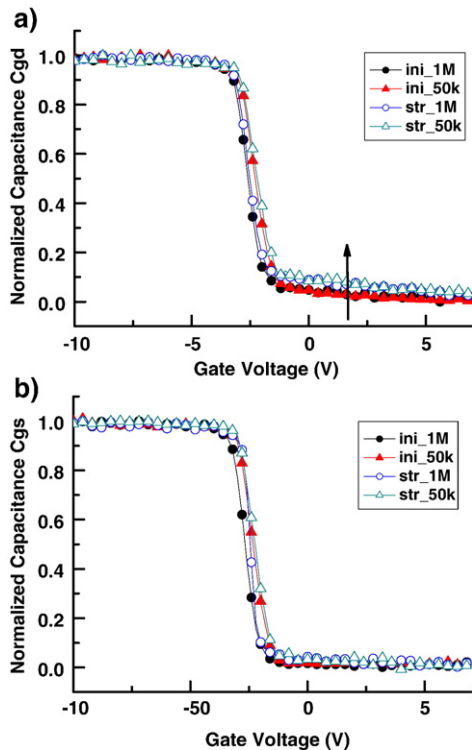

Fig. 2. (a) and (b). Normalized C_{gd} and C_{gs} curves (before and after DC stress) versus gate voltage at frequencies 50 K and 1 MHz.
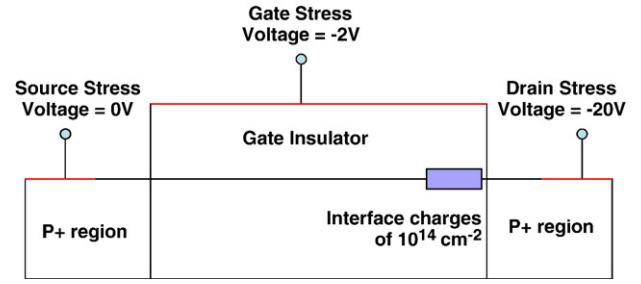

Fig. 3. The proposed degradation model in the TFT structure with interface charges.

were stressed at various conditions of the gate-to-source voltage V_{gs} and the drain-to-source voltage V_{ds} in the range of 0 V to −20 V. For most conditions, the threshold voltage V_{th} shifts negatively and the mobility degrades. These results are well explained in previous reports [11–13]. However, for certain conditions, especially that of V_{gs}=−2 V and V_{ds}=−20 V, the increase of TFT's mobility can be observed.

Fig. 1 shows the curves of the I–V transfer and transconductance Gm of the p-type poly-Si TFT before and after this particular stress condition. After stress, the on current shows a slight increase and a very small change in the threshold voltage and the subthreshold swing. However, the changes of the Gm curve are more obvious since the transconductance represents the derivative of the drain current via gate voltage. As shown in Fig. 1, Gm reaches its maximum at the gate voltage of −4 V and the maximum value increases about 15% compared to that before stress. For the gate voltage between −4 V and −10 V, the Gm curve of the stressed device also decreases more rapidly than that of the unstressed device.

Since the I–V transfer curves show the entire characteristics of the whole channel and may not distinguish the dominant mechanism, C–V measurements were further employed to investigate the asymmetry electric fields at the source and drain of TFTs during the stress. Fig. 2(a) shows the gate-to-drain capacitance C_{GD} curves before and after stress at different frequencies, while Fig. 2(b) shows the corresponding curves of the gate-to-source capacitance C_{GS}. The C_{GD} curves were measured with a floating source and C_{GS} curves were measured with a floating drain. The C–V curves were plotted with normalized value of capacitances, which is the ratio of the measured value to the maximum value of the measured capacitance.
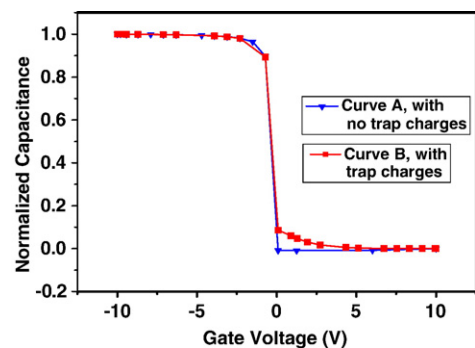

Fig. 4. Simulation results of the normalized C–V curves with and without

Observed from Fig. 2, all curves remain at unity and show no obvious differences when the gate voltage is larger than the flat band voltage V_{FB}, and fall sharply to almost zero around the flat band voltage V_{FB}. However, the C_{GD} curve increases slightly when the gate voltage is smaller than the V_{FB} while in this region the C_{GS} curve almost remains the same. The extra increase for the lower gate voltage of C_{GD} curve may be attributed to the interface trapped charges, which may be caused by the high voltage difference between the gate and the drain during the stress.

As shown in Fig. 2, in the case of p-type TFTs, the C–V curves shift in the negative direction for the gate voltage about V_{FB}, which may be attributed to the increase of the trap states inside the poly-Si thin film [14,15]. Different from that of n-type TFTs, the increase in C_{GD} of p-type TFTs for the gate voltage smaller than V_{FB} are almost independent of frequency. It reveals whether the dominant degradation mechanism is trap states or fixed traps, since the trap states generated by the DC stress respond to the small signal while the fixed trap charges are not affected by the applied frequencies [16]. The hot electrons in the n-type TFTs are more easily generated than the hot holes in the p-type TFTs. Thus, unlike the n-type TFTs, the dominant instability mechanism for the p-type TFTs would be the trapped charges induced by electric filed, instead of the trap states generated by the hot carrier.

For the gate voltage of −2 V, which is much higher than the drain voltage of −20 V during the stress, electrons would be attracted by the gate and trapped at the interface between the oxide and the poly-Si film near the drain region. These trapped electrons at the interface would attract more free holes near the drain region at the gate voltage above V_{th}. Since more holes would be induced, the Gm for the gate voltage around the threshold voltage will be larger than that before stress, which implies the increase in mobility when the TFT begins to turn on. This mobility increase is also consistent with the reduction of the effective channel length due to electron trapping [17].

As for the overall channel of the TFTs, it is believed that the interface states are not created since the subthreshold swing and the threshold voltage did not changed. The C–V measurement results further support the creation of the trap charges on the surface near drain. The increase of C_{GD} for the gate voltage below V_{FB} indicates the increase of carriers which is induced by the trapped electrons near drain [18]. However, C_{GS} does not change after stress because the charge trapping does not occur at the low stress field near the source.

In order to verify the effects of the trap charges in the damaged region near the drain, a two-dimensional (2-D) numerical simulation program DESSIS was used to simulate the device characteristics. The model of the cross section of the device after DC stress is shown in Fig. 3. In the simulation, the grain boundaries inside the poly-Si film are accounted by using the "effective medium approach," which treats the poly-Si film as a uniform material with the density of localized states in the forbidden gap. In this simulation, the maximum interface charges of 1×10^{14} cm^{-2} are arranged near the drain edge, which is the influence of voltage difference between the gate and drain. Fig. 4 shows the simulation results with and without

degraded regions in the device. Curve A is the C–V curve with no degraded region, while curve B is the one with interface charges near the drain region. Comparing to curve A, curve B increases slightly for the gate voltage below V_{FB}. It reveals that the interface charges between the drain and the gate influence the number of induced carriers in channel depletion and weak inversion conditions.

It was reported that the activation energy of electron to inject into the gate oxide is about 3.2 eV and that of hole is about 4.3 eV [18], which means that the probability of electron trapping is larger than hole trapping. The trapped electrons lead to the degradation of p-type TFT due to the high voltage difference between the gate and the drain. On the other hand, the hot holes are few such that the states created in the p-type TFT are much less than that in the n-type TFT. This reflects that the degradation mechanisms are quite different between the n-type and p-type TFTs and more researches may be required to clarify the comparison and the detailed mechanisms for these two operation methods.

4. Conclusions

In this work, the degradation of p-type poly-Si TFTs under DC stress was examined via C–V measurement. It was found that TFT's mobility increases after the stress of $V_g = -2$ V and $V_d = -20$ V. The C–V measurements of the LTPS TFTs before and after stress verify the mechanism and location of degradation by analyzing the difference between C_{GS} and C_{GD}. The slight increase in C_{GD} at the gate voltage smaller than V_{FB} indicates that the degradation is located near the drain, which is attributed to the high voltage difference between the gate and the drain. Device simulation further confirmed that the dominant degradation mechanism of p-type TFT is the trapped charges at the interface near the drain region.

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