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High-performance polycrystalline silicon thin-film transistors with oxide–nitride–oxide gate dielectric and multiple nanowire channels

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Abstract

This work presents a method to enhance the performance of polycrystalline silicon thin film transistors (poly-Si TFTs) by using an oxide–nitride–oxide (ONO) gate dielectric and the multiple nanowire channels structure. Experimental results indicate that the performance of the device was enhanced by using the ONO multilayer, because the ONO gate dielectric constant is increased compared to the conventional oxide gate dielectric. Additionally, the TFTs with a ten nanowire channel structure (NW-TFTs) have superior electrical characteristics compared to other TFTs. This is because a structure with more corners and a shorter radius has better gate control due to the corner effect.
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Keywords: Poly-Si TFTs; Oxide–nitride–oxide; Nanowire

1. Introduction

Polysilicon thin film transistors (poly-Si TFTs) have drawn attention for their application on active-matrix liquid-crystal-displays (AMLCDs) due to their high field effect mobility and driving current. The poly-Si TFTs are promising for integration with peripheral driving circuits on low-cost glass substrates [1,2]. In addition, poly-Si TFTs have the potential to be used in three-dimensional (3D) circuits, including vertically integrated SRAMs [3] and DRAMs [4]. However, the improvement of electrical characteristics and the reduction of undesirable effects are still important issues. It was reported that using a high dielectric constant material as gate insulator can improve the device performance [5]. However, using a high dielectric constant material, such as silicon nitride creates a poor interface between the nitride/poly-Si layers that degrades the device performance. The first report of an oxide–nitride–oxide (ONO) multilayer used as an alternative dielectric for a DRAM cell capacitor was in 1984 [6]. In 1995, poly-Si TFTs with a high dielectric constant ONO multilayer as a gate insulator was reported [7]. In the ONO multilayer, a nitride layer is used to increase the effective dielectric constant and the other oxide layers are used to provide electrical contact in the SiO_2/poly-Si interface. Recently, poly-Si TFTs with a multiple nanowire channels structure was reported to improve the poly-Si TFTs performance [8,9].

In this paper, we combined the ONO gate dielectric with a series of multiple channel structures on poly-Si TFTs to study the effects on device performance. Also, standard TFTs with the same thickness of oxide dielectric were fabricated for comparison. Experimental results show that the electrical characteristic of ONO–TFTs were enhanced, compared to standard TFTs. In addition, the electrical characteristics are highly dependent on channel width dimensions. The ONO–TFT with nanowire channels shows the best performance.

2. Experimental procedure

In this work, a series of TFTs with an oxide–nitride–oxide (ONO) gate dielectric and different structure TFTs with a gate

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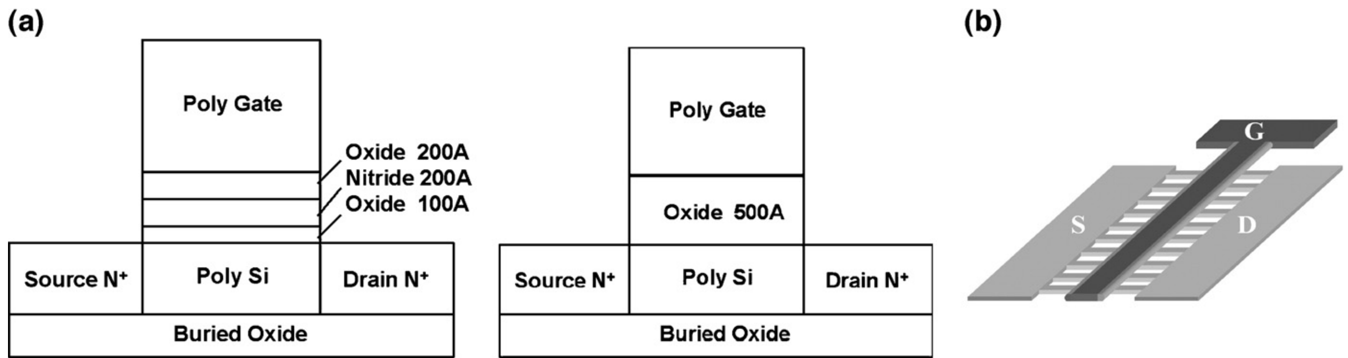

Fig. 1. (a) Schematic plots of TFT with oxide–nitride–oxide (ONO) and oxide gate dielectric, (b) Top view of the device with the NW structure.

length of 5 μm, one set with ten strips of multiple 65 nm nanowire (NW) TFT, a second set with five strips of multiple 0.2 μm channels (M5) TFT, a third set with two strips of multiple 0.5 μm channels (M2) TFT and a set with a single-channel (S1) TFT with 1 μm, were fabricated. Standard TFTs with an oxide dielectric were also prepared as the control samples for comparison. Fig. 1a presents the schematic plots of TFT with an oxide–nitride–oxide (ONO) and an oxide gate dielectric. The top view of device with the NW structure is shown in Fig. 1b.

In the first fabrication process, a 50 nm-thick undoped amorphous silicon (a-Si) layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C on oxidized silicon wafers. The deposited a-Si layer was then recrystallized by solid-phase crystallization (SPC) at 600 °C for 24 h in nitrogen ambience. Then the device active region was patterned by electron beam lithography (EBL) and transferred by reactive ion etching (RIE). After the active region patterning, a 50 nm-thick ONO multilayer gate dielectric with a bottom tetra-ethyl-*ortho*-silicate (TEOS) oxide (10 nm)/silicon nitride (20 nm)/top TEOS oxide (20 nm) (Fig. 1b) was deposited by LPCVD. In the standard TFT, a single layer of 50 nm-thick TEOS oxide was deposited. Then a 150 nm-thick in-situ n^+ doped poly-Si layer was deposited and transferred to a gate electrode by EBL and RIE. After gate patterning, self-aligned phosphorous implantation was performed with a dose of 5×10^{15} cm^{-2}, then the dopant was activated by rapid thermal annealing at 1000 °C. After source and drain implantation, a 200 nm-thick TEOS oxide layer was deposited as the passivation layer by LPCVD. Next, contact holes were defined and Al metallization was performed. Finally, all devices were sintered at 400 °C in nitrogen ambience for 30 min.

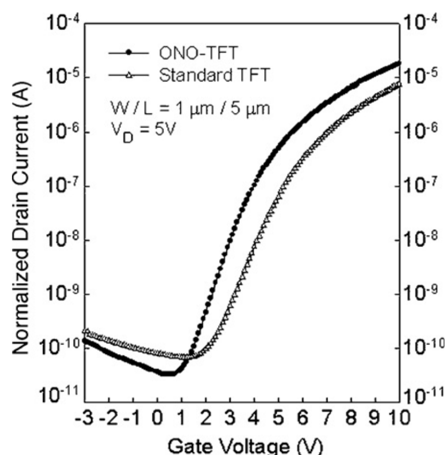

Fig. 2. Typical I_D–V_G transfer characteristics of standard poly-Si TFT with TEOS oxide gate dielectric and the proposed TFT (ONO–TFT) with ONO stack gate dielectric.

3. Results and discussions

Fig. 2 shows the typical I_D–V_G transfer characteristics of a standard poly-Si TFT with a TEOS oxide gate dielectric and the proposed TFT (ONO–TFT) with an ONO stack gate dielectric.

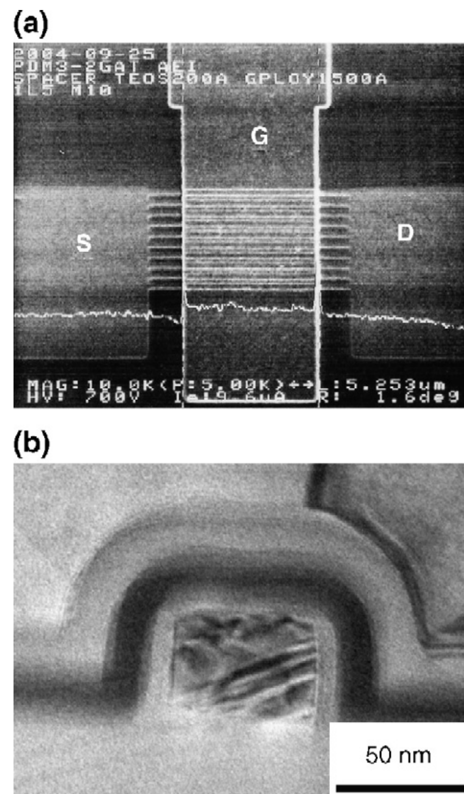

Fig. 3. (a) Scanning electron microscopy (SEM) photography of device with the NW structure, (b) Transmission electron microscopy of one of the channels in the ONO–TFT with the NW structure.

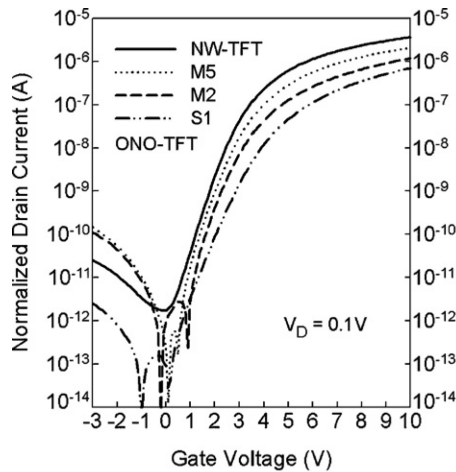

Fig. 4. Transfer I_D–V_G curves of the proposed all ONO–TFTs with various numbers of channels with different widths.

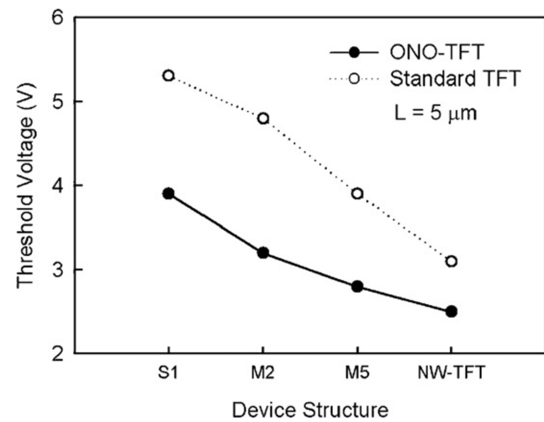

Fig. 6. Threshold voltage (V_{th}) of the ONO–TFTs and standard TFTs versus the multi-channel with different widths.

The standard TFT has a maximum on-current of 7.5 μA, a minimum leakage current of 68 pA and an ON/OFF ratio of 1×10^5. The ONO–TFT has a maximum on-current of 17.4 μA, a minimum leakage current of 33 pA and the current ratio of 5×10^5. It also has a smaller threshold voltage and subthreshold swing (SS) than the standard TFT. The enhanced electrical characteristics of the ONO–TFT are attributable mainly to the increase in the effective gate dielectric constant. The calculated total gate capacitance, which is the parallel multilayer capacitance yields an estimate of the effective gate dielectric constant of 5.1. The accumulation of N atoms at the SiO_2/poly-Si interface and their bonding with an active poly-Si layer reduces the interface trap density [10].

In this experiment, not only was the effective gate dielectric constant increased using an ONO multilayer, but also TFTs with multiple channels were adapted to improve electric performance. Four structures S1, M2, M5 and NW were fabricated and compared. Fig. 3a shows an SEM micrograph of device with NW structure, including the gate, source, drain and ten multiple nanowire channels. Fig. 3b presents a TEM micrograph of one of the channels of an ONO–TFT with the NW structure. The physical width of each channel was confirmed to be 65 nm.

Fig. 4 plots the transfer I_D–V_G curves of all tested ONO–TFTs with various numbers of channel and different widths. Clearly, the device with the NW structure has the highest drain current, the smallest threshold voltage and steepest subthreshold slope of all TFTs.

Fig. 5 plots the maximum normalized drain current of the ONO–TFTs and the standard TFTs versus the different structures at V_D=5 V. The current of the ONO–TFTs increases from 1.7×10^{-5} A to 1.1×10^{-4} A and while that of the standard TFTs increases from 7.5×10^{-6} A to 7.7×10^{-5} A in order from the S1 structure to the NW structure. The corner effect of the devices is the main cause of the improvement in electrical performance. The crowding of the gate fringing field at the corner edges causes the electrical field at the corners to exceed that at the surface of the channel. The larger electrical field and better gate control across the corner increase the carrier density, as discussed in previous work [11]. The corner effect becomes significant as the channel number increases and channel width decreases. Therefore, the pronounced enhancement of device with the NW structure is attributed to the large number of corners and their corner effect.

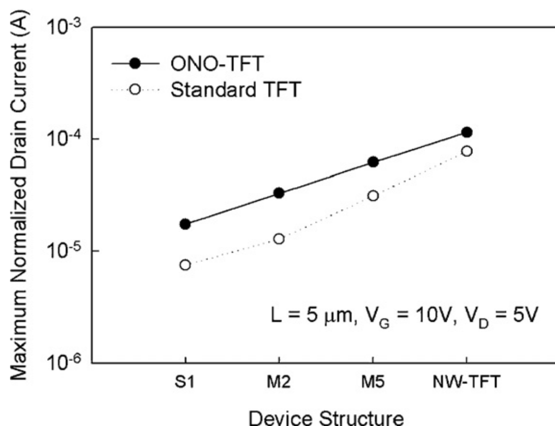

Fig. 5. Maximum normalized drain current of the ONO–TFTs and the standard TFTs versus the different structures at V_D=5 V.

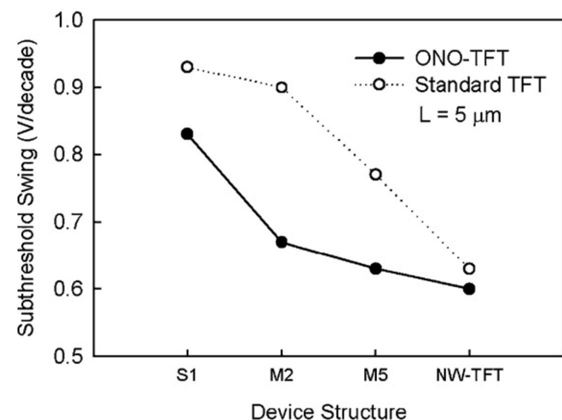

Fig. 7. Subthreshold swing (SS) of the ONO–TFTs and standard TFTs versus the multi-channel with different widths.

Fig. 6 shows the threshold voltage (V_{th}) of the ONO–TFTs and standard TFTs versus the multiple channels with different widths. The V_{th} is defined as the normalized drain current at 10 nA for V_D = 0.1 V. The V_{th} of the ONO–TFT decreases from 3.9 V to 2.5 V and that of the standard TFT decreases from 5.3 V to 3.1 V in order from the S1 structure to the NW structure. The improvement of V_{th} is attributable mainly to the corner effect. The drain current at the corner region turns on earlier than that at the surface of the channel [12]. The additional corner current can increase the drain current. Hence, the V_{th} was reduced according to the constant current definition. In Fig. 6, the V_{th} of the device is reduced as the number of corners increases from the S1 structure to the NW structure. Because devices with the NW structure have the most corners, the ONO–TFT and the standard TFT with this structure have the lowest threshold voltages.

Fig. 7 presents the subthreshold swing (SS) of the ONO–TFTs and standard TFTs versus multiple channels with different widths. The SS is defined as the gate voltage required to increase the drain current by one order of magnitude. The SS of the ONO–TFT is reduced from 0.83 V/decade to 0.6 V/decade and that of the standard TFT is reduced from 0.93 V/decade to 0.63 V/decade in order from the S1 structure to the NW structure. In the subthreshold region, the corner effect can enhance the subthreshold current by increasing the induced electron density at the corner region [13]. Therefore, the SS is decreased as the number of corners increases in order from the S1 structure to the NW structure. Additionally, the current at the corner region is related to its radius, so a device with the smaller radius has a larger corner current. The simulated currents of the devices at a corner with different radii have been reported in [12]. The subthreshold swing of devices with NW structure in the ONO–TFT and the standard TFT are almost equal, showing that gate control is mainly dominated by the corner effect from the NW structure.

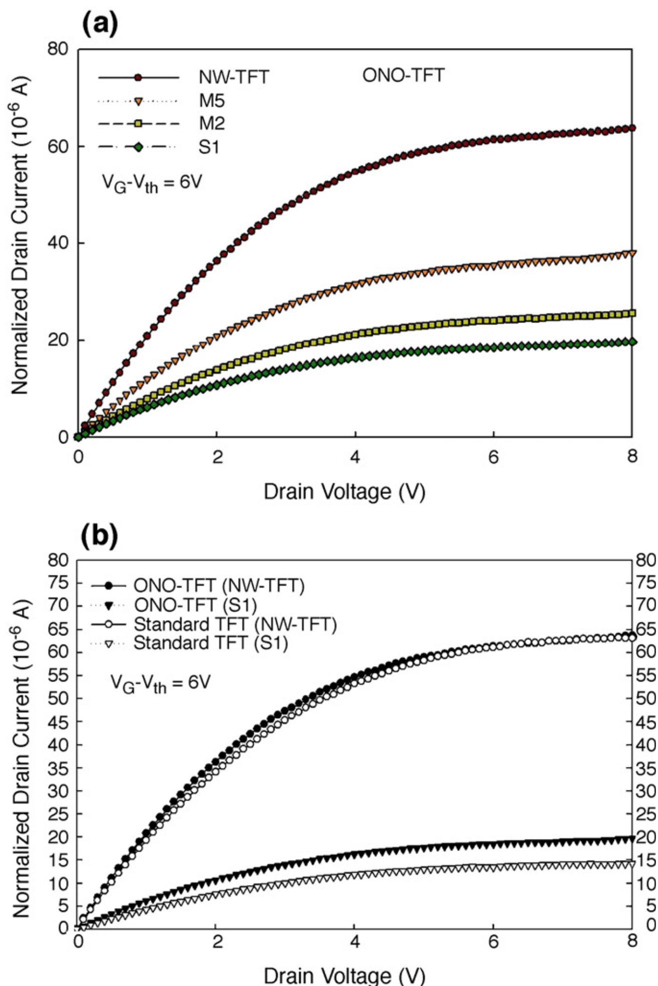

Fig. 8. (a) Output I_D–V_D curves of the ONO–TFTs versus the multi-channel with different widths at V_{GS}=6 V, (b) Output characteristics of the standard TFTs and ONO–TFT with the S1 and the NW structures.

Fig. 8a shows the output I_D–V_D curves of the ONO–TFTs versus multiple channels with different widths at V_{GS} = 6 V. The saturation drain current drastically increases from the S1 structure to the NW structure because of the corner effect. Fig. 8b shows the output characteristics of the standard TFTs and ONO–TFT with S1 and NW structures. For S1 TFT, the maximum drain output current of ONO–TFT is 1.35 times that of the standard TFT, with a gate dielectric constant ratio of K_{ONO}/K_{SiO_2} = 1.31. However, the current of devices with NW structure is almost equivalent in both the ONO–TFTs and standard TFTs without an improved gate dielectric constant ratio of K_{ONO}/K_{SiO_2}. This result again shows that the electrical performance of devices with NW structure is dominated by the corner effect.

4. Conclusion

This paper has proposed a high performance TFT with a nanowire structure and multilayer ONO gate dielectric. The proposed TFT with ONO gate dielectric has better electrical properties compared to the standard TFT with a TEOS oxide film. Furthermore, this study applied multiple channels structures to ONO–TFT and standard TFT to promote device performance. Experimental results show that the device performance is enhanced with an increasing number of channels, from S1, M2, M5 to NW structures, because the structure with more corners and smaller radii has the better gate control due to the corner effect. Therefore, the devices with NW structure exhibit superior electrical performance, including high current drivability, low threshold voltage, steep subthreshold slope and favorable output characteristics. The results also show that the characteristics of devices with a nanowire structure are almost the same when comparing the ONO–TFT and standard TFT. Hence devices with a nanowire structure are dominated by the corner effect. Such TFTs are thus very promising candidates for use in future high performance poly-Si TFT applications.

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