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A 10~18GHz Wide-band Transformer feedback LNA

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***Abstract*—A wide-band (10~18GHz) low noise amplifier(LNA) is presented . With transformer feedback in the traditional cascode amplifier, good input matching is achieved from 10 GHz to 18 GHz. The noise figure is below 3.5dB over 10-18GHz. There is no input-matching elements in the input gate of the cascode amplifier, so that the LNA can achieve lower NF. The LNA is designed based on CMOS TSMC 0.18μm mixed signal/RF process. With 1.8V supply voltage and three stage amplifiers to achieve wider gain bandwidth, the LNA can achieve input-matching of -12dB over the bandwidth; minimum NF 2.4dB; gain(S21) of 17dB and 1dB gain compression(P1dB) at -22.6dB. The power consumption is 37.6mW(exclude buffer)**

***Keywords*-low noise amplifier(LNA); transformer feedback; wide-band**

I. INTRODUCTION

Wide-band communication system (like UWB for 3.1 to 10GHz; 57 to 64GHz millimeter wave system) have received much attention due to high data rate and high speed communication. In such a wideband system, LNA is in the first stage after antenna in the front-end receiver block. To interface with the antenna and the preselect filter, LNA requires input match to 50Ω over the bandwidth. Meanwhile LNA must provide high gain and the most important, low noise.

Several typologies have been proposed for wideband input matching. (a)distributed amplifier[1]:distributed amplifier (DA) can achieve much wider input matching by several stages of amplifier. However, DA has gain problem due to long transmission line loss and consume more power and area. It is unsuitable for modern wideband system. (b) negative feedback amplifier[2]: negative feedback amplifier can achieve wideband matching due to parasitic capacitance. This configuration doesn't provide very high gain and may has stable problem. (c) common gate configuration: common gate configuration[3] has good linearity and wideband input matching. Due to the simplicity of common gate input-matching mechanism, it has low noise but smaller gain than common source amplifier. (d) filter configuration[4]: With inductors and capacitances in the input of degenerated common source amplifier, it forms a Chebyshev filter structure in the input. The input matching bandwidth is dependent on the order of Chebyshev filter. Therefore it can achieve wider input matching but the noise figure is degraded by the imperfect effect of inductors and capacitances.

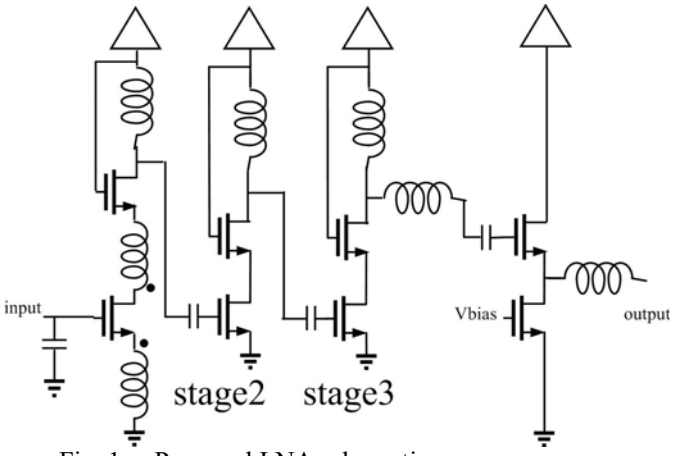

Fig. 1. Proposed LNA schematic

In this paper, a LNA designed in CMOS TSMC 0.18μm mixed signal/RF process is proposed. The LNA has no input tuning circuits for lower noise. Input matching is achieved due to parasitic capacitance(Cgd,Cgs) and transformer feedback. The design consideration is analyzed, followed by the post-simulation results and the conclusion.

II. CIRCUIT ANALYSIS

The architecture of proposed LNA is shown in Fig. 1.We cascade two stages (stage2 and stage3) to amplify signal, because 0.18μm mixed signal/RF process has poor gain above 10 GHz. The buffer achieves output matching to 50Ω for measurement. For input matching analysis, Z_A in Fig 2 can be approximated as a resistor R_A at high frequency. Looking into common gate transistor M2, the impedance Z_L is [3]

$$Z_L = \frac{1}{\left(gm_2 - \frac{gm_2 \cdot Xo^2(\omega) - Ro}{Ro^2 + Xo^2(\omega)} \right) - j\left(\frac{1}{Xs(\omega)} + \frac{1 + gm_2 Ro}{Ro^2 + Xo^2(\omega)} \cdot Xo(\omega) \right)}$$

$$= R(\omega) + jX(\omega) \cdots\cdots\cdots (1)$$

where Ro is the output resistor of M2

$$Xs(\omega) = \frac{-1}{\omega Cgs_2}$$

$$Zo(\omega) = jXo(\omega) = \frac{1}{j\omega Cgd_2} // R_A // j\omega L_{d1}$$

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The impedance Z_L is very close to 50 Ω over the bandwidth due to the common gate typology of transistor M2. We can assume Z_L is 50Ω for simplified calculated.

A transformer model [5] is shown in Fig.3 where L1=0.5nH, L2=1nH, k=0.6, n=2 in proposed LNA.

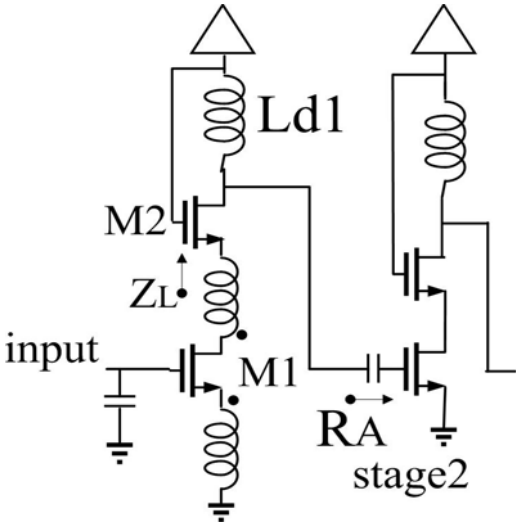

Fig. 2. Proposed LNA input stage

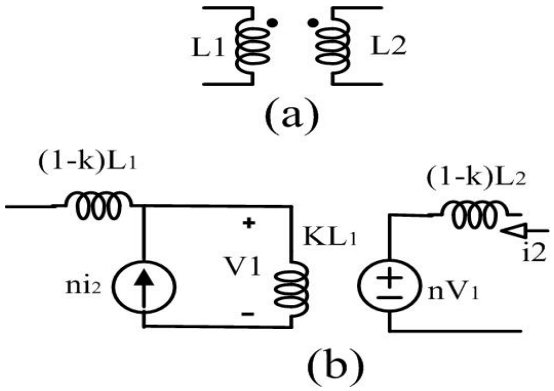

Fig. 3. (a) Transformer (b) Equivalent circuit of transformer

By replacing the transformer equivalent circuit into Fig.2 and the input matching small signal circuit is shown in Fig.4.

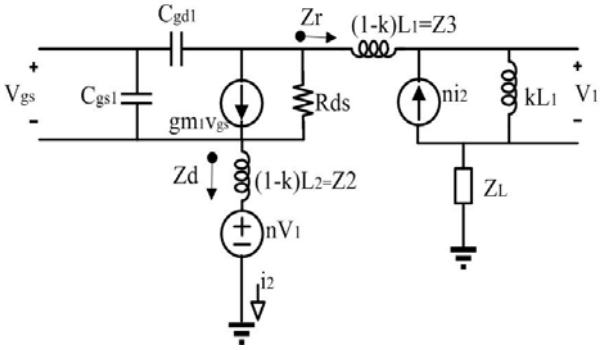

Fig. 4. Input matching small signal circuit

where

$$Zr = Z3 + Z_L - (n-1)Z1$$

$$= j\omega(1-k)L1 + R(\omega) + jX(\omega) - j\omega kL1$$

and

$$Zd = Z2 + (n^2 - n)Z1$$

$$= j\omega(1-k)L2 + 2\,j\omega kL1$$

$$= j\omega\left[(1-k)L2 + 2kL1\right] = j\omega Ls$$

where Ls=[(1-k)L2+2kL1]

Zd is an inductor and simplified input matching mechanism is shown in Fig.5

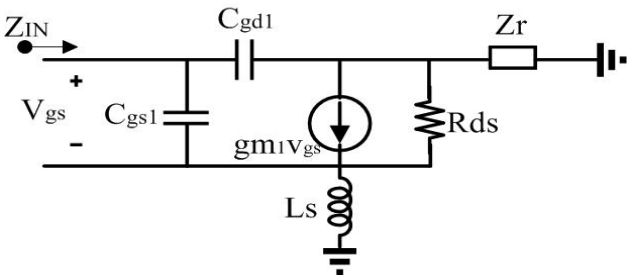

Fig. 5. Simplified input matching mechanism

To calculated input impedance for high frequency, C_{gs1} C_{gd1} must be taken into account[6] and the S11 smith chart is shown in Fig .6.

$$Zin \approx \left(\frac{1}{j\omega Cgs1} + \frac{LsyGm}{Cgs1}\right)\left[1 + \frac{Cgd1}{Cgs1}(1 + yGmZr)\right]^{-1}$$

$$y = \frac{Zr}{Rds + Zr + j\omega Ls}$$

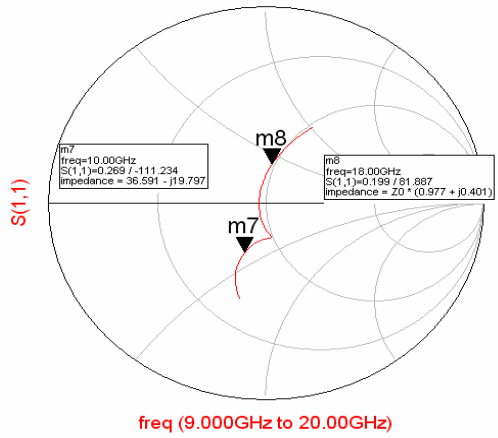

Fig. 6. S11 of proposed LNA

Due to the transformer feedback and the parasitic capacitance, the real part of S11 in Fig.6 is close to 50 Ω over 10~18GHz. Meanwhile the circuit has low NF because only the parasitic capacitance in the gate of M1.

III. POST-SIMULATION RESULTS AND LAYOUT PHOTOGRAPH

This section presents the post-simulation results of proposed LNA operating over 10-18GHz under typical-typical corner with a supply voltage of 1.8V. This work is designed and simulated using TSMC 0.18μm mixed signal/RF CMOS 1P6M technology. The transformer and inductors in the circuit is verified by EM-Simulate(ADS momentum.)

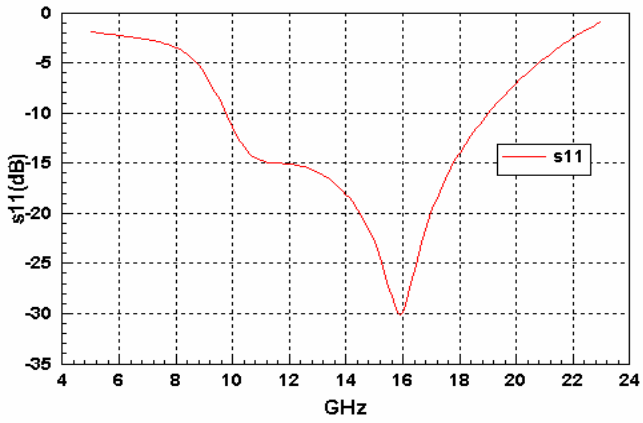

Fig.7 Post-simulated S11 versus frequency

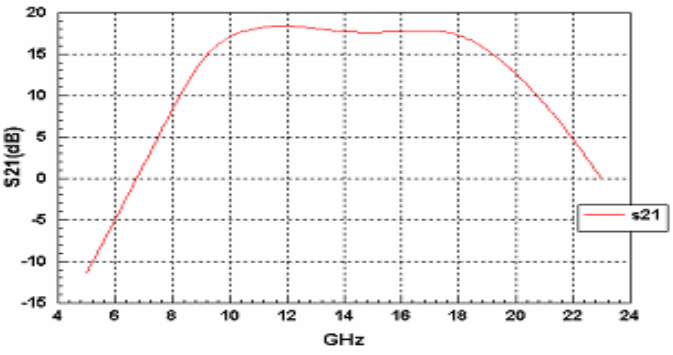

Fig.8 Post-simulated S21 versus frequency

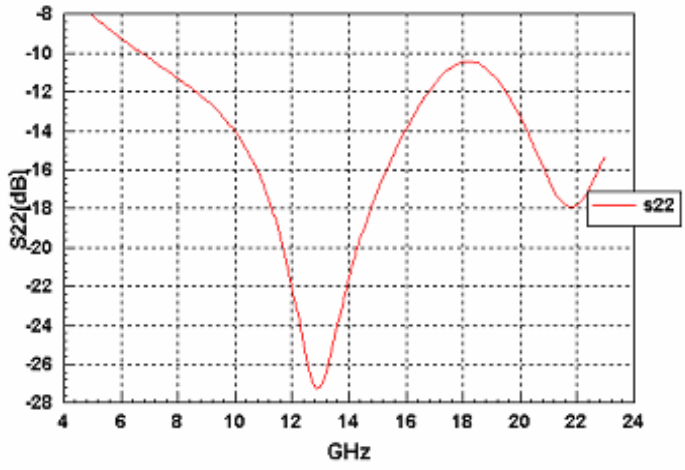

Fig.9 Post-simulated S22 versus frequency

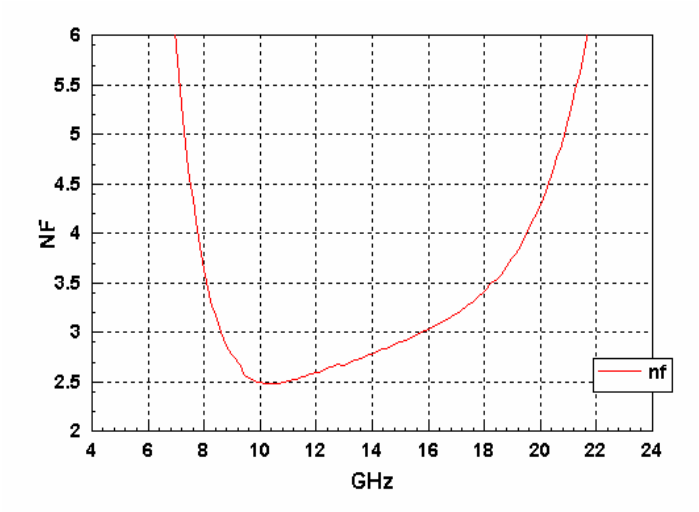

Fig. 10 Simulated NF versus frequency

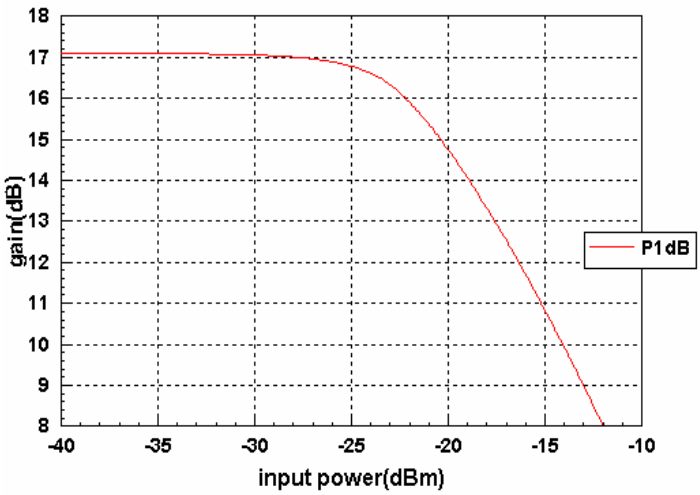

Fig. 11 P1dB for 15GHz

The S-parameter is shown in Fig. 7, Fig. 8, and Fig. 9 where S11 in Fig.7 < -15dB over 11~17GHz. The gain (S21) in Fig.8 is 17dB from 10 to 18GHz with variation less than 1dB. S22 in Fig.9 is less than -10dB over 10~18GHz. The transistor's size and the transformer must be fine tuned to provide a good input impedance matching and low noise. The simulated noise figure is shown in Fig. 10. In Fig. 10,it has been shown that the minimum NF is 2.5dB at 10GHz, and increase to 3.4dB at 18GHz. The P1dB in Fig.11 is -22.6dBm for 15GHz. The total power consumption is 37.6mW.

The layout of the LNA is shown in Fig. 12. The chip area is 1mm by 0.8mm.

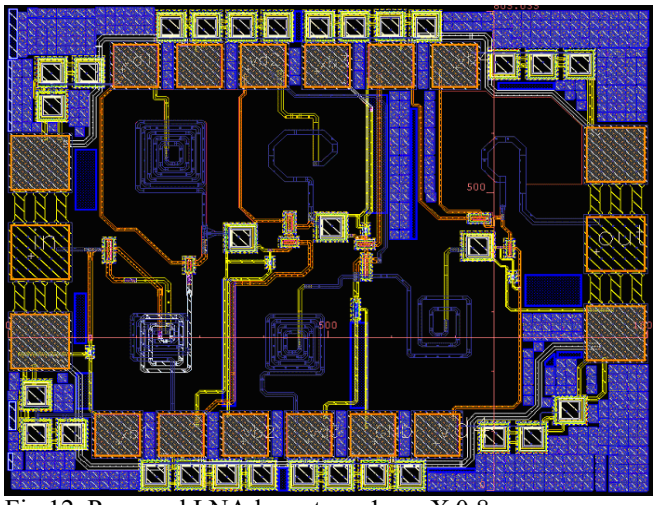

Fig.12 Proposed LNA layout 1mm X 0.8mm

CONCLUSION

In this paper, a novel wide bandwidth LNA is proposed based on CMOS TSMC 0.18μm mixed signal/RF process. We only need parasitic capacitance and transformer feedback to achieve input matching over 10~18GHz. And due to the simplicity of the wideband input matching mechanism, very low noise can be achieved from 10~18GHz.

Acknowledgment

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