The Safe Operating Area of GaAs-Based Heterojunction Bipolar Transistors

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***Abstract*—The safe operating area (SOA) of GaAs-based heterojunction bipolar transistors has been studied considering both the self-heating effect and the breakdown effect. The Kirk effect induced breakdown (KIB) was considered to account for the decrease of the breakdown voltage at high currents. With reasonable emitter ballastors, the KIB effect was shown to be the major cause for device failure at high currents, while the thermal effect controls the low current failure. The effect of emitter resistance and base resistance on device stability was also studied. While the emitter resistance always improves the device stability by expanding the SOAs, the base resistance degrades SOAs when the KIB dominates the failure mechanism. The effect of the base resistance on SOAs was explained by its control on the flow of the avalanche current. Since the KIB effect depends on the collector structure, it was shown that a nonuniformly doped collector can effectively improve the SOAs.**

***Index Terms*—GaAs, heterojunction bipolar transistor (HBT), Kirk effect, safe operating area (SOA), self-heating.**

I. Introduction

GaAs-BASED heterojunction bipolar transistors (HBTs) have long been recognized as the leading device technology for high-speed high-power applications. With the increased popularity of wireless communications, extending the HBTs' capability into even higher power for base-station applications is quite obvious. To significantly increase the power-handling capability, the devices need to be operated at voltages much higher than what is normally used today. We have recently demonstrated a 28-V InGaP/GaAs power HBT with high efficiency and high linearity [1]. The BV_{cbo} of the transistors was beyond 70 V. Kurpas *et al.* have also reported InGaP HBTs with high-voltage capabilities [2]. The advantages of using InGaP HBTs over traditional LDMOSs include better efficiencies, higher operating frequencies and better linearity.

However, HBTs, as in all bipolar devices, suffer from various feedback phenomena, which may cause instability and device failure in certain operating conditions. The most well-known damaging effect is the "thermal runaway" caused by self-heating [3]–[9]. When a bipolar transistor is operated at high powers, the increased junction temperature causes the bandgap energy and therefore the emitter junction built-in potential to drop. As a result, the collector current increases. An approximate expression for the collector current under such electrothermal feedback can be shown as

$$I_c = I_0 \exp\left[\frac{q}{kT}(V_{\mathrm{be}} - R_e I_e - R_b I_b + R_{\mathrm{th}}\phi I_c V_{\mathrm{ce}})\right] \quad (1)$$

where R_{th} is the thermal resistance and ϕ is the electrothermal-feedback coefficient, typically 1.25 mV/°C for GaAs. At high-power operations, the I_c–V_{be} curve can bend backwards at high currents. Once the device hits the bend-over point, it can have two solutions for its current–voltage (I–V) characteristics, and therefore causing device instability. If there are multiple fingers, some of the fingers may go into the high-current state and some into the low-current state, causing the hot fingers to thermally run away. A simple way to alleviate this problem is to increase R_e, or to add ballast resistors [10]–[13]. The instability can then be delayed to higher currents. In normal operations where I_b is much smaller than I_e, the instability [or safe operating area (SOA)] boundary is defined by, according to (1)

$$I_c = \frac{kT/q}{R_{\mathrm{th}}\phi V_c - R_e}. \quad (2)$$

II. Kirk Effect-Induced Breakdown (KIB) and Its Effect on SOA

For transistors operated at high voltages, another effect that is even more devastating can happen. That is the impact ionization or avalanche effect. When this happens in the collector, for an n-p-n transistor, the avalanche current results in a hole current back injected into the base [14]–[18]. This current can reverse the sign of the base–current, so the third term in (1) behaves similarly to the self-heating effect. It causes V_{be} to drop and leads to device instability. This impact ionization caused instability can be much worsened when the Kirk effect happens. For transistors with high BV_{cbo}'s, the collector doping is usually low. When the injected carrier density exceeds the doping density, Kirk effect takes place and the location of the peak electric field shifts from the base–collector interface to the collector–subcollector interface. If the collector voltage is high enough, an avalanche breakdown happens. Because the space-charge concentration in the collector is now $(J_c/q\nu_s) - N_d$, which increases with the current flowing through the collector, the impact ionization and avalanche breakdown will take place at a lower voltage as the current increases. The additional base–current caused by the avalanche process can provide a feedback mechanism resulting in device failure.

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This mechanism can be seen clearly from the following expression for the collector current under the breakdown condition

$$I_c = \alpha M I_0 \exp\left[\frac{q}{kT}(V_{\mathrm{be}} - R_e I_e - R_b I_b^* + R_{\mathrm{th}}\phi I_c V_{\mathrm{ce}})\right] \tag{3}$$

where α is the common base–current gain and M is the avalanche multiplication factor. Notice that the base–current I_b^* now includes the hole current flowing back to the base terminal due to the impact ionization in the collector. Since the avalanche current is in the reverse direction of the normal base–current, the voltage drop across the base resistance will change sign when the back injected hole current is higher than the normal base–current. Therefore, this base-resistance voltage drop serves as a positive feedback for the collector current in the same way as the self-heating effect. Therefore, under this situation, the device will also be killed.

The commonly used expression for the multiplication factor is

$$M = \frac{1}{\left(1 - \frac{V_{\mathrm{bc}}}{\mathrm{BV}_{\mathrm{cbo}}}\right)^n}. \tag{4}$$

Because of the Kirk effect, $\mathrm{BV}_{\mathrm{cbo}}$ needs to be changed to the breakdown voltage $\mathrm{BV}_{\mathrm{KIB}}$ with the presence of the collector current. Since the effective space-charge concentration changes sign and increases with the current because of the Kirk effect, this new breakdown voltage $\mathrm{BV}_{\mathrm{KIB}}$ decreases as the collector current increases. Therefore, the onset voltage of instability decreases with the current. For transistors with low collector doping, as in most high-voltage transistors, the KIB effect becomes the major cause for device failure at high currents. This breakdown-caused device failure is much more important than the thermal effect when devices are under RF operation. The thermal effect has a very long time constant, so it does not show up easily when devices are operated at high frequencies. But the breakdown effect is nearly instantaneous, the device will be killed immediately when the device's operating point hits the unstable point.

Therefore, in order to define the SOA of an HBT, one has to consider both the thermal effect and the KIB effect. In the I_c–V_{ce} plane, the SOA boundary defines the region that the device can be safely operated. Once the device's operating point hits the SOA boundary, two solutions will result leading to a device failure. After understanding the cause for device instability, the SOA boundary can be solved by searching for the unstable points using (1), (3), and (4). To account for the effect of the terminal resistors, which are important in the feedback effects mentioned above and when external ballast resistors are used, the terminal voltages are adjusted to include all the voltage drops across the resistors. Since $\mathrm{BV}_{\mathrm{KIB}}$ depends on the current injected into the collector because of KIB, $\mathrm{BV}_{\mathrm{KIB}}$ as a function of the current has to be determined before the equations can be solved. It should be mentioned that this current is only the current injected from the emitter, the current from the avalanche process, which generates an equal amount of electrons and holes, should not be included.

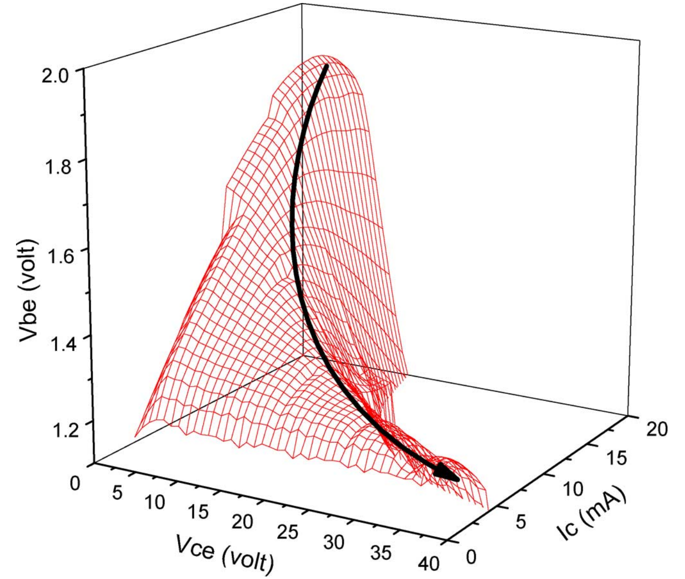

Fig. 1. Three dimensional plot of the characteristics of an HBT in the I_c–V_{ce}–V_{be} space. The ridge of the mountainlike surface is the SOA boundary.

In this paper, $\mathrm{BV}_{\mathrm{KIB}}$'s under different current injection conditions are calculated using a one-dimensional semiconductor device simulator "SimWindows" [19]. The effective space-charge concentration in the collector is taken to be $N_d(x) - J/q\nu_s$, where $N_d(x)$ is the collector's doping density and ν_s is the electron's saturation velocity. The breakdown is defined when the peak electric field reaches the critical breakdown field. We have compared this calculation with the more elaborate calculation using electron/hole impact ionization rates. The results are very close to each other.

III. Representations of SOAs

The mutually dependent (1)–(4) were solved for the device I–V characteristics. Temperature dependencies of the current gain and the thermal resistance were taken from the experimental results and were considered in the calculation. The solved device characteristics are best described by a three-dimensional (3-D) plot in the I_c–V_{be}–V_{ce} space. Any two variables are enough to determine the device's operation point in this space. All the allowed solutions are therefore represented by a surface in the 3-D plot. Here, we take an example of an InGaP/GaAs n-p-n HBT with a collector thickness of 2.5 μm, which is uniformly doped to a doping concentration of 6×10^{15} cm^{-3}. The emitter size was assumed to be 3×8 μm^2, the emitter resistance (including ballastor), base resistance, and collector resistance were taken to be 50, 17, and 2 Ω, respectively. The calculated I–V characteristics are shown in Fig. 1. The X- and Y-axes are taken as V_{ce} and I_c while the Z-axis is V_{be}. This mountain-shaped surface represents the allowed operation points for the device. The mountain ridge, which runs from the high I_c, low V_{ce} corner to the low I_c, high V_{ce} corner, is the local maximum for V_{be} and is the dividing line for the device's safe operation and unstable operation. We can picture this as follows: If we bias the device with certain V_{ce} and slowly increase the collector current, the V_{be} value goes up until it

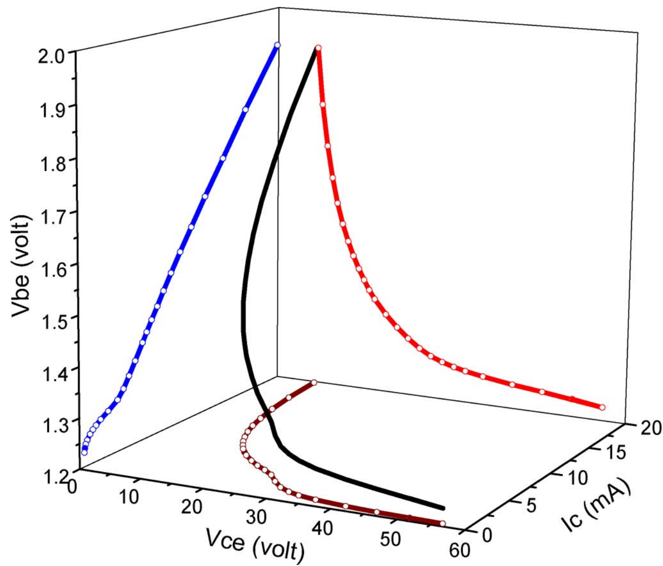

Fig. 2. Three dimensional SOA curve and its projections on the $V_{\rm be}$–$V_{\rm ce}$, I_c–$V_{\rm ce}$, and $V_{\rm be}$–I_c planes.

reaches the ridge of the mountain. At this point, $V_{\rm be}$ can no longer go any higher. If we let $V_{\rm be}$ go down, there are two paths for the device to go down hill. In other words, there will be two solutions, one with a higher current and the other with a lower current once the device passes the ridge. Therefore, the device fails if its operation reaches the ridge. This ridge, which is a curve in our 3-D space, is therefore the SOA boundary. The projections of the curve onto the I_c–$V_{\rm ce}$, I_c–$V_{\rm be}$, and $V_{\rm be}$–$V_{\rm ce}$ planes are the different representations of the SOA boundary in different coordinate systems. The calculated SOA boundary and its representations in the three planes for our example are shown in Fig. 2.

Since the SOA is usually shown as a curve in the I_c–$V_{\rm ce}$ plane, we focus our following discussions on the representation on this plane (however, we need to bear in mind that the real curve should be in a 3-D space). First, we did a set of calculations with constant $V_{\rm be}$ inputs of 1.25, 1.3, 1.4, 1.5, and 1.6 V. The calculated I–V curves are shown in Fig. 3. For each curve, there is a bend-over point, beyond which the device becomes unstable, because each $V_{\rm ce}/V_{\rm be}$ pair gives two solutions. The connection of all the bend-over points is the SOA boundary, which is the same as the projection of the 3-D SOA curve on the I_c–$V_{\rm ce}$ plane.

To find out the root cause for instability, we show in Fig. 4 the terminal base–currents along with the I–V's shown in Fig. 3. As $V_{\rm ce}$ increases, both I_c and I_b increase due to self-heating. When $V_{\rm be}$ is high, higher than 1.3 V, in this case, I_b suddenly drops and goes to negative when the instability point is reached. This is the impact ionization or avalanche effect we mentioned earlier. The hole current generated by the avalanche process in the collector back injects into the base, causing the reverse of the base–current. Because the avalanche current easily overwhelms the base–current, the base–current reversal point is generally the instability point. Due to the Kirk effect, the breakdown voltage decreases as $V_{\rm be}$ (or I_c) increases, the instability point (or the SOA boundary) takes place earlier (at lower $V_{\rm ce}$'s) when $V_{\rm be}$ is higher. At a very low $V_{\rm be}$ (e.g.,

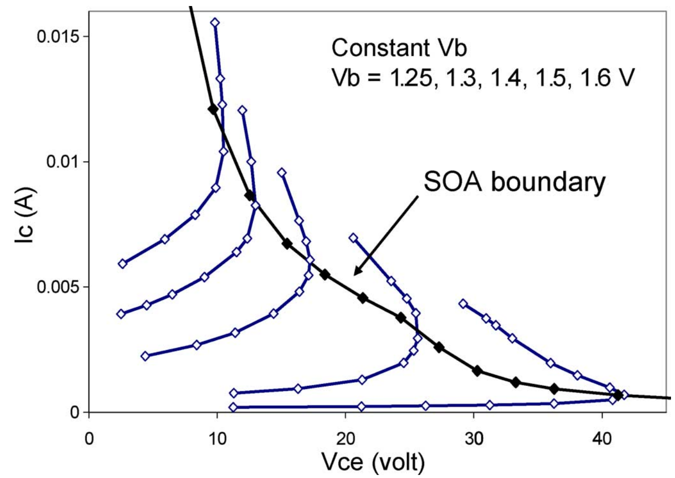

Fig. 3. Device I–V characteristics with various $V_{\rm be}$ inputs. The bend-over points are the places that the device becomes unstable. Therefore, the connection of the bend-over points is the SOA boundary.

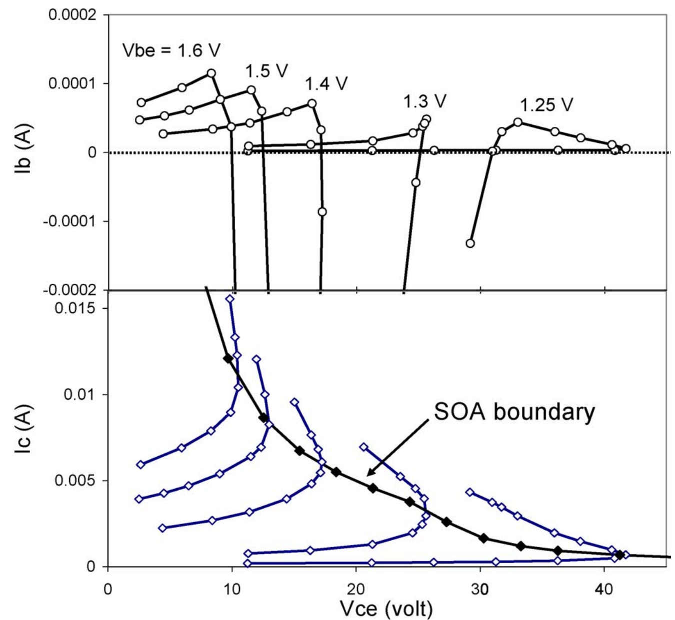

Fig. 4. Base–currents of the device curves shown in Fig. 3. The base–current reversal is due to the avalanche current being injected back into the base, and it indicates the onset of the device instability when the KIB is the dominant failure mechanism.

1.25 V), the instability point happens before the reversal of the base–current. This is because, the instability is caused by the self-heating not by the breakdown effect. As described earlier, both self-heating and avalanche effect can cause instability. The question is which one is the dominant effect at a given bias condition. In the example presented here, at $V_{\rm be} = 1.25$ V, the breakdown voltage is higher than the thermal instability point shown in (2). Therefore, the device failure is controlled by the self-heating effect. But, at higher $V_{\rm be}$'s, the breakdown voltage is reduced by the Kirk effect and becomes lower than those defined by the thermal effect. The device failure is controlled by the avalanche effect, and the failure point is clearly marked by the sudden decrease and the reversal of the base–current.

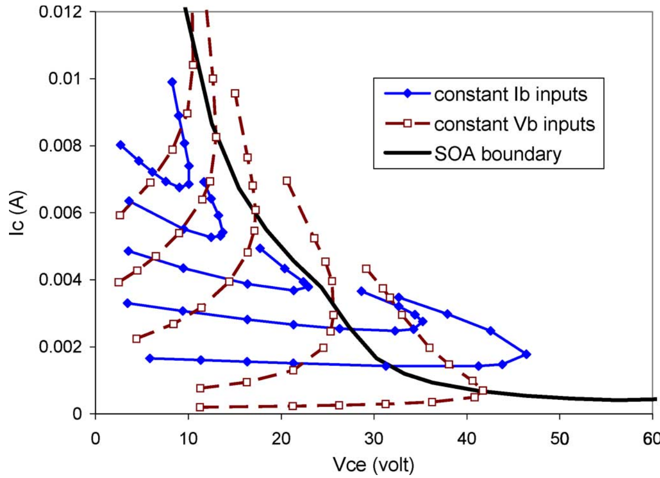

Fig. 5. Device I–V characteristics with various I_b inputs along with those constant V_b inputs. The bend-over points of the curves with constant I_b inputs, some of them lie inside the SOA and some outside, are not the failure points.

The SOA boundary should not be confused with the commonly regarded unstable boundary determined by the I–V curves with constant I_b inputs. Fig. 5 shows a family of I–V curves with constant I_b and constant V_b inputs. Obviously, the curves bend over at different places. The boundary defined by the bend-over points with constant I_b inputs is different from the SOA boundary. It should be understood that a bend-over in the I–V curve does not necessarily mean that the device will be killed at that point. For constant I_b inputs, the device will not be killed even the curves bend over if the device is measured properly and as long as the curves stay within the SOA boundary. For the example given in Fig. 5, the bend-over boundary defined by constant I_b inputs lies within the SOA boundary at high currents, while at low currents, it goes beyond the SOA boundary. Therefore, the device will never be able to reach the bend-over points at low I_b inputs. But, at high I_b's, the device will not fail even it bends over.

The failure of a device when the operation point comes across the SOA boundary is best illustrated by a two-finger simulation. Here, we assume a transistor with two identical fingers, each with an emitter size of 24 μm^2. The structure of the device is the same as before. The transistor is assumed to be operated along a load line with a V_{cc} bias of 31 V and a load resistance of 2000 Ω. This load line crosses the SOA boundary at two places. When they cross each other, the device becomes unstable and the two fingers go into two different states with one going to the high-current state and the other one going to the low-current state. The 3-D plot of the load line and the SOA boundary, and that of the two finger characteristics when the load line and the SOA meet each other are shown in Fig. 6(a) and (b). As described above, once the device operation point hits the SOA boundary, there are two solutions or two different paths for the device to go down hill. These two different paths are the I–V's for the two different fingers. The planar view of the I–V relationship when this happens is shown in Fig. 6(c).

The time evolution of the device failure can be seen from the waveform of the output current by assuming a sinusoidal input voltage swing. It is shown in Fig. 7(a). In this calculation, we have purposely made the emitter resistance slightly different for the two fingers, one with 49.99 Ω and the other with 50.01 Ω, to see how failure takes place. In each cycle, there are four failure points. Between the high-current and low-current failure points, there is a forbidden region that the device cannot enter. If the time evolution goes from left to right, the two points that make the device fail are point A and point C. The reason that these two points are the failure points can be clearly seen from the expanded view of these two points shown in Fig. 7(b) and (c). The other two points, which are mirror images of points A and C, are not accessible because time goes only in one direction. When the device reaches either point A or point C, the currents of the two fingers diverge as time progresses, leading to a device failure.

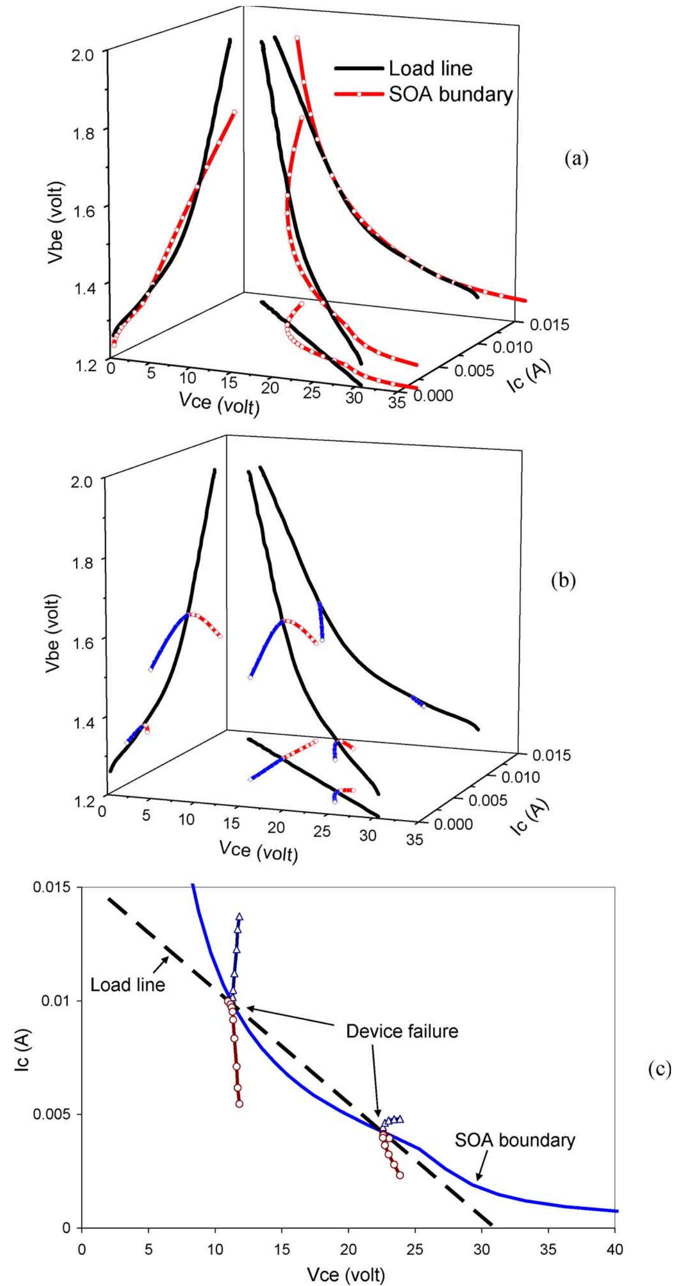

Fig. 6. (a) Three dimensional plot of a load line that interests the SOA boundary in two places. (b) Three dimensional plot of the I–V characteristics of the two fingers when the load line crosses the SOA boundary. (c) Two-finger I–V characteristics in the I_c–V_{ce} plane.

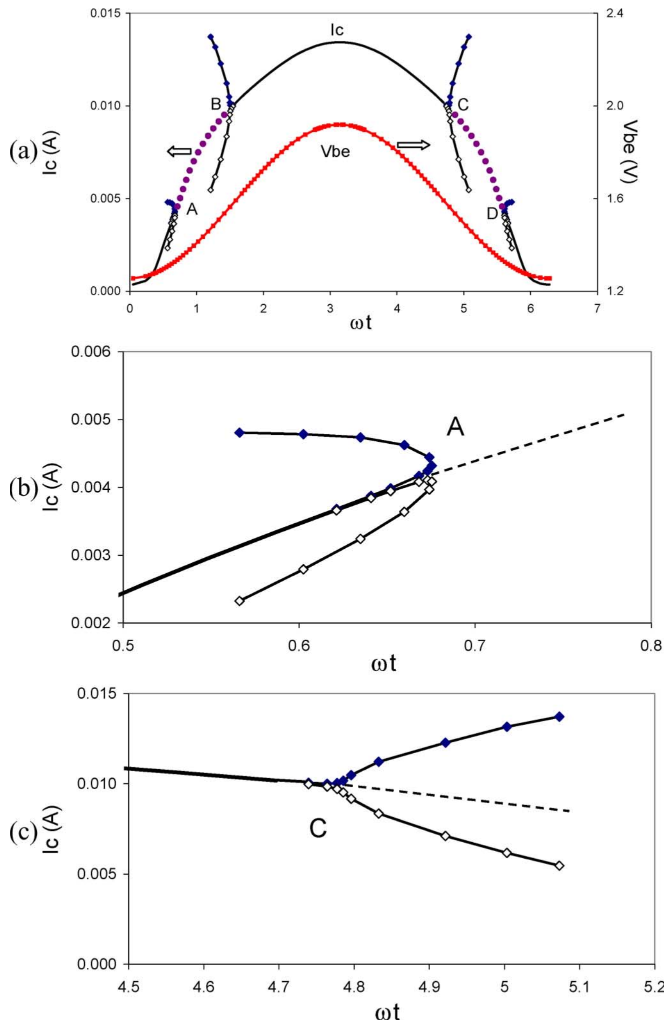

Fig. 7. (a) Waveforms of the output current and the input voltage. The four points marked on the figure are where the device operation point hits the SOA boundary. The splitting of the current for the two fingers indicates how the device fails. (b) Expanded view of point A. (c) Expanded view of point C.

IV. Effects of Emitter Resistance and Base Resistance on SOAs

It is well known that the use of emitter ballast resistors reduces the transistors' thermal instability. Its effect on the impact ionization caused SOA is the same. Based on (3), R_e always provides a negative feedback that alleviates the positive feedback caused by the self-heating and impact ionization. The role of the base resistance on device stability is more complicated. If the SOA is controlled by self-heating alone, a higher base resistance would result in a better SOA, the same way as the emitter resistor does. But, if the SOA is controlled by the impact ionization, because the avalanche current may reverse the base–current, a higher base resistance would result in a worse SOA.

Fig. 8 shows the calculated SOA boundaries for $R_e = 50$ and 70 Ω. The SOAs caused by self-heating alone and breakdown effect alone are also shown for comparison. It can be seen that at high voltages, the SOAs are controlled by the thermal effect. But, at high currents, because the Kirk effect reduces the breakdown voltage, the SOA boundaries move to much lower

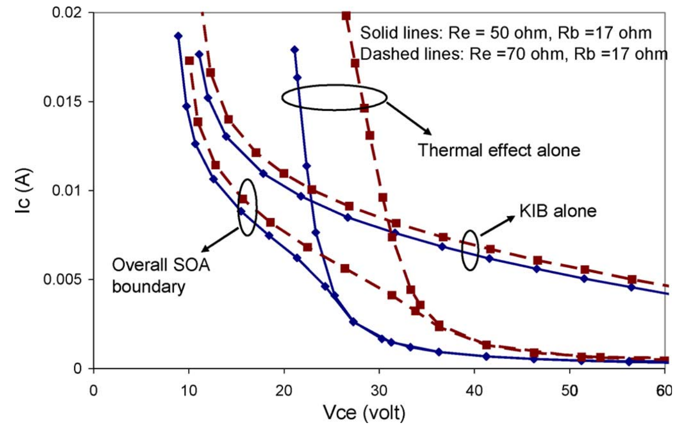

Fig. 8. SOA boundaries for $R_e = 50\ \Omega$ and $R_e = 70\ \Omega$. The SOAs caused by thermal effect only and those caused by KIB effect only are also shown.

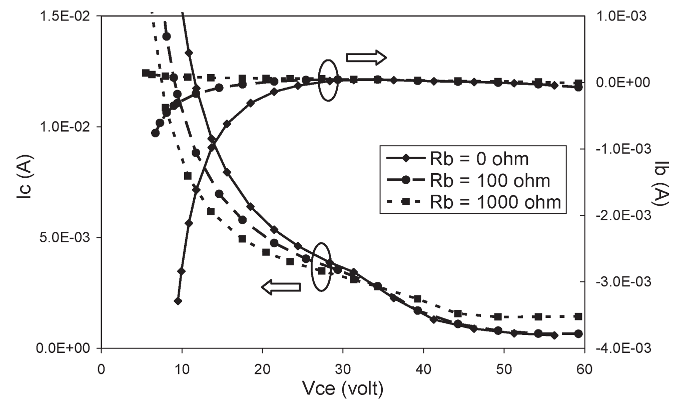

Fig. 9. Effect of R_b on the SOAs. Base ballasting can improve SOAs controlled by thermal effect but degrade the SOAs controlled by KIB effect.

voltages and are controlled by the KIB effect. The thermal SOA has a very strong dependence on R_e, as discussed in (2). But, its effect on the SOAs controlled by the KIB effect is much smaller. Therefore, the effect of the emitter ballast resistors on high-current SOAs is very limited.

The base resistance plays two roles in SOAs. It increases the SOA when the device stability is governed by self-heating, and the avalanche effect is not a concern, but reduces the SOA when the opposite is true. Fig. 9 shows the calculated SOAs for $R_b = 0$, 100, and 1000 Ω. At high currents, the SOA is smaller as R_b increases. At low currents and high voltages, a high R_b, however, gives a better SOA. As explained earlier, the effect of R_b is similar to that of R_e when there is no impact ionization in the collector. The effect, however, is reduced by a factor of the current gain because the voltage drop across the base resistance is proportional to the base–current. Therefore, one has to use a very large base resistor as the ballastor in order to see any improvement in SOA. However, at high currents when the SOA is controlled by the KIB effect, we do not need to have a very large base resistance in order to see the degradation in SOA. Because of the back flow of the avalanche current going to the base terminal is directly controlled by the base resistance, a smaller change in base resistance can have a profound effect on the SOA. Therefore, in device applications, if one operates the device at high currents, it is important to avoid high base resistance.

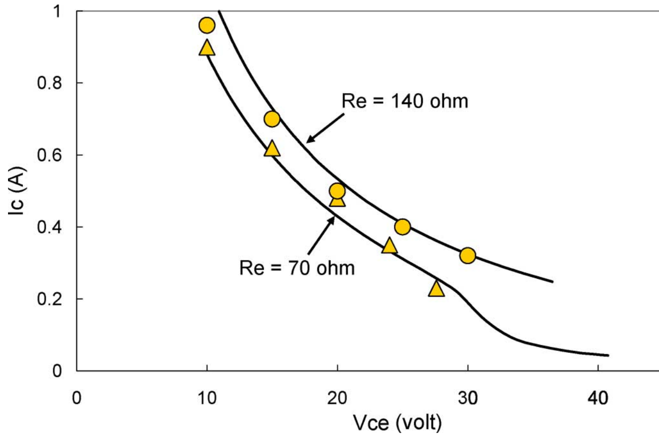

Fig. 10. Measured and calculated SOAs for a 64 finger high-voltage transistor. The emitter resistances were 70 and 140 Ω.

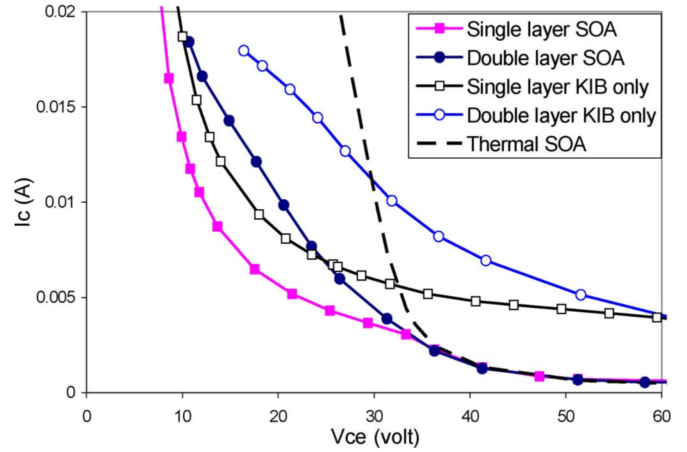

Fig. 11. SOA of a two-layer (low–high) collector HBT. One can tailor the SOAs by properly adjusting the collector doping profile.

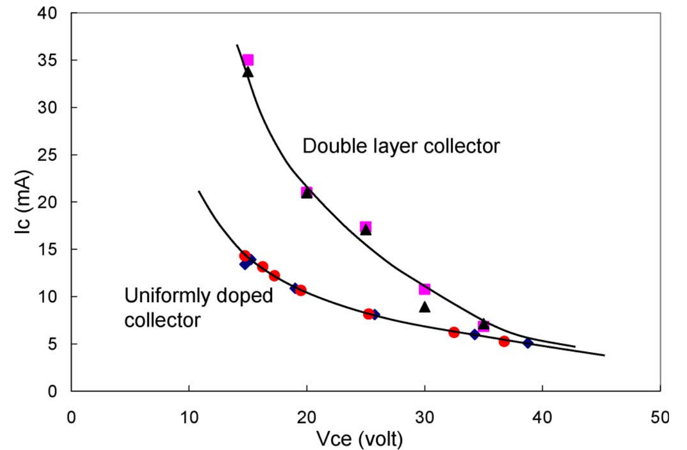

Fig. 12. Experimentally measured SOAs of HBTs with a uniformly doped collector and those with a two-layer collector.

The calculation presented here has been used to fit the experimental results of our high-voltage HBTs. The device consisted of 64 fingers. The collector was doped to a density of 6×10^{15} cm^{-3} and had a thickness of 3 μm. Emitter ballast resistances of 70 and 140 Ω were used. The measured SOAs and the calculated ones are shown in Fig. 10. Very good agreement was obtained. The fact that the SOAs are pretty close to each other at high currents when very different ballast resistors are used cannot be explained by self-heating alone. It is because that the failure mode was controlled by the KIB effect mentioned above.

V. Nonuniformly Doped Collector for Improved SOA

Since the KIB effect depends on the collector structure very much, it is possible that one can tailor the doping profile in the collector to improve the SOAs. For a uniformly doped collector, when the Kirk effect happens, the injected carrier concentration exceeds the doping density in the collector. The effective space-charge density changes sign and is modified to $(J_c/q\nu_s) - N_d$. It causes the high-field region in the collector to move from the base–collector interface to the collector–subcollector interface. Therefore, when breakdown happens, it happens in the region close to the subcollector. For a given collector voltage, the peak electric field will be lower when the net space-charge concentration is lower. Therefore, a higher N_d in the high-field region would reduce the intensity of the peak electric field. Based on this principle, one can significantly increase the breakdown voltage at high currents without sacrificing too much on the low-current breakdown voltage ($\mathrm{BV_{cbo}}$), by using a nonuniformly doped collector with a high doping region close to the subcollector and a low doping region close to the base. Such structure has been shown experimentally to improve SOAs [20], [21].

Fig. 11 shows the calculated SOA curves for a two-layer collector structure along with those of our standard uniformly doped collector structure. The two-layer structure has a collector doping of 4×10^{15} cm^{-3} for the first 2 μm and 4×10^{16} cm^{-3} for the next 0.5 μm. The $\mathrm{BV_{cbo}}$ of this device (65 V) is similar to that of the device with a uniform collector (65.5 V) presented above. The emitter resistance used in the calculation is 70 Ω. Comparing the two devices, we can see that the SOA is greatly improved at high currents. At low currents, the two curves are about the same because they are limited by the thermal effect. If we assume that there is no self-heating, which is the case during RF operations, the improvement is even larger (The curves are also shown in the figure). While the two-layer structure used here is not optimized, it is possible that the SOA curve can be tailored to fit the desired device applications by adjusting the doping profile in the collector. Fig. 12 shows the experimentally measured SOAs for InGaP HBTs with two different collector structures, one with a uniformly doped collector and the other with a two-layer collector. The last 0.2 μm of the collector for the two-layer structure was doped ten times higher than the rest of the collector. It can be seen from the figure, a great improvement in SOA is achieved at high currents. This is the result of the improved KIB because of the use of a high doping level close to the subcollector.

VI. Conclusion

In conclusion, we have presented a comprehensive study of the SOA of an HBT. The onset of the device instability is clearly

defined in the I_c–$V_{\rm be}$–$V_{\rm ce}$ space. Both the thermal effect and the impact-ionization effect were taken into consideration. The importance of the KIB was analyzed and was shown to be the dominant failure mechanism for devices operated at high currents. The roles of emitter resistance and base resistance on device stability have also been studied. While emitter ballastors are useful for improving SOAs, the base resistance can be harmful when the device failure is controlled by the KIB effect. Since the KIB effect depends on the doping structure of the collector, one can significantly improve the SOAs by properly designing the doping profile in the collector.

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