Modeling the Well-Edge Proximity Effect in Highly Scaled MOSFETs

Yi-Ming Sheu, Ke-Wei Su, Shiyang Tian, Sheng-Jier Yang, Chih-Chiang Wang, *Member, IEEE*, Ming-Jer Chen, *Senior Member, IEEE*, and Sally Liu

***Abstract*—The well-edge proximity effect caused by ion scattering during implantation in highly scaled CMOS technology is explored from a physics and process perspective. Technology computer-aided design (TCAD) simulations together with silicon wafer experiments have been conducted to investigate the impact of this effect. The ion scattering model and TCAD simulations provided a physical understanding of how the internal changes of the MOSFETs are formed. A new compact model for SPICE is proposed using physics-based understanding and has been calibrated using experimental silicon test sets.**

***Index Terms*—CMOS wells, high-energy ion implantation, ion scattering, MOSFETs, SPICE model, technology computer-aided design (TCAD) simulation.**

I. INTRODUCTION

As CMOS very large scale integration technology progresses to the nanometer regime, several physical effects become significant as a result of aggressive layout scaling [1]–[3]. MOSFETs are formed during the front end of the fabrication process, which mainly consists of shallow trench isolation (STI), MOSFET wells, and MOSFET gate formation. The effect of the well-edge proximity to the MOSFET gates was first reported in [4] and originates from the lateral scattering of ion implantations at the photoresist edge when forming MOSFET wells, which in turn causes a change in the MOSFET threshold voltage. Fig. 1 schematically shows the reason for the well-edge proximity effect on MOSFET devices from a cross-sectional viewpoint. The high-energy ions scattered at the well photoresist edge introduce extra dopant atoms in the silicon near the well edge. As the MOSFET gate approaches the well edge, the dopant concentration of the MOSFET core area will increase, therefore causing a comparative increase in threshold voltage. The effect becomes of increasing importance as CMOS devices continue to shrink further.

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Y.-M. Sheu is with the Device Engineering Division, Taiwan Semiconductor Manufacturing Company, Hsinchu 300, Taiwan, R.O.C., and also with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: ymsheu@tsmc.com).

K.-W. Su, S.-J. Yang, C.-C. Wang, and S. Liu are with the Device Engineering Division, Taiwan Semiconductor Manufacturing Company, Hsinchu 300, Taiwan, R.O.C. (e-mail: s_liu@tsmc.com).

S. Tian is with Synopsys, Inc., Dallas, TX 75254 USA.

M.-J. Chen is with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C.

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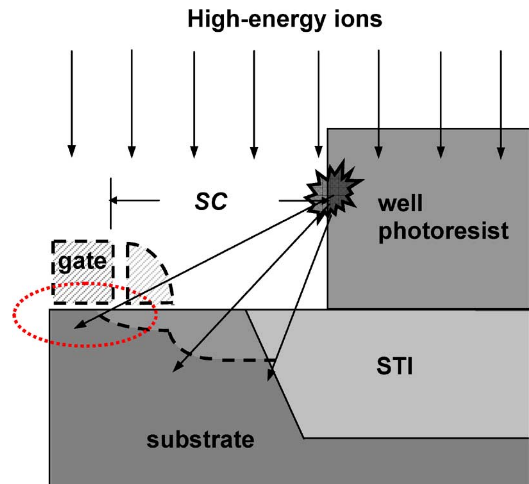

Fig. 1. Origin of well-edge proximity effect. High-energy dopant ions scatter at the well photoresist edge during well ion implantation, and the scattered ions are implanted in the MOSFET channel before the gate is formed. SC denotes the distance of the well photoresist edge to the MOSFET gate edge.

In this paper, a silicon wafer experiment was performed using state-of-the-art CMOS technology to investigate this effect. Monte Carlo ion scattering and integrated technology computer-aided design (TCAD) simulation were conducted to evaluate the dopant profile variations of the well ion implantation. Calibrated process and device TCAD simulations were used to quantify the impact on MOSFET electrical characteristics. Utilizing a physics-based understanding and silicon experimental results, a new model that corrects the inaccuracies of current SPICE models is proposed.

II. ION SCATTERING PHYSICS AND MODELING

Moving ions (projectiles) in a solid loose their energy via two independent mechanisms. The first mechanism is elastic nuclear stopping, which causes the ions to be scattered away from their original paths. The second mechanism is inelastic electronic stopping, which acts as a drag force causing negligible angular deflections of the moving ions.

The principal assumption of the Monte Carlo model is that the interaction of the energetic ions with the solid may be separated into a series of distinct two-body collisions (binary collision approximation). Thus, Monte Carlo modeling of ion implantation consists of following the ions from one scattering event to the next and properly accounting for all energy loss mechanisms and deflections. The Monte Carlo model for implants into crystalline silicon was described in detail in [5].

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Here, only models pertaining to high-energy ion implantation into the photoresist will be discussed.

In the Monte Carlo model, the photoresist is treated as an amorphous material with the average path length of the ion between collisions being $l = 1/\sqrt[3]{N}$, where N is the atomic density of the photoresist. The collision partners are randomly selected, assuming that the probabilities of encountering each component of atoms are proportional to their stoichiometric abundances (assuming 50% hydrogen, 37.5% carbon, and 12.5% oxygen). For each collision, the impact parameter is determined by $p = \sqrt{R_n} p_{\max}$, where R_n is a uniformly distributed random number between 0 and 1, and $p_{\max}$ is the maximum impact parameter given by $l/\sqrt{\pi}$. The interactions between the ions and the target atoms are modeled using the Ziegler–Biersack–Littmark universal interatomic potential [6]. If the atomic mass of the projectile is greater than that of the target atom, it can be shown that, for a single collision, a maximum scattering angle exists, i.e.,

$$\theta_{\max} = \arcsin\left(\frac{m_2}{m_1}\right) \quad (1)$$

where m_1 and m_2 are the atomic mass of the projectile and the target atom, respectively. Therefore, although hydrogen is more abundant in composition, carbon and oxygen are more effective in deflecting the implanted ions. Most ions experience many collisions before they are scattered out of the photoresist.

For electronic stopping, the Lindhard–Scharff (LS) formula [7] is used, i.e.,

$$S_e = \alpha \frac{1.212 Z_1^{7/6} Z_2}{\left[Z_1^{2/3} + Z_2^{2/3}\right]^{3/2} m_1^{1/2}} \sqrt{E} \quad (2)$$

where Z_1 and E are the atomic number and the kinetic energy of the projectile, respectively. Z_2 is the average atomic number of the photoresist, and α is an empirical correction factor. It is interesting to note that without any adjustment of the parameter α $(= 1)$, LS stopping power predicts the projected ranges of B and P implants below 1 MeV very well.

At high energy, the cross section for nuclear scattering is small, and the ions experience very few nuclear collisions. Thus, electronic stopping is the dominant energy loss mechanism. For example, for a B 300 keV implant, electronic stopping accounts for 88% of the total energy loss. In this energy regime, most ions move in approximately straight lines and are rarely scattered out of the photoresist. As the ions slow down and approach their projected range, the nuclear scattering cross section increases significantly, and nuclear stopping becomes dominant. After experiencing many collisions, some ions are scattered out of the photoresist edge. Once an ion is scattered out of the photoresist, it is assumed to move in a straight line until it reenters the silicon substrate. The exact entry point depends on the position at which the ion exits the photoresist, its direction of motion, and the topography of the device.

Fig. 2 shows the angular distribution and the depth distribution of the ions that are scattered out of the photoresist edge for B 300 keV and P 625 keV implants. Both of these dopants have approximately the same projected range at 1.08 μm in the photoresist. It is worthwhile noting that, for the given implant conditions, the total number of ions that are scattered out of the photoresist is roughly the same for both B and P. It can also be seen that most ions are scattered out of the photoresist just before reaching the projected range. In addition, ions exit the photoresist edge with a peak at angle of $\sim 10^\circ$, and a significant portion of ions exit with angles below 30°. Ions exiting at large angles may travel a long distance in a lateral direction and be implanted into the active area of the MOSFET. Thus, the dopant distribution due to the well-edge proximity effect can be accurately simulated using the Monte Carlo simulator.

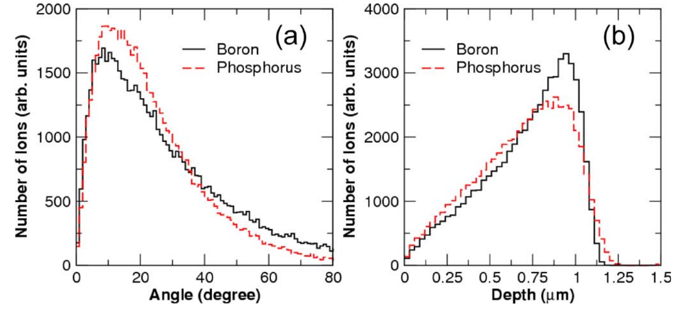

Fig. 2. (a) Angular and (b) depth distributions of the ions scattered out of the photoresist edge for B 300 keV and P 625 keV implants. Angle is measured from the incident direction, and depth is the vertical distance from the top surface of the photoresist to the point where the ion exits from the photoresist edge.

III. TCAD Numerical Simulation

Full-process two-dimensional TCAD simulation was performed to model MOSFET dopant distribution and electrical behavior. Monte Carlo well ion implantation mentioned in the previous section was applied to simulate the dopant scattering effect at the edge of the well photoresist. The well to gate edge distance is denoted as SC and is shown in Fig. 1. Ions scatter from the well photoresist edges and are implanted into the silicon active areas when forming retrograde wells using high-energy boron and phosphorus ion implantations for nMOSFET and pMOSFET, respectively. Fig. 3 shows the simulation dopant distributions after well ion implantations. In the graph for SC $= 0.9$ μm, the well dopant concentrations are low and almost constant at the silicon surfaces through the active area for both n- and p-wells. As SC decreases to 0.54 μm, several extra dopant clusters introduced from well-edge ion scattering can be observed at the STI and silicon surface near the well photoresist edges. When SC further decreases to 0.4 μm, the extra dopant clusters move toward the center of the active area, and the well dopant concentrations become higher in cases where the SC is larger. In Fig. 4, final vertical boron and phosphorus profiles along the MOSFET center for various well to gate edge distances are shown for nMOSFET and pMOSFETs, respectively. The additional implants, besides the retrograde well implants, are boron 1.4×10^{13} cm^{-2} 100 keV for the nMOSFET and phosphorus 1×10^{13} cm^{-2} 240 keV for the pMOSFET. As observed, the channel dopant concentration increases as the well photoresist edge approaches the MOSFET active area. To further quantify the extra dopant concentration

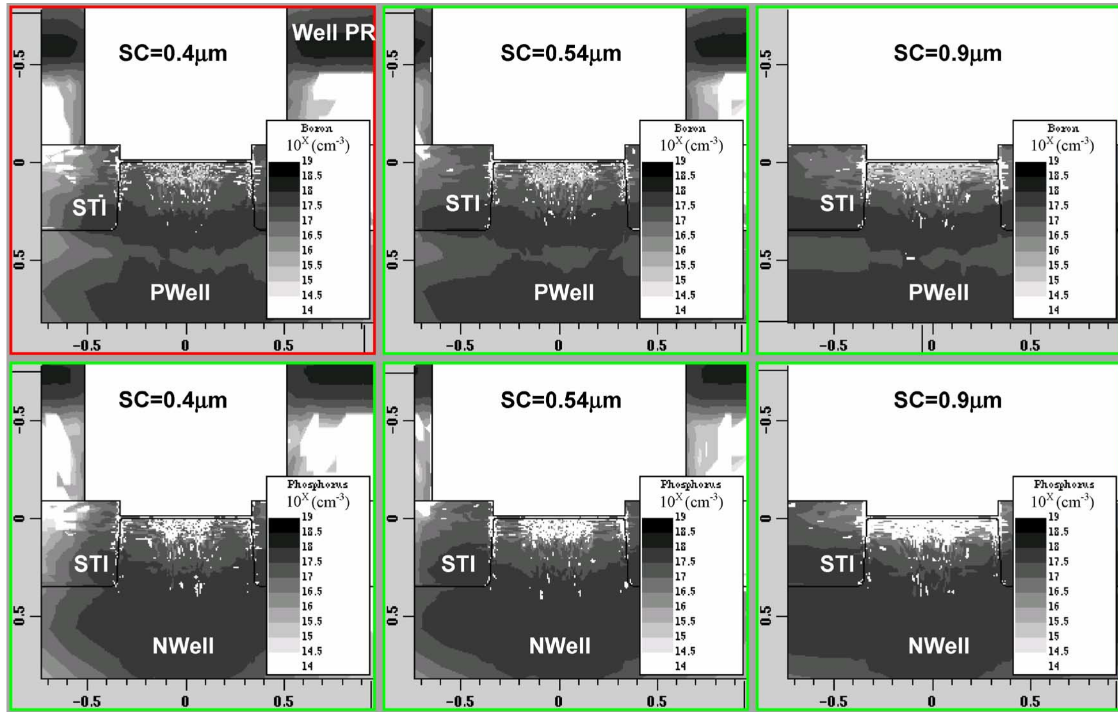

Fig. 3. TCAD-simulated dopant distribution versus well to gate edge distance SC. The well dopant distributions are influenced by the SC value. When SC decreases, extra well dopant clusters move toward the center of the active area.

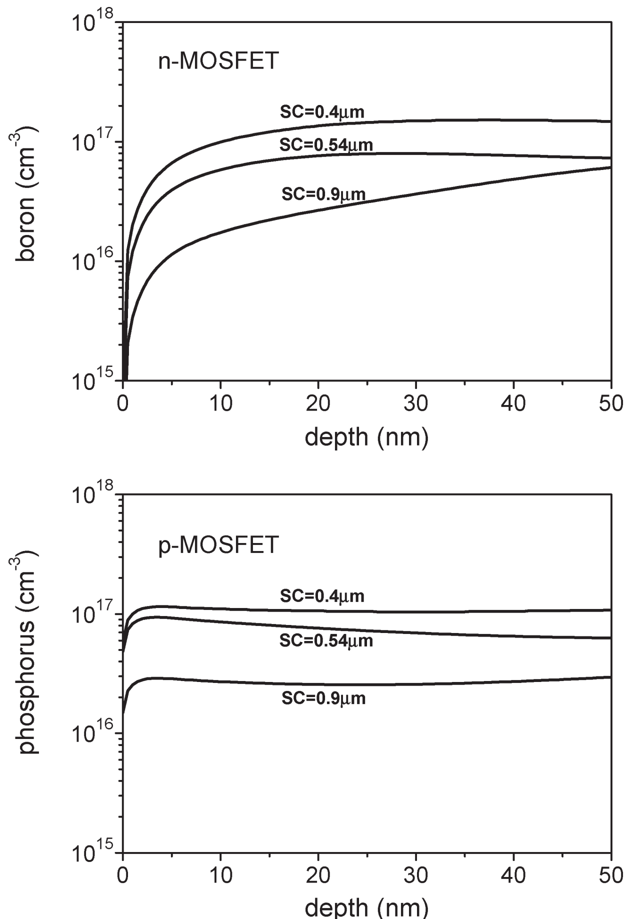

Fig. 4. TCAD-simulated vertical channel dopant profile versus well to gate edge distance SC. The channel dopant concentration increases as the well photoresist edge approaches the MOSFET active area.

introduced by well-edge ion scattering, the average dopant concentrations for the area 20 nm below the MOSFET gate versus SC were plotted in Fig. 5.

The silicon experiment using novel CMOS technology was conducted to explore the well-edge proximity effect. MOSFETs with various well to gate edge distances were designed, fabricated, and electrically measured. The process and device simulations were first calibrated according to a standard MOSFET set, in which the SC is larger than 10 μm. Then, simulations using various SC values were performed to obtain the threshold voltage trend of the MOSFET versus SC. Fig. 6 shows the matched result of silicon experiment and TCAD simulation.

IV. Compact Model for SPICE

Since this new layout-dependent phenomenon increases the threshold voltage and thus decreases the drain current of the MOSFETs, it is especially important for those circuits with high integration density. This effect might also introduce uncertainties to those circuits that are sensitive to the matching of threshold voltage. Therefore, it is necessary to consider this effect in SPICE simulation and postlayout extraction flow. However, the most challenging part of a layout-dependent model is to determine a method of catering for various layout styles in as complete a manner as possible while retaining the efficiency of the procedure.

Fig. 7 shows typical several layout styles of a MOSFET in a well. As shown in Fig. 7(a) and (b), the well edges are close to the MOSFETs in the channel-length direction, and in Fig. 7(c) and (d), the proximity occurs in the channel-width direction. Narrow MOSFETs will have a strong well-edge proximity effect for layouts (c) and (d) as a large portion of the channel

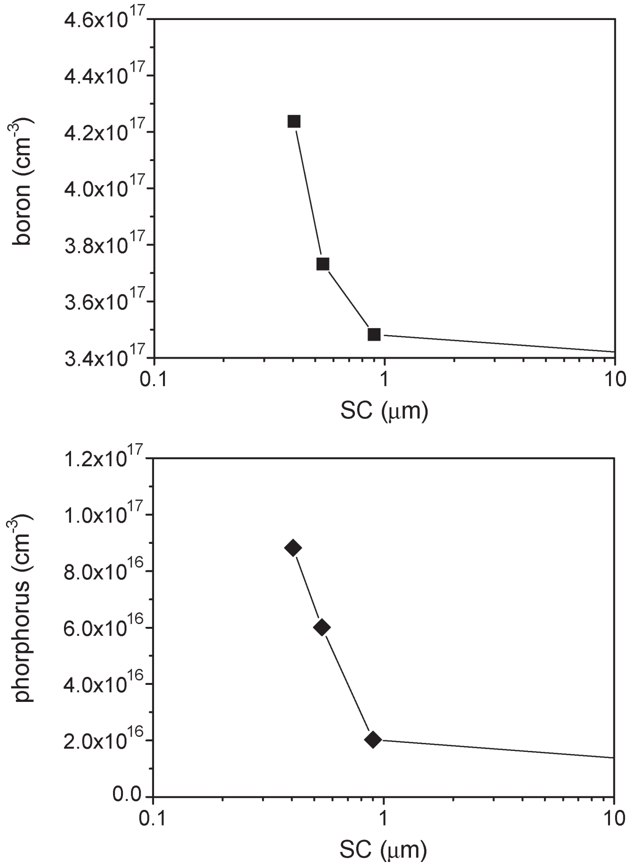

Fig. 5. TCAD-simulated average dopant concentration for the area 20 nm below the MOSFET gate versus SC.

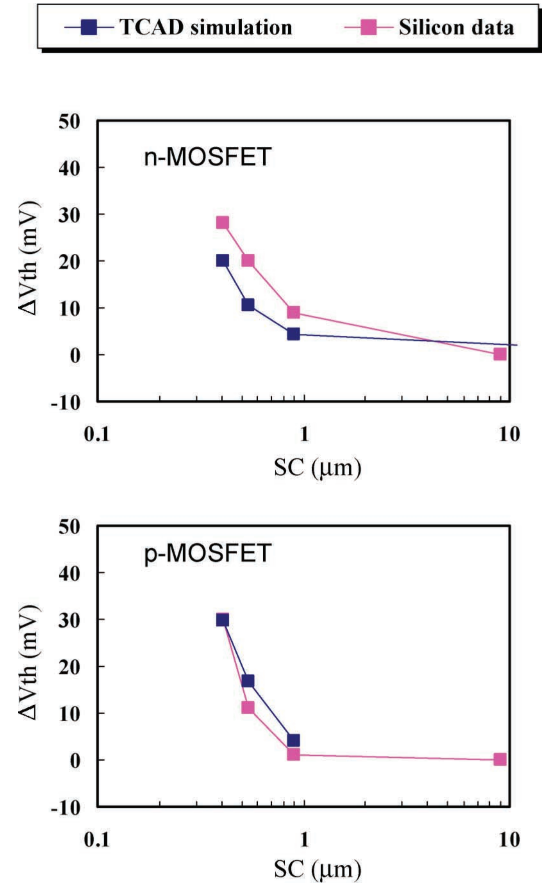

Fig. 6. MOSFET threshold voltage shift versus well to gate edge distance of the silicon experimental and TCAD-simulated results for nMOSFET and pMOSFET. $L_g = 0.216\ \mu$m.

region is influenced by the dopant ion scattering at the well edge. However, the MOSFET channel width does not play an important role in layouts (a) and (b). A useful compact model should cover each of these possibilities.

Fig. 8 shows another generalized example to cover various layout conditions, including those shown in Fig. 7. From Fig. 8, the overall additional dose of dopant introduced by ion scattering at the well edges and that affect the channel region can be represented by the integrals

$$\text{additional_dose} \propto \frac{1}{W_{\text{drawn}} \cdot L_{\text{drawn}}} \cdot \left[\sum_{i=1}^{n} \left(W_i \cdot \int_{\text{SC}_i}^{\text{SC}_i + L_{\text{drawn}}} f(x)dx \right) + \sum_{i=n+1}^{m} \left(L_i \cdot \int_{\text{SC}_i}^{\text{SC}_i + W_{\text{drawn}}} f(y)dy \right) \right] \tag{3}$$

where $f(x)$ is used to account for both lateral and vertical distribution variations of scattered well dopants. In some cases, $f(x)$ might be a combination of several exponential terms. However, our analysis shows that $1/x^2$ is a good approximation for $f(x)$ to cover most conditions. With this approximation, an effective device-to-well-edge distance SC_{eff} is proposed

$$\begin{aligned} \text{SC}_{\text{eff}} &= \left\{ \frac{1}{W_{\text{drawn}} \cdot L_{\text{drawn}}} \cdot \left[\sum_{i=1}^{n} \left(W_i \cdot \int_{\text{SC}_i}^{\text{SC}_i + L_{\text{drawn}}} \frac{1}{x^2} dx \right) + \sum_{i=n+1}^{m} \left(L_i \cdot \int_{\text{SC}_i}^{\text{SC}_i + W_{\text{drawn}}} \frac{1}{y^2} dy \right) \right] \right\}^{-0.5} \\ &= \left\{ \frac{1}{W_{\text{drawn}} \cdot L_{\text{drawn}}} \cdot \left[\sum_{i=1}^{n} \left(W_i \cdot \left(\frac{1}{\text{SC}_i} - \frac{1}{\text{SC}_i + L_{\text{drawn}}} \right) \right) + \sum_{i=n+1}^{m} \left(L_i \cdot \left(\frac{1}{\text{SC}_i} - \frac{1}{\text{SC}_i + W_{\text{drawn}}} \right) \right) \right] \right\}^{-0.5}. \end{aligned} \tag{4}$$

Note that SC_{eff} can easily summarize all the four conditions shown in Fig. 7. A smaller SC_{eff} indicates that the MOSFET

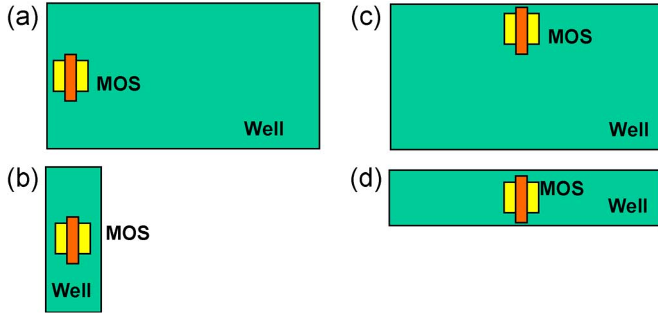

Fig. 7. Typical layouts showing different positions of MOS transistors in a well.

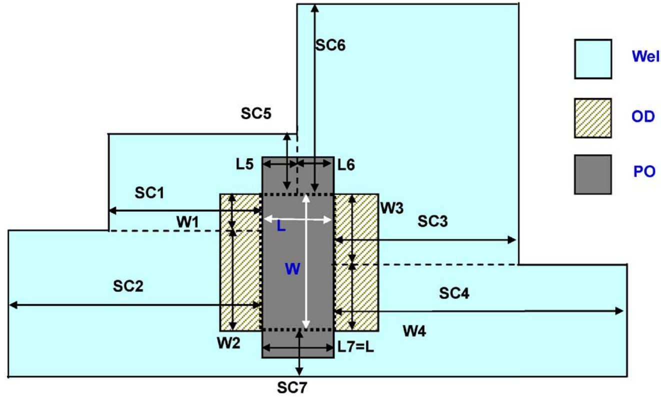

Fig. 8. Schematic presentation of a MOSFET layout and parameters used to establish a well-edge proximity SPICE model.

is closer to the well edge and the well-edge proximity effect will be more severe. Then, the impact of the well-edge proximity effect can be described by adding more SC_{eff}-dependent equations to the conventional model. Since the major effect is due to the MOSFET dopant profile change, three corresponding MOSFET parameters, namely 1) threshold voltage, 2) body effect coefficient, and 3) carrier mobility, are modified to include the variations caused by this effect. The respective equations are

$$\mathrm{Vth0} = \mathrm{Vth0}_{\mathrm{org}} + \mathrm{KVTH0WE} \cdot \left(\frac{1}{\mathrm{SC}_{\mathrm{eff}}^{\mathrm{NWE}} + \mathrm{SC0}^{\mathrm{NWE}}} - \frac{1}{\mathrm{SCREF}^{\mathrm{NWE}} + \mathrm{SC0}^{\mathrm{NWE}}} \right) \tag{5}$$

$$K2 = K2_{\mathrm{org}} + \mathrm{K2WE} \cdot \left(\frac{1}{\mathrm{SC}_{\mathrm{eff}}^{\mathrm{NWE}} + \mathrm{SC0}^{\mathrm{NWE}}} - \frac{1}{\mathrm{SCREF}^{\mathrm{NWE}} + \mathrm{SC0}^{\mathrm{NWE}}} \right) \tag{6}$$

$$\mu_{\mathrm{eff}} = \mu_{\mathrm{eff,org}} \cdot \frac{1 + \frac{\mathrm{KU0WE}}{\mathrm{SC}_{\mathrm{eff}}^{\mathrm{NWE}} + \mathrm{SC0}^{\mathrm{NWE}}}}{1 + \frac{\mathrm{KU0WE}}{\mathrm{SCREF}^{\mathrm{NWE}} + \mathrm{SC0}^{\mathrm{NWE}}}} \tag{7}$$

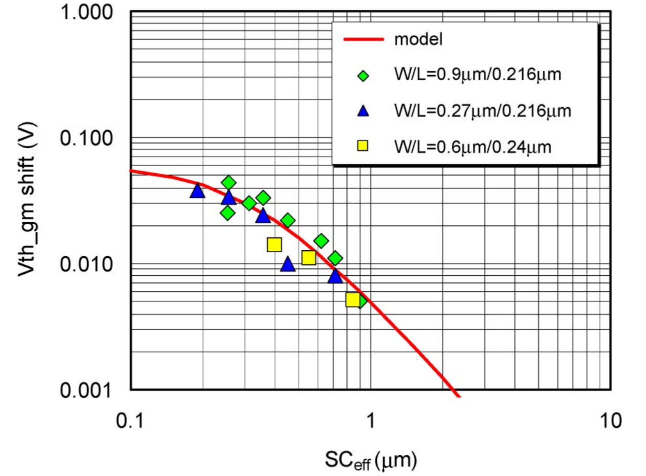

Fig. 9. Model verification results of the MOSFET threshold voltage shift compared to the silicon experiment data.

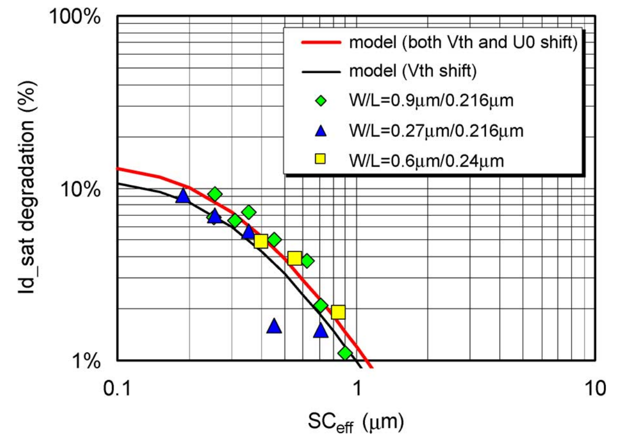

Fig. 10. Model verification results of the MOSFET drive current degradation compared to the silicon experiment data.

where Vth0 is the threshold voltage of the MOSFET, $K2$ is the body effect parameter, and μ_{eff} is the effective carrier mobility. SC_{eff} is the effective distance from the well edge to the channel region, which can be extracted from circuit layouts for each MOSFET by the layout parameter extraction tools using (4). SCREF, SC0, KVTH0WE, K2WE, KU0WE, and NWE are the fitting parameters.

This model has been verified using various types of MOSFET layout patterns, as shown in Fig. 7. Devices with different channel lengths and widths are also considered here in order to check the dependence of the well-proximity effect on W and L. Figs. 9–11 show the comparison between the model and silicon for threshold voltage shift, drive current degradation, and body effect increase of MOS transistors. As shown in these plots, the correlation between the model and silicon is quite reasonable. Note that no matter whether the device is close to the well edge either in the channel length or in the width direction, the concept of SC_{eff} can explain those differences, and thus the data obtained from layouts illustrated in Fig. 7 show the same trend in threshold voltage change (dVth) versus SC_{eff} plot, as indicated in Fig. 9. For those devices with smaller SC_{eff}, the threshold voltage will also increase further, but it may saturate at a certain value.

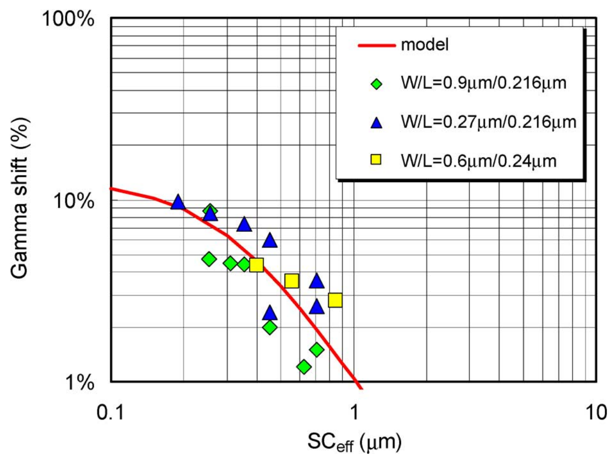

Fig. 11. Model verification results of the MOSFET body effect change compared to the silicon experiment data.

Fig. 10 shows the drive current degradation induced by the well-edge proximity effect. When SC_{eff} becomes smaller, the threshold voltage increases, and thus the drive current will decrease. In addition to the Vth change, our analysis shows that the effective mobility is also degraded by the well-edge proximity effect. This is because impurity scattering becomes more severe as the dopant concentration increases. Fig. 11 demonstrates the dependence of body effect on the well-proximity effect. When SC_{eff} is small, the average doping density in the channel region will increase. Then, the body effect (gamma) will become higher at the same time. The model is able to predict this change.

V. Conclusion

As a result of aggressive CMOS technology scaling MOSFET characteristics have become increasingly layout dependent. In this paper, we have demonstrated the result of a study into the well-edge proximity effect in highly scaled CMOS technology from the ion scattering perspective. Ion scattering models and TCAD simulations provide an internal view of the influence of this effect on MOSFET. Additional SPICE models were established based on the physical understanding observed from the TCAD simulation and verified using the results from specially designed silicon experiment.

Acknowledgment

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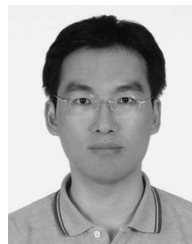
Yi-Ming Sheu was born in Hsinchu, Taiwan, R.O.C., in 1968. He received the B.S. degree in material science and engineering from the National Cheng Kung University, Tainan, Taiwan, in 1991 and the M.S. degree in optical science from the National Central University, Taoyuan, Taiwan, in 1996. He is currently working toward the Ph.D. degree in the Department of Electronics Engineering, National Chiao Tung University, Hsinchu.

In 1997, he joined the Taiwan Semiconductor Manufacturing Company, Hsinchu, and is currently engaged in advanced CMOS device design.



Ke-Wei Su was born in Tainan, Taiwan, R.O.C, on February 23, 1973. He received the B.S.E.E. and Ph.D.E.E. degrees from the National Taiwan University, Taipei, Taiwan, in 1994 and 1998, respectively.

In 2001, he joined the SPICE group of the Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan. His current focus is on the compact modeling of MOSFETs for both bulk and silicon-on-insulator (SOI) technologies.

Shiyang Tian received the B.S. degree in physics/optics from Shandong University, Jinan, China, in 1987, and the M.S. and Ph.D. degrees in electrical and computer engineering from The University of Texas at Austin, in 1994 and 1997, respectively.

Upon graduation, he joined Technology Modeling Associates (now part of Synopsys, Inc., Dallas, TX) working on the semiconductor process modeling, where he developed an accurate and versatile Monte Carlo implant simulator (Taurus MC), which is now integrated into Synopsys TCAD simulation tools TSUPREM-4, Taurus-Process, and Sentaurus-Process. He has authored or co-authored more than 40 publications in journals and conference proceedings.

Sheng-Jier Yang was born in Taipei, Taiwan, R.O.C., in 1964. He received the B.S. degree from Tatung Institute of Technology, Taipei, in 1987, the M.S. degree from the National Central University, Taoyuan, Taiwan, in 1989, and the Ph.D. degree from the Arizona State University, Phoenix, in 2000, all in chemical engineering.

From 2000 to 2002, he was a Device Engineer with PowerOn Technologies, Inc., Phoenix, AZ, where he was worked on optimizing discrete power MOSFETs for application voltages ranging from 20 to 800 V. Since 2002, he has been with Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan. His current focus is on characterizing strain-induced impact on advanced MOSFET and its layout dependence.

Chih-Chiang Wang (M'03) received the B.S. degree in physics science from the Catholic Fu Jen University, Hsien, Taiwan, R.O.C., in 1989 and the M.S. degree in electrooptical engineering from the National Chiao Tung University, Hsinchu, Taiwan, in 1991.

In 1991, he was with the Electronics Research and Service Organization (ERSO/ITRI) and worked on 0.7- and 0.5-μm DRAM devices design and 0.25 logic devices development. In 1998, he joined the Taiwan Semiconductor Manufacturing Company, Hsinchu. Since 2001, he has been the Manager of TCAD Team, Taiwan Semiconductor Manufacturing Company, and is responsible for process and device calibration/simulation. His works primarily focused on aggressive CMOS technology and the related models development. Recently, he focused on fundamental model investigation and development in line with aggressive CMOS technology development.

Ming-Jer Chen (S'84–M'85–SM'98) received the B.S. degree in electrical engineering (with highest honors) from the National Cheng Kung University, Tainan, Taiwan, R.O.C., in 1977, and the M.S. and Ph.D. degrees in electronics engineering from the National Chiao Tung University (NCTU), Hsinchu, Taiwan, in 1979 and 1985, respectively.

In 1985, he joined the faculty of the Department of Electronics Engineering, NCTU. From 1987 to 1992, he was a Consultant with the Taiwan Semiconductor Manufacturing Company, Hsinchu, where he led a team from NCTU and Electronics Research and Service Organization (ERSO/ITRI) to build up a series of process windows and design rules. Since 1993, he has been a Full Professor with NCTU. From 2000 to 2001, he was a Visiting Professor with the Department of Electrical Engineering and the Center for Integrated Systems, Stanford University, Stanford, CA. He has graduated 14 Ph.D. students and more than 80 Master's students. He has been granted six US patents and six Taiwanese patents covering high-precision analog capacitors, 1-T SRAM cell, dynamic threshold MOS, and electro-static discharge (ESD) protection. His research interests have long been focused on the device physics and currently on nanoscale electronics.

Dr. Chen is a member of Phi Tau Phi.

Sally Liu received the B.S. degree in physics and the M.S. degree in applied physics from the National Tsing Hua University, Hsinchu, Taiwan, R.O.C., and the Ph.D. degree in electrical engineering and computer science from the University of California, Berkeley.

She spent 15 years with AT&T Bell Laboratories, six years with Conexant/Rockwell Semiconductors, and two years with RFIC. Since 2004, she has been the Director of the Advanced Technology Modeling Division with Taiwan Semiconductor Manufacturing Company, Hsinchu. She has been engaged in the research and development of device modeling and simulation, circuit simulation and optimization, statistical modeling and design centering, circuit verification, IP characterization, and electronic design automation (EDA) framework.