Self-Substrate-Triggered Technique to Enhance Turn-On Uniformity of Multi-Finger ESD Protection Devices

Ming-Dou Ker, *Senior Member, IEEE*, and Jia-Huei Chen

***Abstract*—A novel self-substrate-triggered technique for on-chip ESD protection design is proposed to solve the non-uniform turn-on phenomenon of multi-finger gate-grounded nMOS (GGnMOS). The center-finger nMOS transistors in the multi-finger GGnMOS structure are always turned on first under ESD stress, so its source terminal is connected to the base (substrate) terminals of the other parasitic lateral n-p-n bipolar transistors (BJTs in the GGnMOS structure) to form the self-substrate-triggered design. With the proposed self-substrate-triggered technique, the first turned-on center-finger nMOS transistors are used to trigger on the others. Therefore, all fingers of GGnMOS can be triggered on simultaneously to discharge ESD current. From the experimental results verified in a 0.13-μm CMOS process with the thin gate oxide of 25 Å, the turn-on uniformity and ESD robustness of the GGnMOS can be greatly improved without increasing extra layout area through the proposed self-substrate-triggered technique.**

***Index Terms*—Electrostatic discharge (ESD), multi-finger gate-grounded nMOS, non-uniform turn-on phenomenon, self-substrate-triggered technique.**

I. Introduction

WITH THE PROCESS evolution, the device size is continually scaled down and the salicided process used to improve the operating speed of CMOS ICs. However, the electrostatic discharge (ESD) robustness of devices in the advanced CMOS technology becomes inferior. To sustain a reasonable ESD robustness in nanoscale CMOS ICs, on-chip ESD protection circuits must be added into the chips [1]. The typical ESD levels of general commercial IC products are 2 kV in human-body-model (HBM) ESD test and 200 V in machine-model (MM) ESD test [2]. To sustain the required ESD levels, ESD protection devices are often designed with large device dimensions, which are often drawn with the multi-finger layout style to reduce the total occupied silicon area [3]. Typically, multi-finger gate-grounded nMOS (GGnMOS) devices are widely used as ESD protection structures owing to the effectiveness of parasitic lateral n-p-n BJT in handling high ESD current. However, it has been reported that multi-finger GGnMOS can not be uniformly turned on under ESD stress [4]–[7]. That is, even if a larger multi-finger GGnMOS is used as the ESD protection device, uniform conduction of all fingers is hard to achieve, and hence the expected ESD level can not be realized [7]. The following is the mechanism that results in non-uniform turn-on phenomenon of multi-finger GGnMOS.

In the multi-finger GGnMOS structure with P+ guard ring surrounding it, due to the different distances from the base regions of each parasitic lateral n-p-n BJT to the substrate guard ring, the base resistance of parasitic lateral n-p-n BJT in the central region of the multi-finger GGnMOS is higher than those in the side regions. Therefore, in the multi-finger GGnMOS structure, the center nMOS fingers are always triggered on faster than the others under ESD stress. As long as the center nMOS fingers are triggered on, the ESD overstress voltage is clamped to the snapback holding voltage of nMOS. Moreover, if the secondary breakdown voltage (Vt2) of GGnMOS is smaller than its trigger voltage (Vt1), the other non-turned-on nMOS fingers in the side region cannot be triggered on before the first turned-on nMOS fingers are burned out [5]. Therefore, the ESD current will be only discharged through some local regions. Thus, ESD robustness of multi-finger GGnMOS cannot be efficiently increased by increasing the device dimension. To solve this problem, some circuit designs such as gate-coupled [8]–[12] or substrate-triggered [13]–[16] techniques have been proposed to reduce the trigger voltage (Vt1) of GGnMOS for improving the turn-on uniformity of multi-finger GGnMOS.

In this work, a novel self-substrate-triggered GGnMOS (SST_GGnMOS) is proposed to solve the non-uniform turn-on issue of multi-finger GGnMOS and improve its ESD robustness. The proposed SST_GGnMOS has been successfully verified in a 0.13-μm CMOS process [17].

II. Prior Designs to Enhance Turn-On Uniformity of GGnMOS

A. Layout Skill

In the traditional layout style of multi-finger GGnMOS, the difference in the base resistance of each parasitic BJT is a main reason to cause non-uniform turn-on phenomenon. Fig. 1 shows a layout style that can make the base resistance of each parasitic lateral n-p-n BJT in the multi-finger GGnMOS approximately equal, which is implemented by inserting a P+ diffusion region adjacent to the source terminals of each finger nMOS transistor [18]. With the equal base resistance, all parasitic lateral n-p-n BJTs can be triggered on simultaneously to discharge ESD current. However, the layout area is greatly increased by the insertion of P+ diffusion region into each source region. Also, such a layout style is strictly prohibited in the deep-submicron CMOS

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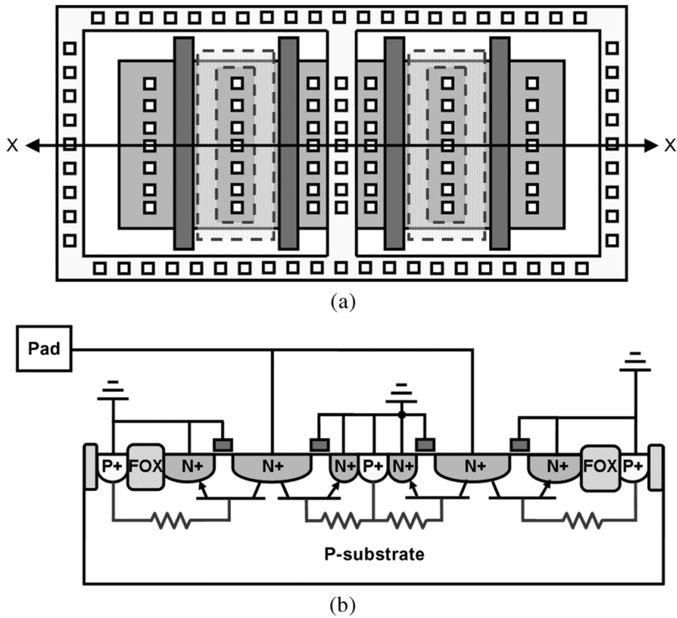


Fig. 1. (a) The layout top-view and (b) the X-X′ cross-sectional view of the layout skill that makes the base resistance of each parasitic BJT approximately equal by inserting a P+ diffusion adjacent to the source terminal of each finger nMOS transistor [18].

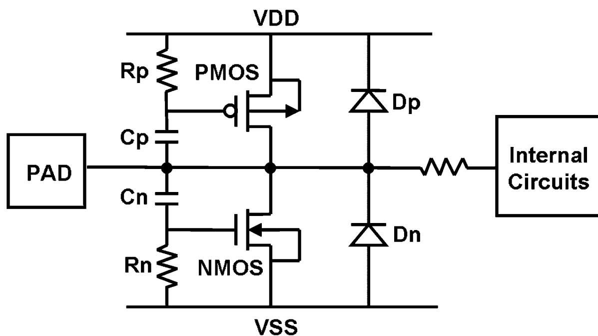


Fig. 2. ESD protection circuit with gate-coupled technique [8].

processes, because the substrate resistance of each finger nMOS drawn in this layout style becomes so small that all parasitic lateral n-p-n BJTs in the nMOS fingers are hard to be triggered on quickly to protect the thin gate-oxide of internal circuits [19].

B. Gate-Coupled Technique

Fig. 2 shows the ESD protection circuit with gate-coupled technique [8]. The nMOS/pMOS is configured with its drain connected to the input pad and its source connected to the VSS/VDD. A capacitor is connected between the input pad and the gate of nMOS/pMOS transistor. A resistor is connected between the VSS/VDD and the gate of nMOS/pMOS transistor. By tuning the resistance and capacitance, a suitable voltage can be coupled to the gate of nMOS/pMOS only under the high-voltage ESD stress condition, thus lowering the trigger voltage of nMOS/pMOS. The non-uniform turn-on issue of large-sized multi-finger nMOS can be overcome through the gate-coupled technique. However, the higher gate bias coupled to nMOS/pMOS will induce more channel current and higher electric field to rupture the thin gate oxide of nMOS/pMOS.

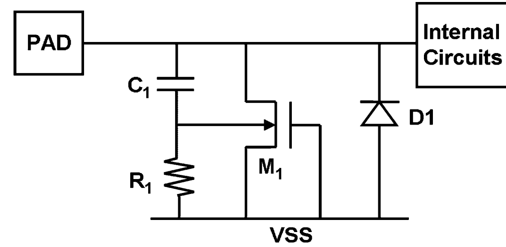


Fig. 3. ESD protection circuit with substrate-triggered technique [13].

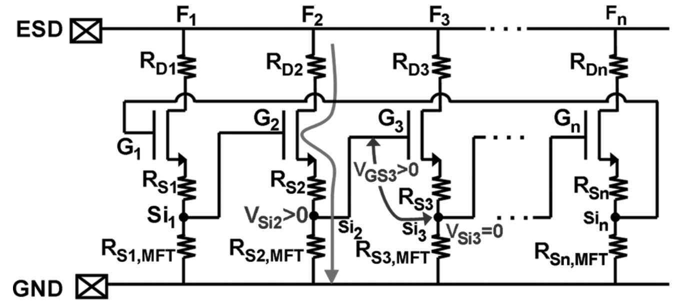


Fig. 4. Equivalent circuit of domino-type multi-finger turn on (source-gate-coupled) nMOS for subsequent finger triggering indicating the function of the device [20].

Therefore, the ESD robustness of ESD protection device will be suddenly degraded at higher coupled gate bias during ESD stresses, i.e. over-gate-driven effect [5], [10]–[12]. Gate-coupled ESD protection circuit must be carefully designed and optimized to avoid the sudden degradation on ESD level.

C. Substrate-Triggered Technique

One ESD protection circuit with substrate-triggered technique is shown in Fig. 3 [13]. The capacitance and resistance must be tuned for coupling a suitable voltage to the body of parasitic lateral n-p-n BJT (or the substrate of GGnMOS) only under ESD stress condition to lower the trigger voltage of GGnMOS, which can improve the turn-on uniformity of GGnMOS.

As compared with the gate-coupled design, the substrate-triggered technique is to increase the base voltage of the parasitic BJT, thus avoiding the channel current and the overstress across the gate oxide. Therefore, the substrate-triggered technique can continually improve ESD robustness of the ESD protection devices without the sudden degradation as that in the gate-coupled design. The substrate-triggered design can safely and effectively improve the ESD robustness of ESD protection devices [5], [14], [15].

D. Multi-Finger Turn-On Technique

Fig. 4 depicts the domino-type multi-finger turn-on technique [20] to solve the non-uniform turn-on issue of GGnMOS, where the $\mathrm{R_{Dn}/R_{Sn}}$ is the drain/source ballast resistor. The resistor $\mathrm{R_{Si,MFT}}$ in each finger nMOS transistor is used to generate a voltage bias to the adjacent gate. After one arbitrary finger is triggered on as indicated by the arrow at finger $\mathrm{F_2}$, the initial ESD current flows through resistor $\mathrm{R_{S2,MFT}}$ and builds up a potential $\mathrm{V_{Si2}}$ to bias the nMOS gate of finger $\mathrm{F_3}$. Therefore, the

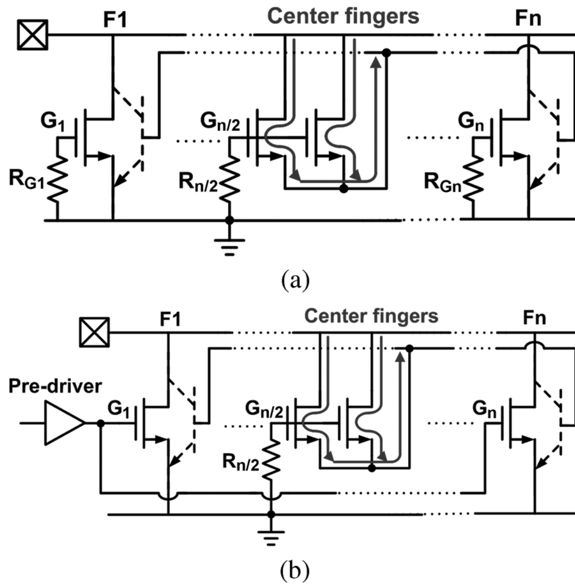


Fig. 5. The equivalent circuits of the self-substrate-triggered GGnMOS (SST_GGnMOS) for on-chip ESD protection design for (a) the input pad to VSS and (b) output pad to VSS.

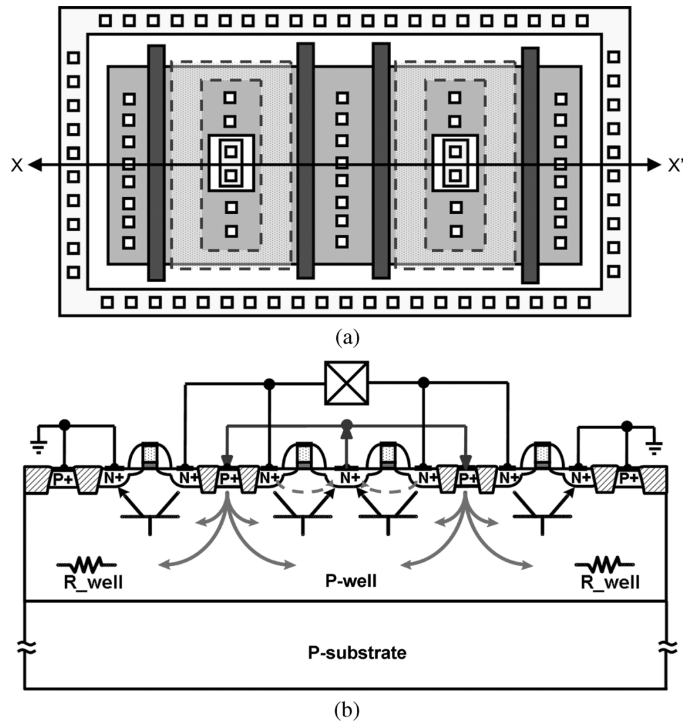


Fig. 6. (a) The layout top view and (b) the X-X′ cross-sectional view of the SST_GGnMOS. The P+ diffusion regions inserted to the drain of each finger as the substrate-triggered nodes are connected to the source terminal of the center-finger nMOS transistors.

parasitic BJT inherent in the finger F_3 can be triggered on due to the well-known gate-coupled effect. The same mechanism transfers the internal source signal at Si_3 to the gate of finger F_4, thus triggering the finger F_4. Through this domino effect of subsequently triggered fingers, the entire fingers in the GGnMOS structure are eventually forced into a homogenous conduction state [20]. The values of the resistors in this circuit should be designed appropriately to achieve the expected results, and the layout realization is more complicated.

III. Self-Substrate-Triggered Technique

There are two main issues those responsible for the non-uniform turn-on problems of multi-finger GGnMOS. One is that the parasitic lateral n-p-n BJTs of center fingers usually have the largest substrate (base) resistance under traditional layout style, which makes the center-finger nMOS transistors be triggered on earlier. The other is the obvious snapback characteristics of the parasitic lateral n-p-n BJT inherent in nMOS, which makes the first turned-on center fingers solely sustain the high ESD current. In this work, the above-mentioned characteristics that originally lead to non-uniform turn-on phenomenon will be used to improve the turn-on uniformity of multi-finger GGnMOS.

The proposed self-substrate-triggered GGnMOS (SST_GGnMOS) just utilizes the current of the first turned-on center nMOS fingers as the substrate-triggered current for promoting the turn-on uniformity among the fingers. The equivalent circuits of SST_GGnMOS for on-chip ESD protection designs of the input and output pads to VSS are shown in Fig. 5(a) and (b), respectively. The configurations are similar to the traditional multi-finger GGnMOS, except that the source of the center-finger nMOS transistors is connected to the parasitic bipolar base terminals of all the other fingers instead of connecting to ground. For the output ESD protection application in Fig. 5(b), the gates of the center-finger nMOS transistors are connected to ground instead of the pre-driver to avoid disturbance of normal circuit function. While ESD pulse is applied to the I/O pad, the center-finger nMOS transistors are turned on first and then the current flows from the center fingers to the bases of all the other parasitic lateral n-p-n BJTs. The current from the center-finger nMOS transistors will result in a voltage drop across the substrate (base) resistor to elevate the voltage of base terminals, which will make the parasitic n-p-n lateral BJTs turn on more efficiently to discharge ESD current and thus improve ESD levels.

Fig. 6(a) and (b) shows the layout top view and cross-sectional view of SST_GGnMOS, respectively. The layout is realized by inserting the P+ diffusion regions in the drain of each finger nMOS transistor as the substrate-triggered nodes. The source terminal of the center-finger nMOS transistors is connected to these substrate-triggered nodes. Because the drain area is usually larger than its source area in the layout of multi-finger GGnMOS with silicide blocked region, inserting the P+ triggered nodes does not increase the total layout area. Besides, no additional masks (such as ESD implantation [21]) and external triggering circuits are needed in the proposed self-substrate-triggered GGnMOS. That is, ESD level can be improved without increasing the layout area and fabrication cost through the self-substrate-triggered technique.

IV. Experimental Results

The novel SST_GGnMOS has been realized in a 0.13-μm CMOS process with gate-oxide thickness of 25 Å. To guarantee that the center-finger nMOS transistors can be turned on first to trigger on the others, the channel lengths of the center-finger nMOS transistors (Lcf) are drawn with the minimum rule of

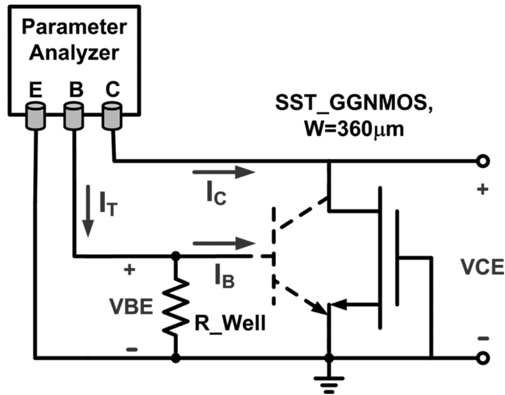


Fig. 7. The experimental setup and definitions of the current and voltage components to measure the DC characteristics of the SST_GGnMOS with channel width of 360 μm.

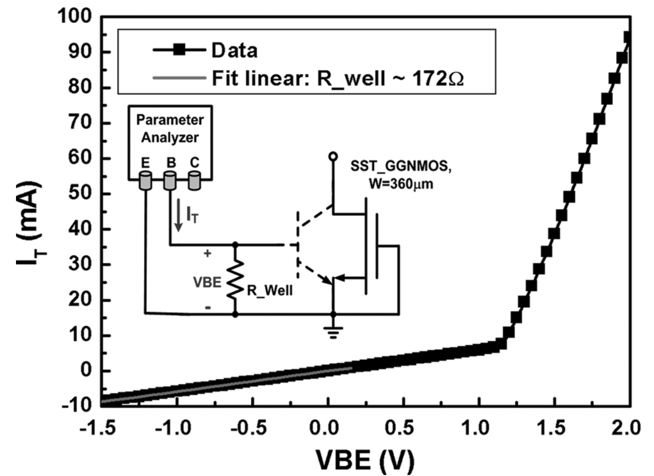


Fig. 8. The measured base-to-emitter DC *I-V* curve of the SST_GGnMOS with channel width of 360 μm, when the collector is open circuit.

0.13 μm, whereas those of the other fingers are drawn with 0.18 μm in the SST_GGnMOS structure. The traditional multi-finger GGnMOS with all channel lengths of 0.18 μm is also fabricated in the same chip for comparison. Each finger width of these two devices is kept as 30 μm, and the maximum finger number is as many as 20. Both of traditional GGnMOS and the proposed SST_GGnMOS have silicide blocked region on their drain sides. After silicon fabrication, the DC characteristics of the SST_GGnMOS device are measured by the parameter analyzer (HP 4156B). The automatic transmission line pulsing (TLP) system [22], [23], the human-body-model (HBM), and the machine-model (MM) ESD testers are used to verify the ESD levels of the traditional GGnMOS and the new-proposed SST_GGnMOS. The Emission Microscope (EMMI) is used to distinguish the turn-on behaviors between the new proposed SST_GGnMOS and the traditional GGnMOS.

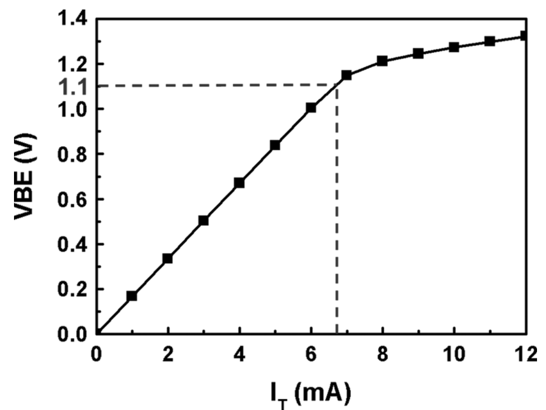


Fig. 9. The relation between the substrate-triggered current and the corresponding base-to-emitter voltage (VBE) under VCE of 1.2 V.

A. Characteristics of the SST_GGnMOS

To investigate the characteristics of SST_GGnMOS, the layout of the SST_GGnMOS with $\mathrm{W/L} = 360\ \mu\mathrm{m}/0.18\ \mu\mathrm{m}$ ($\mathrm{Lcf} = 0.13\ \mu\mathrm{m}$) is slightly modified in the test chip. The source of the center fingers is not connected to the P+ triggered nodes but connected to ground. The P+ triggered nodes are connected outward to a bond pad as the base terminal of the parasitic BJT inherent in the SST_GGnMOS structure. Fig. 7 shows the experimental setup and the definitions of the current and voltage components in this measurement. The parameter analyzer (HP 4156B) is used to measure the DC characteristics of the SST_GGnMOS. The equivalent P-well resistance inherent in the P+ trigger nodes to the P+ substrate guard ring is denoted as R_well. The applied current into the P+ triggered node is denoted as IT and the current into the base-to-emitter (B-E) junction is denoted as $\mathbf{I}_{\mathrm{B}}$ in Fig. 7.

The measured base-to-emitter DC *I-V* curve of the SST_GGnMOS with channel width of 360 μm is shown in Fig. 8. The inset shows the experimental setup. The collector terminal of the parasitic lateral n-p-n BJT is floating, and a voltage is applied to the base and emitter terminals to investigate the characteristics of the B-E junction diode. As shown in Fig. 8, the B-E junction diode is in parallel with an inherent P-well resistance (R_well) of $\sim$ 172 Ω, and the B-E junction diode does not dominate the *I-V* characteristics until the base-to-emitter voltage (VBE) is larger than 1.1 V. That is, the voltage drop across the effective P-well resistance must be $\sim$1.1 V to turn the parasitic lateral BJT "on" by forward biasing the base-to-emitter junction. The relation between the substrate-triggered current and the corresponding value of VBE under the condition of $\mathrm{VCE} = 1.2$ V is shown in Fig. 9. For the substrate-triggered current between 0 mA and 6 mA, VBE is smaller than 1.1 V, so the R_well dominates the *I-V* characteristics and the base-to-emitter voltage (VBE) increases linearly with the substrate-triggered current ($\mathbf{I}_{\mathrm{T}}$) as expected. The substrate-triggered current must be greater than $\sim$7 mA to make the base-to-emitter voltage higher than 1.1 V, as indicated by the dotted line in Fig. 9.

The relation between the current gain of parasitic lateral n-p-n BJT in the SST_GGnMOS structure ($\mathrm{W} = 360\ \mu\mathrm{m}$) and the substrate-triggered current under the measured conditions of

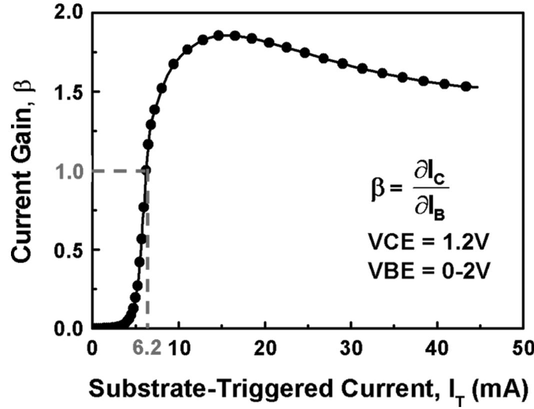


Fig. 10. The relation between the current gain of parasitic lateral n-p-n bipolar transistor inherent in the SST_GGnMOS and the substrate-triggered current under VCE of 1.2 V and VBE from 0 to 2 V.

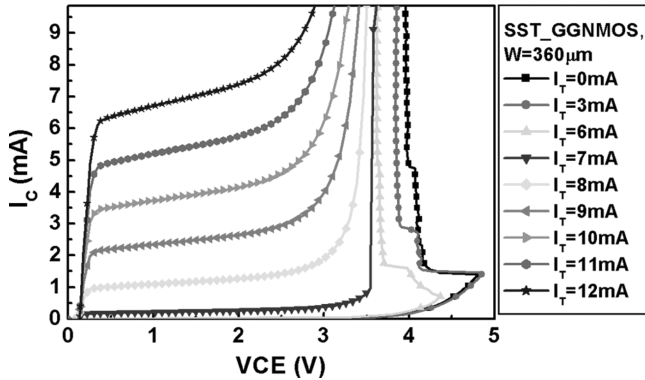


Fig. 11. The measured DC *I-V* curves of the SST_GGnMOS with channel width of 360 μm under different substrate-triggered currents.

VCE = 1.2 V and VBE = 0-2 V is shown in Fig. 10. The base current I_B is calculated as

$$I_B = I_T - \frac{\text{VBE}}{\text{R_well}} \tag{1}$$

where R_well is the equivalent P-well resistance inherent in the SST_GGnMOS structure. The current gain is defined as the differential value of I_C to I_B. As indicated by the dotted line in Fig. 10, the substrate-triggered current must be larger than 6.2 mA for the current gain of the parasitic lateral n-p-n BJT to be greater than unity, which is the key factor of effective conduction of parasitic lateral n-p-n BJT.

The measured DC *I-V* curves of SST_GGnMOS device under different substrate-triggered currents $(\mathbf{I}_T)$ are shown in Fig. 11. When the substrate-triggered current injected at the P+ triggered nodes is increased from 0 mA to 6 mA, the trigger voltage of the SST_GGnMOS device is only reduced slightly from 4.8 V to 4.4 V, and the SST_GGnMOS still goes through snapback region. On the contrary, when the substrate-triggered currents are above 7 mA, the parasitic BJT is initially turned on and the SST_GGnMOS device can conduct high current without the snapback mechanism. From the above experimental results, it is concluded that the substrate-triggered current must be greater than ~7 mA to achieve the substrate-triggered effect for the SST_GGnMOS with channel width of 360 μm in this testchip.

B. Substrate-Triggered Current Provided by the Center Fingers

As shown in Fig. 12(a), to observe the substrate-triggered current provided by the center fingers, the voltage pulses with different pulse amplitudes generated by the 100-ns TLP system are applied to the drain terminal of the SST_GGnMOS with channel width of 360 μm. The pulse width generated by the TLP system is as short as 100 ns to simulate the ESD condition. With the specially drawn testchip, the source of the center-finger nMOS transistors and the source of the others are separately connected to different bond pads, and then wired to each other with a current probe on it for measuring the transient current generated by the center fingers. As shown in Fig. 12(b) and (c), the measured substrate-triggered currents provided by the center fingers are as large as 20 mA and 180 mA under the applied 0-to-5 V and 0-to-30 V TLP voltage pulses, respectively. The measured current waveform shows that the center fingers are turned on under TLP pulses and can quickly generate substrate-triggered currents. Fig. 12(d) shows the relation between the TLP voltage magnitude and the substrate-triggered current provided by the center fingers (Icf). When the magnitude of the TLP voltage pulse is smaller than the trigger voltage of the center fingers (~4.8 V), the center fingers are not turned on, thus the triggered current is zero for TLP voltage from 1 V to 4 V. As long as the TLP voltage is larger than the trigger voltage of the center fingers, the center fingers are turned on to provide substrate-triggered current much larger than 7 mA. That is, the center fingers can provide adequate substrate-triggered current to effectively promote turn-on uniformity of SST_GGnMOS. To further reduce the trigger voltage of center fingers, the gate-coupled technique (with a small capacitance from the pad to the gate of center fingers) can be added into this SST_GGnMOS. Such a small capacitance can be realized by the overlap metal layers under the bond pad, therefore the overall layout area of I/O cell is still kept the same.

In reality, the source of the center fingers is connected to the substrate-triggered nodes in the SST_GGnMOS structure. Thus, the current of the center fingers will flow through the inherent resistor R_well to create a voltage drop between the base and emitter terminals and to trigger on the other fingers. As long as the other fingers are triggered on, the center fingers would be suppressed to turn off because the voltage potential between the base and emitter terminals of the center fingers becomes approximately zero.

C. TLP Measurement Results

The TLP system provides a single and continually-increasing-amplitude pulse to the device under test, and the pulse width is as short as 100 ns to simulate the ESD condition. By using the TLP measurement, the snapback characteristics and the secondary breakdown currents (It2) of the devices can be investigated. It2 is the index for HBM ESD robustness, which is indicated as the corresponding current when the leakage current under the voltage bias of 1.2 V is above 1 μA in this work. The relation between It2 and HBM ESD level (V_{ESD}) can be approximated as $V_{ESD} \cong \text{It2} \times 1.5\ \text{k}\Omega$, where 1.5 k$\Omega$ is the equivalent resistance of human body.

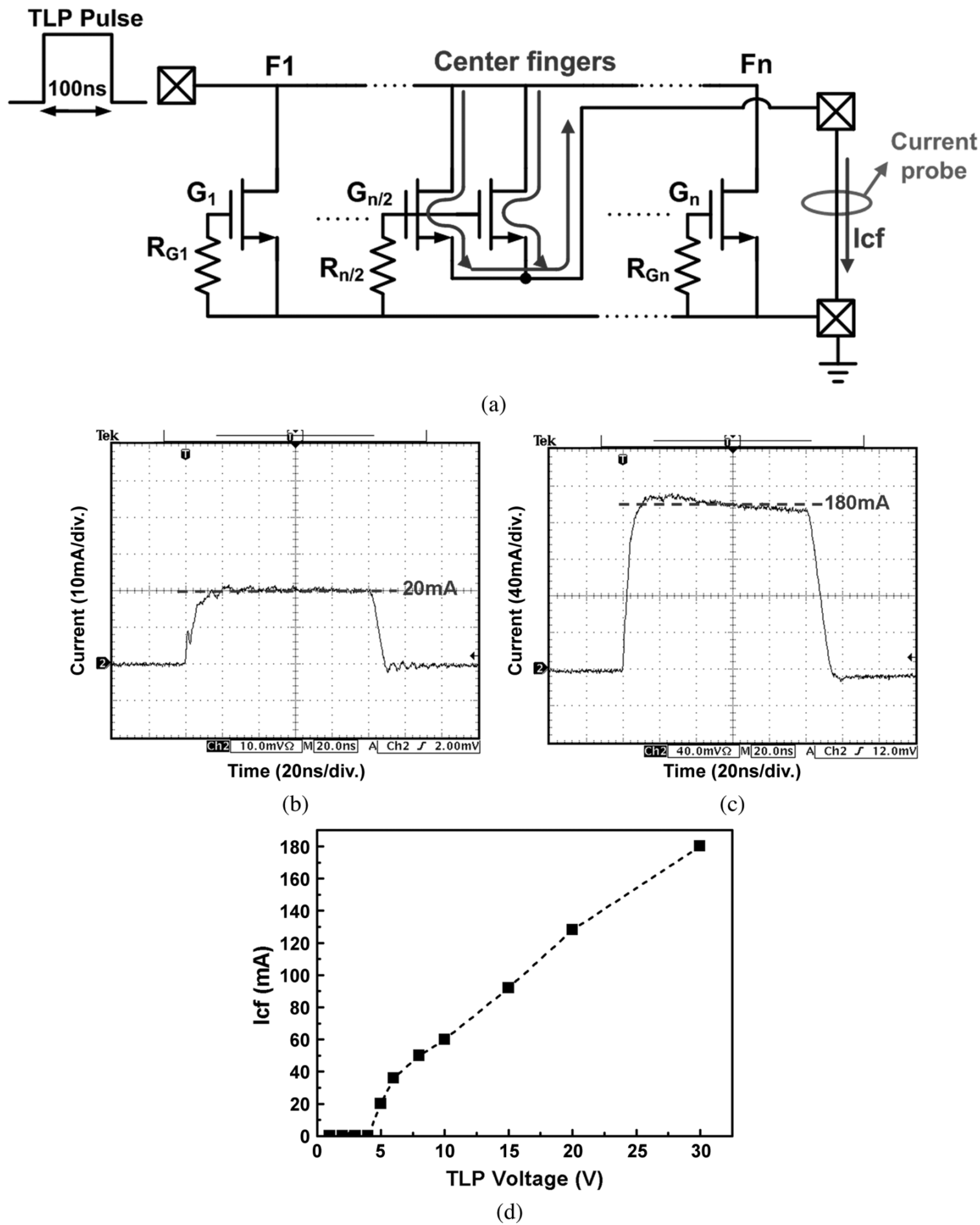


Fig. 12. (a) The measurement setup to observe the substrate-triggered current provided by the center fingers. The substrate-triggered current waveforms under the TLP pulse magnitude of (b) 5 V and (c) 30 V. (d) The relation between the TLP voltage magnitude and the substrate-triggered current provided by the center fingers (Icf).

Fig. 13(a) and (b) shows the TLP-measured *I-V* curves and the corresponding leakage currents of the traditional GGnMOS and the SST_GGnMOS under different channel widths, respectively. In the SST_GGnMOS structure, the center fingers with shorter channel length will go through snapback region first. Therefore, in Fig. 13(b), the SST_GGnMOS still have obvious snapback characteristics like the traditional GGnMOS as shown in Fig. 13(a). The It2 of GGnMOS and SST_GGnMOS both increase with channel width, but the It2 of the SST_GGnMOS (3.5 A) is greater than that of traditional GGnMOS (2.9 A) under the same device size (channel width of 480 μm). To more clearly distinguish between these two devices, the dependence of It2 per unit channel width on device total channel width is shown in Fig. 13(c).

In Fig. 13(c), the It2 per unit channel width of traditional GGnMOS decreases from 7.4 mA/μm to 5.8 mA/μm when the channel width increases from 240 μm to 480 μm. In Fig. 13(c), the It2 of traditional GGnMOS cannot increase linearly with channel width, which is due to the non-uniform turn-on issue among the multiple fingers of large-sized GGnMOS. On the contrary, the It2 per unit channel width of the SST_GGnMOS remains higher than 7.4 mA/μm as the channel width increases to 600 μm. Moreover, when the device channel width increases, the It2 per channel width is still almost kept the same (with only a little degradation) in the SST_GGnMOS. This implies that the turn-on uniformity can be effectively achieved by the proposed self-substrate-triggered technique. From these experimental results, the It2 of the proposed SST_GGnMOS has better width

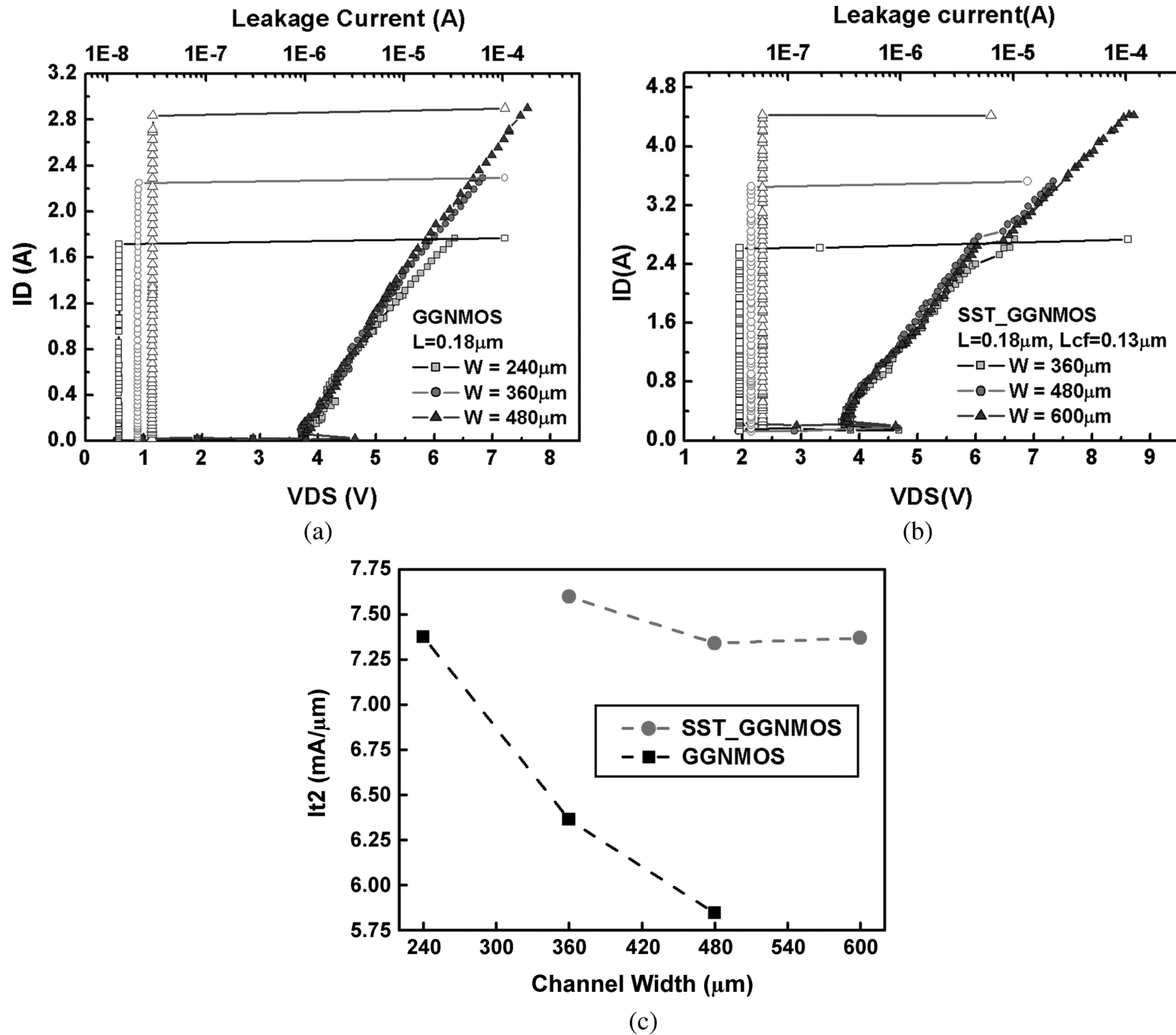


Fig. 13. The TLP-measured *I-V* curves of (a) the traditional GGnMOS and (b) the SST_GGnMOS under different channel widths, including the corresponding leakage currents under the drain voltage bias of 1.2 V. (c) The comparison of It2 per micron between the traditional GGnMOS and the proposed SST_GGnMOS under different channel widths.

scalability, and the SST_GGnMOS can sustain more ESD current than that of traditional GGnMOS under the same layout area.

D. ESD Robustness

The HBM and MM ESD stresses are applied to the ESD protection devices to verify their ESD robustness. In these ESD verifications, the devices are tested under the positive-to-VSS ESD stress, and the failure criterion is defined as the measured voltage at the current level of 1 μA shifted 30% from its original value. The comparison of the ESD levels between the traditional GGnMOS and the SST_GnMOS is shown in Fig. 14. In Fig. 14, under the same device dimension (channel widths of 360 μm and 480 μm), the HBM ESD level of the SST_GGnMOS is two times larger than that of traditional GGnMOS. When the device channel width is increased, the HBM ESD level of the SST_GGnMOS is increased considerably, however, that of GGnMOS is only increased a little. The experimental results show that the HBM ESD level can be greatly improved through the self-substrate-triggered technique, which is consistent with the TLP measurement results (higher It2 leads to higher HBM ESD level). However, in the experimental results, the correlation between It2 and HBM ESD levels of traditional GGnMOS and SST_GGnMOS is somewhat different. When the process moves to deep-submicron scale, the correlation between It2 and HBM ESD level will be changed. Under process splits and circuit splits, some significant differences in TLP measurement and HBM ESD test had been observed in a 0.13-μm CMOS process [24].

Fig. 15 shows the relation between the device channel widths and the MM ESD levels of GGnMOS and SST_GGnMOS. For the traditional GGnMOS, even the device channel width increases to 480 μm, the MM ESD level (only 100 V) is still below the typical commercial specification of 200 V. But, the MM ESD levels of the proposed SST_GGnMOS are 200 V, 250 V, and 375 V for device channel widths of 360 μm, 480 μm, and 600 μm, respectively. The experimental results of HBM and

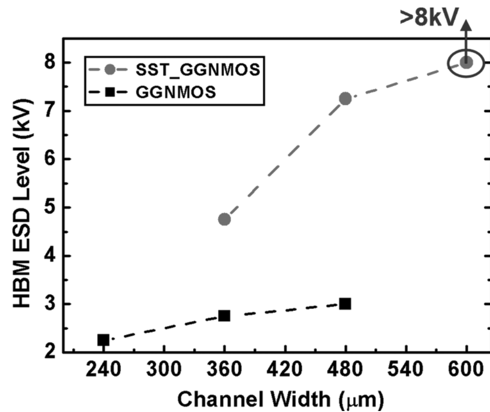


Fig. 14. The relation between the HBM ESD levels and channel widths of traditional GGnMOS and the proposed SST_GGnMOS.

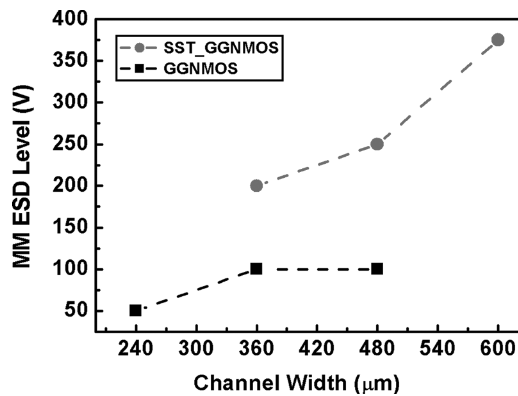
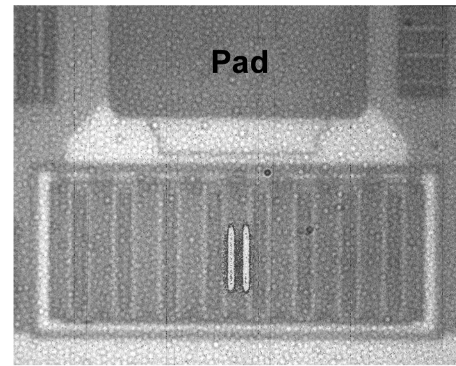
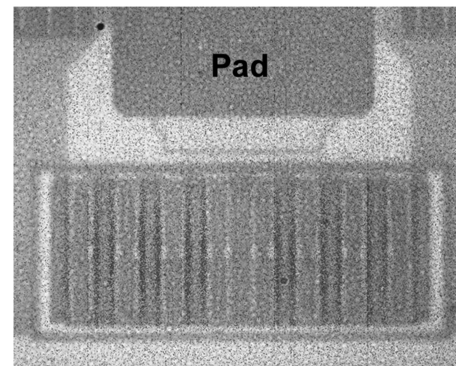


Fig. 15. The relation between the MM ESD levels and channel widths of traditional GGnMOS and the proposed SST_GGnMOS.



(a)



(b)

Fig. 16. Back-side EMMI photographs on (a) the traditional GGnMOS ($W/L = 480\ \mu m/0.18\ \mu m$) and (b) the SST_GGnMOS ($W/L = 480\ \mu m/0.18\ \mu m$, Lcf $= 0.13\ \mu m$) under current pulse of 50 mA. The current distributions are shown with color in these two pictures, where are among the two center fingers in the traditional GGnMOS and among all fingers except the two center fingers in the SST_GGnMOS.

MM ESD levels have verified that the SST_GGnMOS has superior ESD robustness than the traditional GGnMOS.

E. Turn-On Analysis by EMMI

To compare the turn-on behaviors between the traditional GGnMOS and the new proposed SST_GGnMOS, the spatial distribution of ESD-like currents were directly observed by using EMMI analysis on these two devices. EMMI is a widely used technique for wafer-level reliability and yield analysis for semiconductor devices. In general, the analysis is performed by collecting the emitted visible and near infrared wavelength photons when impact ionization and the recombination of electron-hole pairs occurs [4]. In this work, the packaged testchip was thinned on the back side to allow the detection of the photons emission from the back side of the devices, which has been referred as back-side EMMI analysis. The back-side EMMI analysis can avoid the emitted photons covered by the overlying layers such as dielectrics and metal interconnections, and thus can observe the turn-on regions more clearly.

Fig. 16(a) and (b) shows the back-side EMMI photographs of traditional GGnMOS and the SST_GGnMOS when ESD-like current pulses with magnitude of 50 mA is injected into their drain regions through the bond pad, respectively. The channel widths of these two devices are both 480 μm, and the width of unit finger is 30 μm (the total finger number is 16). Fig. 16(a) confirms that the turn-on regions of the traditional GGnMOS are only located at the center regions (two center fingers) of whole device area. However, as the colored images shown in Fig. 16(b), the currents are uniformly distributed through the SST_GGnMOS except the two center fingers. As long as the center fingers trigger the others on, the current will be mainly discharged through the other 14 fingers, and the center fingers will be off. The turn-on time of the center fingers are too short for the EMMI system to collect enough photons. So, in the back-side EMMI photograph, the regions of the center fingers are not colored. The EMMI photographs have practically proven that the turn-on uniformity of the SST_GGnMOS is superior to that of the traditional GGnMOS.

V. Conclusion

To improve the turn-on uniformity of multi-finger GGnMOS, a novel self-substrate-triggered technique has been designed and verified in a 0.13-μm CMOS process with gate-oxide thickness of 25 Å. The device characteristics of SST_GGnMOS have been successfully verified in silicon, and the experimental results have confirmed that the center-finger nMOS transistors can provide the SST_GGnMOS with sufficient substrate-triggered current. The HBM ESD level, MM ESD level, and the It2 per unit channel width of the SST_GGnMOS are all much higher than those of the traditional GGnMOS. Furthermore, the back-side EMMI photographs confirm that

the SST_GGnMOS has superior turn-on uniformly than that of traditional GGnMOS under ESD-like current pulse stresses. The proposed SST_GGnMOS is a good solution for ESD protection design in the nanoscale CMOS technology.

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