Hermetic Packaging Using Eutectic SnPb Solder and Cr/Ni/Cu Metallurgy Layer

Annie T. Huang, Chung-Kuang Chou, and Chih Chen

Abstract-We have developed an easy, low-cost, and low-temperature optoelectronic hermetic packaging technology utilizing the eutectic SnPb solder and the Cr/Ni/Cu bonding pad. Bonding characteristics of the design were investigated in three different setups: silicon-silicon, silicon-glass, and glass-glass samples. Hermeticity was achieved at 200 °C without flux for all samples during the final bonding process. The bonding pads did not dewet during or after the reflow process. By utilizing the eutectic SnPb solder, the self-alignment process can be achieved. Because the bonding process was conducted through visual alignment, original misalignment was estimated to be more than 100 μ m. The surface tension of melting solder during the reflow process allowed the samples to self-align and obtain a misalignment of less than $20\mu m$ after solidification, which was 4% of the entire solder width. The bonding strength of the three setups ranged from 3 to 10 MPa. Among the three setups, glass-glass samples appear to have the strongest bonding strength. This low-temperature and cost-effective soldering process has demonstrated its feasibility and potential utilization in optoelectronic packaging.

Index Terms—Flux-free, hermetic packaging, integrated circuit packaging, semiconductor device packaging, soldering, thin-film circuit packaging.

I. INTRODUCTION

THE optoelectronic industry has become the second leading-edge industry following the semiconductor industry due to its wide range of applications in communications, information, and medicine, etc. Along with the trend of miniaturization of electronic devices, electronic packaging has emerged as the limiting factor in overall size reduction. Currently, the optoelectronic packaging used in the field of emission displays (FEDs) or organic light-emitting diodes (OLEDs) requires a vacuum or noble gas environment because these devices must be isolated from moisture and oxygen to ensure device reliability. It is, therefore, of great importance for the optoelectronic packages to be hermetic in order to protect the devices from the harsh environment at its operating conditions.

Most hermetic packaging technologies require a bonding temperature higher than 300 °C [1]-[4]. Because certain de-

Manuscript received March 19, 2005; revised October 31, 2005. This work was supported by the National Science Council of Taiwan under Grant NSC92-2216-E009-008.

A. T. Huang was with the Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu 30050, Taiwan, R.O.C. She is now with the Department of Materials Science and Engineering, University of California, Los Angeles, CA 90024 USA.

C.-K. Chou and C. Chen are with the Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu 30050, Taiwan, R.O.C. (e-mail:chih@cc.nctu.edu.tw).

Digital Object Identifier 10.1109/TADVP.2006.879427

vices are sensitive to the temperature, some localized heating techniques have been proposed [5], [6]. For example, one can generate heat via built-in microheaters on the silicon substrate, or use microwaves as the heat source to localize the heating on metals. However, neither of these technologies has been fully developed, and both are costly and difficult to implement for mass production. Furthermore, localized heating creates a large temperature gradient that would induce stresses and cause the formation of cracks on the substrates, thus limiting the selection of substrate materials.

A lower processing temperature will prevent the malfunction of a temperature-sensitive device as well as minimize built-in stress after cooling. In this study, the eutectic tin-lead (63% Sn 37% Pb) was chosen due to its low melting temperature of 183 °C. The metallization layers used in this study are similar to the under bump metallurgy (UBM) used for flip chip technology. Because the process is compatible with the current manufacturing process in the IC industry, this bonding technology can be applied readily to the industry. Another advantage of the design is that it makes use of the solder's unique properties. First, solder is a metal. Metal has the lowest permeability to moisture compared with epoxy, glass, and other nonmetal materials. With a width of a few micrometers, metals can block moisture for over a decade. In addition, solders are known to possess self-alignment properties in flip chip technology. As a bonding material, solder provides good hermeticity. Most importantly, the process is cost effective. The design is useful for future applications in optoelectronic packaging.

Different solders can be applied to hermetic packaging for different applications. Lee *et al.* have tested In–Sn as a bonding material using the reflow temperature as low as 120 °C [7]. Kim *et al.* have tested Au–Sn solder line at 400 °C [8]. Due to their difference in melting points, Sn–Pb, Au–Sn, and In–Sn can have a wide range of applications.

In optoelectronic devices, it is sometimes necessary to have packaging transparent to light and RF signals. Because glass is mechanically robust and chemically stable, it can be applied to biological or optical microelectromechanical system (MEMS) devices [5], [9]. Since direct glass-to-glass or silicon-to-glass bonding requires high temperatures, low-temperature glass bonding can only be achieved utilizing an intermediate bonding layer. Therefore, in this paper, we will investigate the hermetic bonding of silicon–silicon as well as silicon–glass and glass–glass bonding using the eutectic SnPb solder.

II. EXPERIMENTAL SETUP

This experiment consists of three different setups: silicon-to-silicon bonding, silicon-to-glass bonding, and

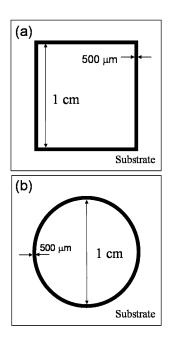


Fig. 1. Design patterns for hermetic bonding.

glass-to-glass bonding. The design of the bonding pads, shown in Fig. 1, includes square and circle patterns of 500- μm width. The square pattern has a dimension of 1 cm \times 1 cm and the circle pattern has a 1-cm diameter.

We first cleaved the silicon wafer and sawed glass slides into 1.5×1.5 cm square pieces. The patterned trilayer metal bonding pad was then obtained on the silicon or glass pieces using e-beam evaporation followed by the liftoff process. . The trilayer metal pad consists of 500 Å of chromium, 2000 Å of nickel, and 6000 Å of copper. The chromium layer serves as an adhesive layer to the silicon and glass. Both nickel and copper act as reaction layers with the solder. Because copper reacts quickly with tin, the original design of the metal layer with 1 μ m of Cu on 500 Å of chromium dewetted within 1 min. To prevent dewetting during the reflow process, an additional 2000 Å of nickel was then added to the modified design. After the trilayer bonding pad was obtained, the eutectic SnPb solder was reflowed with the addition of flux on the top of the bonding pad at 200 °C at normal room atmosphere. Because solder does not react with silicon or glass, the reflow process was done by placing a few small pieces of solder on top of the trimetal lines. Upon melting, solder reacts along the metal line until the entire metal line was covered with solder. The excess solder formed a ball shape residing at a corner of the metal line, which could easily be removed with tweezers in the molten state. The flux was then washed off after this reflow process. Silicon-silicon, silicon-glass, or glass-glass sample pairs were prepared by aligning two square pieces facing bond pad to bond pad using visual alignment, as shown in Fig. 2. We then placed a glass slide of 75×25 mm on top of the sample pair to enhance bonding, and then reflowed without flux on a hot plate at 200 °C at room atmosphere. It was fluxless for the bonding process. The success of the process was due to the compressive stresses from the glass slide during the final bonding process. The solder on both substrates was in a liquid state. The weight

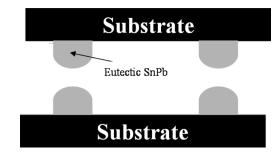


Fig. 2. Schematic picture of the sample pairs during the bonding process.

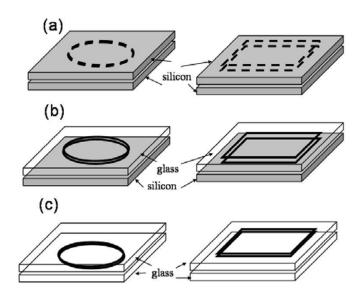
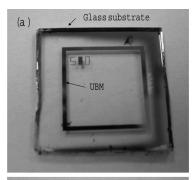


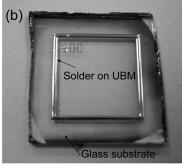
Fig. 3. Schematic diagrams of bonding process for hermetic packaging. Three different setups are silicon–silicon, silicon–glass, glass–glass bonding; two tested shapes are circle and square of 500- μ m width.

from the glass slide broke the native oxide of the molten solder so the bonding could be easily achieved.

Due to the lower thermal conductivity of glass, the reflow time for silicon–silicon and silicon–glass bonding is about 1.5 min as opposed to 3 min for glass–glass bonding. Fig. 3(a)–(c) are the schematics of the Si–Si, Si–glass, and glass–glass test samples, respectively. Because the flux is not required in this process, it is considered a fluxless bonding procedure at this final bonding step.

A leak check was then performed to test the hermeticity of the bonding. FC-84, a 3M fluorocarbon liquid, was used to perform the gross leak checks of bonded sample pairs. FC-84 is the detector fluid used for gross leak check which conforms to Military Specification 883. It has a boiling point of 155 °C. Our gross leak check was performed in the FC-84 solution at a temperature of around 100 °C. Because air expands as temperature increases, bubbles can be detected if there is leakage. Alignment accuracy was also measured by taking cross sections of the samples that passed the gross leak check. For each sample, misalignment was measured on four cross sections evenly throughout the sample. The bonding strength test was also measured with a pulling tester. To prepare the sample for the pull test, each side of the sample pair was adhered to a square nut using the crystal glue. The nuts on the two sides of the sample pair were





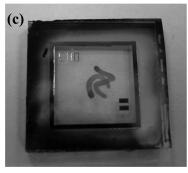


Fig. 4. (a) Glass sample with square bonding pad. (b) Glass sample with square bonding pad after reflow of solder. (c) Sample pairs after bonding process.

then clamped onto the tester for the pull test. During the operation, the machine displays the instantaneous loading and the maximum loading at the breaking point. For the characterization of the packages, a scanning electron microscope (SEM), an optical microscope (OM), and energy dispersive spectroscopy (EDS) were utilized.

III. RESULTS

A photograph of a glass sample with square bonding pad is shown in Fig. 4(a). Fig. 4(b) shows a photo of a glass sample after the solder reflow process. As can be seen, the eutectic solder wets uniformly on the bonding pad. Fig. 4(c) shows the picture of the glass sample after the bonding process. Bonding of glass—Si and Si—Si samples can also be achieved using the same procedure. Similar to solder bump, surface profile of the solder on bonding pads appears to be in a hemi-cylindrical shape so the height of the solder can be controlled by the width of the metallization layer, which is approximately a 80- μ m height on 500- μ m metal line. The uniformity of the solder may not be an issue for the subsequent bonding process, since the solder was in a liquid state. During a trial run of the bonding process, most

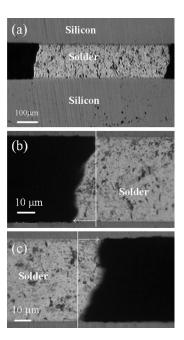


Fig. 5. Cross section of one solder joint of a square silicon–silicon sample after polishing. (a) Whole length of one solder joint. (b) Enlarged picture of the left side. (c) Enlarged picture of the right side.

samples showed leakage. After the placement of a glass slide on top of the sample pairs, the percentage of samples that passed the gross leak check increased drastically. With the design of 500 Å of Cr, 2000 Å of Ni, and 6000 Å of copper, we did not observe dewetting behavior during or after the reflow process. One thing to note is that when the original misalignment was small, we did observe self-alignment during the reflow process. Therefore, sample pairs were aligned and bonded without the addition of flux.

A. Silicon-Silicon Bonding

During the first trial of the bonding process, one out of the two samples leaked. When we placed a glass slide during bonding process, all of the samples passed the leak check. Alignment accuracy was measured by taking cross sections of a sample that passed the gross leak check. Fig. 5(a) shows an SEM image of the cross section of a solder joint. Fig. 5(b) and (c) are enlarged images of the left and right side, respectively. The average misalignment was 11.2 and 13.6 μ m for square and circle samples, respectively. Since the width of the solder line was 500 μ m, the misalignment was only approximately 3% of the width.

Fig. 6(a) and (b) are photographs of the fractured surface of a leaked sample; Fig. 6(c) and (d) are the photographs of an unleaked silicon–silicon sample. A leaked sample usually fractured at solder-to-solder interface, whereas an unleaked sample usually fractured at the interface of Cr and silicon. Fig. 7(a) and (b) display the SEM images of two different kinds of fracture surfaces for a leaked sample. Light-color grains represent the Pb-rich phase. Dark-color grains are the Sn-rich phase. Both images show that the failures appeared to be ductile fractures. However, fracture can occur along Pb-rich grains as shown in Fig. 7(a). Fracture can also occur at some concentration points at the solder fracture surface as shown

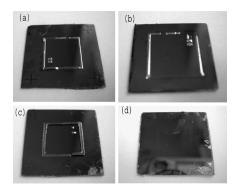


Fig. 6. (a) and (b) Fracture surfaces of a leaked silicon–silicon sample. (c) and (d) Fracture surfaces of an unleaked sample.

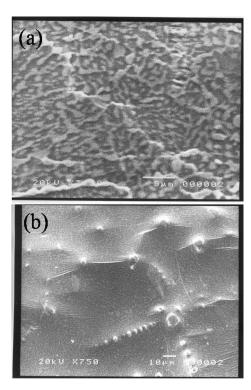


Fig. 7. Fracture interface of a silicon–silicon leak sample pair. (a) Ductile fracture occurs along the Pb-rich phase represented by bright color grains. (b) Ductile fracture occurs along concentration points on silicon–silicon fracture interface.

in Fig. 7(b). From EDS analysis, an unleaked sample usually fractures at Cr-silicon interface.

B. Silicon-Glass Bonding

For silicon–glass sample pairs, three out of the four samples passed the gross leak check with the use of a glass slide during the bonding process. The thermal expansion coefficient for silicon is 2.33 ppm/ $^{\circ}$ C, and the thermal expansion coefficient for glass is 4.8 ppm/ $^{\circ}$ C. It was suspected that a shear stress was created after the bonding process due to the different thermal expansion coefficient of glass and silicon. However, the calculated shear stress only caused about 1 μ m of displacement. Residual stress after cooling was thus not serious for these samples. After taking cross sections of a sample that passed the gross leak check, the average misalignment was found to be 27.3

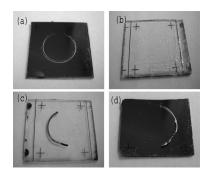


Fig. 8. Photographs of fracture surfaces of two unleaked silicon–glass sample pairs. (a) Silicon side. (b) Glass side. (c) Silicon side for another pair. (d) Glass side for another pair.

and 11.3 μ m for square and circle samples, respectively. Pulling tests were performed on other samples that passed the gross leak check. The average bonding strength of the glass-silicon sample pair was about 7 MPa.

Fig. 8(a) and (b) are photographs of the fracture of a typical unleaked silicon–glass sample. The metal layer is detached from the glass substrate. In some other cases, the metal layer can detach from the silicon substrate as well, as shown in Fig. 8(c) and (d).

C. Glass-Glass Bonding

Without placing the glass slide on the sample during reflow, two out of the three of them leaked. After the placement of a glass slide during the reflow process, none of the samples leaked. The average misalignment of the glass–glass sample pairs is 13.5 and 14 $\mu \rm m$ for square and circle patterns, respectively. The bonding strength of glass–glass bonding ranged from 2 to 10 MPa. The average bonding strength was 5.3 MPa. Because the bonding result of 10 MPa could be obtained, the glass–glass bonding pairs were proven to be comparable or even better than the silicon–silicon bonding pairs.

Fig. 9(a) and (b) show the typical photographs of fracture surface of a square-leaked sample pair. Points of the same number in the two micrographs corresponded to the same fracture locations. The silver color in Fig. 9(a) and (b) indicates the solder interface and the black color indicates Cr and substrate interface. As seen in Fig. 9(b), a small piece of glass was torn apart from the glass substrate at point 1 and transferred onto the glass cap in Fig. 9(a). This demonstrates that if bonding is achieved, the tensile strength of the solder exceeds that of the glass.

Fig. 9(c) and (d) are the photographs of an unleaked sample pair. Similar to silicon–silicon bonding, fracture occurred mostly at the Cr–glass interface. Occasionally, all metal layers are detached from both sides and hang between the sample pairs right after the pulling test.

IV. DISCUSSION

The above results show that almost all samples passed the gross leak check after placement of a glass slide of approximately 1 g, and the results do not vary with the design of pattern. The glass slide served two functions. Its weight was able to break the native Sn oxides layer. At the same time, because glass was a poor thermal conductor, by placing the glass slide on the

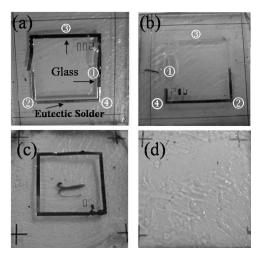


Fig. 9. Photographs of a typical fracture interface after tensile test for an unleaked sample. Glass is torn apart from the glass substrate shown in (b) and transferred onto the bonding pattern of the glass substrates shown in (a). Points of the same number in the two micrographs correspond to the same fracture location. (c) and (d) Photographs of fracture surfaces of another unleaked square glass-glass sample pair.

top of the bonding pairs during the reflow process, there was less heat loss to the environment. As a result, bonding was achieved without the application of flux during this final bonding process. The results also demonstrate that the design of the Cr/Ni/Cu metallurgy layer is able to eliminate dewetting problems. After we deposited both copper and nickel within the reflow time of the bonding process, dewetting was not observed. In this design, the height of solder after reflow was solely controlled by the width of patterns. Because the surface tension of the eutectic SnPb solder generated a cylindrical shape on the copper line with the same line width, the height of the solder was believed to be constant across the entire metal lines. Other width(s) of metal pads like 100 and 1000 μ m were also investigated. The metal line with 100- μ m line width gave a much lower solder height. This was undesired because low standoff height might have had a higher shear strain under the same shear stress. The hermetic sealing may have been broken at lower stress. In addition, it was much more difficult to align using the 100- μ m-width line during the bonding process. The 100- μ m line width was, therefore, not able to provide successful bonding results. When we reflowed the solder on 1000- μ m-width line, the surface tension between the solder and the metal pads was too strong, so there was difficulty in removing excess solder. The results were also not satisfactory.

Solder materials are known to self-align during the reflow process. This phenomenon was observed in our experiment during the reflow process for both circle and square shapes. Because we aligned substrates by visual observation or simply by aligning the silicon chips' edges, the original alignment might have been as large as a few hundred micrometers. After the reflow process, all samples had an alignment accuracy of within 20 μ m. When the misalignment was up to 100 μ m, hermeticity could still be easily achieved with the design due to the low permeability of solder. Patra and Lee presented quasi-static modeling of the self-alignment mechanism in

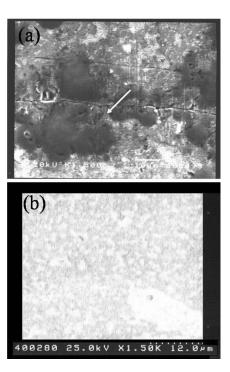


Fig. 10. Cross-sectional SEM images of the solder joints for (a) a leaked sample, and (b) an unleaked sample.

flip chip soldering. [10] The self-alignment profile and bump shape of a solder depended on the original misalignment, axial loading, and surface tension of the solder. Surface tension of the solder was determined by the bonding area and the surface tension coefficient of solder materials. When the misalignment increasesd, the bonding area decreasesd, thus reducing the surface tension available to pull the bumps to self-align. Though the geometry of bonding pads in the design was different from the solder bump, alignment accuracy obtained could still be explained in the same way. The bonding process done with a better original alignment yielded a smaller misalignment.

For glass–glass and glass–silicon samples, leaked sample pairs usually fractured at solder–solder interface; an unleaked sample pair usually fractured at the Cr–silicon or Cr–glass interface. This trend indicated that leakage occurred at the solder–solder interface when bonding was not completely formed. This result could be further confirmed by taking cross sections of a leaked and an unleaked sample. Fig. 10(a) and (b) show the cross-sectional SEM images of a leaked sample and an unleaked sample, respectively. A boundary of solder interface can be seen clearly in Fig. 10(a), as indicated by the arrow in the figure. If the reflow time is sufficient and the temperature is high enough during the bonding process, a solder joint without any solder–solder interface or boundary as in Fig. 10(b) can be obtained. Therefore, it is concluded that this fluxless hermetic packaging is feasible under proper bonding conditions.

The pulling test results show a significant range for bonding strength. Compared to the tensile strength of the SnPb solder in the literature, which is 33.9 MPa, the bonding strength measured for the hermetic packaging was significantly lower. Our tensile results showed that the fracture generally occurred in the interface of the metallization layer and the substrate. Therefore, the

limitation of the bonding strength was on the adhesion strength of the interface.

The shear stress induced by the thermal expansion coefficient was not significant for the above setups. If a more precise alignment was required, the thermal stress might still be a concern. To reduce thermal stress between glass-silicon bonding samples, another kind of glass can probably be utilized. Pyrex 7740 glass is known to have a similar thermal expansion coefficient with silicon. If Pyrex 7740 is used instead of glass substrates, the stress problem can be further reduced. Furthermore, because the bonding process was done in ambient air, at the reflow temperature, the oxide thickness grew and it was thus necessary to apply a certain amount of compressive stress to break the oxide as was done with the glass slide in our experiment. If the process could be performed in a noble gas environment, or in a vacuum, the growth of oxide would be eliminated and a much smaller mechanical stress would be required. As a result, the gap between bonded samples should be increased as well due to a lower compressive force applied, thus achieving a higher standoff height.

V. CONCLUSION

With our low-cost and fluxless bonding process, hermetic packaging is achieved for the three setups. As expected, the self-alignment behavior was also observed during the bonding process. With original misalignment of probably more than $100~\mu m$, we were able to achieve a final misalignment much smaller than $100~\mu m$. The average misalignment of all samples was about $12~\mu m$. This shows that accurate alignment can be easily achieved without initial precise alignment. Average bonding strength for glass–glass, silicon–glass, and silicon–silicon was 4.5, 7.0, and 5.3~MPa, respectively, and the fracture interface of leaked samples was found to occur at the solder–solder interface, whereas that of unleaked samples occurred at the Cr–Si or Cr–glass interface. The bonding strength and hermeticity, however, may be further improved if the samples can be bonded in a noble gas or vacuum environment.

REFERENCES

- [1] R. K. Shukla and N. P. Mencinger, "A critical review of VLSI dieattachment in high reliability applications solid state technology," *Solid State Technol.*, vol. 28, pp. 67–74, 1985.
- [2] A. L. Tiensuu, J. A. Schweitz, and S. Johansson, "In situ investigation of precise high strength micro assembly using Au–Si eutectic bonding," in Proc. 8th Int. Conf. Solid-State Sens. Actuators (Transductors '95), 1995, vol. 252, pp. 236–239.
- [3] M. Madou, Fundamentals of Microfabrication. Boca Raton, FL: CRC, 1997.

- [4] W. H. Ko, J. T. Suminto, and G. J. Yeh, Micromachining and Micropackaging of Transducers. New York: Elsevier, 1985, pp. 41–61.
- [5] Y. T. Cheng, L. W. Lin, and K. Najafi, "A hermetic glass-silicon package formed using localized aluminum/silicon–glass bonding," J. Microelectromech. Syst., vol. 10, no. 3, pp. 392–399, 2001.
- [6] N. K. Budraa, H. W. Jackson, M. Barmatz, W. T. Pike, and J. D. Mai, "Low pressure and low temperature heremetic wafer bonding using microwave heating," in *Proc. 12th IEEE Int. Conf. Micro Electro Mech. Syst.*, 1999, vol. 490, pp. 490–492.
- [7] C. K. Lee, W. F. Huang, and J. S. Shie, "Wafer bonding by low-temperature soldering," Sens. Actuators A, vol. 85, pp. 330–334, 2000.
- [8] S. A. Kim, Y. H. Sco, Y. H. Cho, G. H. Kim, J. Y. Park, and J. U. Bu, "Closed loop solder-lines on heated substrates," in *Proc. Electron. Compon. Technol. Conf.*, 2002, pp. 1101–1105.
- [9] B. Ziaie, J. A. VonArx, M. R. Dokmeci, and K. Najafi, "A hermetic glass-silicon micropackage with high-density on-chip feedthroughs for sensors and actuators," *J. Microelectromech. Syst.*, vol. 5, no. 3, pp. 166–179, 1996.
- [10] S. K. Patra and Y. C. Lee, "Quasi-static modeling of the self-alignment mechanism in flip-chip soldering-part 1: Single solder joint," *J. Elec*tron. Packag., vol. 133, pp. 337–342, 1991.



Annie T. Huang received the B.S. degree in chemical engineering from the University of California, Berkeley, in 2000 and the M.S. degree in materials science and engineering from National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 2002. She is currently pursuing the Ph.D. degree in materials science and engineering, University of California, Los Angeles.

Her research interest is electronic packaging and thermomigration of solder.



Chung-Kuang Chou received the B.S. degree in materials science and engineering from National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 2002 and the M.S. degree in materials science and engineering from University of California, Los Angeles, in 2004

He is currently serving in the Taiwanese army to fulfill his two-year obligation service. His research interest is electronic packaging and electromigration of solder.



Chih Chen received the B.S. degree in materials science and engineering from National Tsing Hua University, Hsinchu, Taiwan, R.O.C., in 1992, the M.S. and Ph.D. degrees in materials science and engineering from University of California, Los Angeles, in 1996 and 1999, respectively.

Since 2004, he has been an Associate Professor of materials science and engineering, National Chiao-Tung University, Hsinchu, which he joined in 2000 as an Assistant Professor. He has authored or coauthored 33 journal papers in the areas of electronic

packaging, electromigration of solder, and electronic materials.