Plasma Damage-Enhanced Negative Bias Temperature Instability in Low-Temperature Polycrystalline Silicon Thin-Film Transistors

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***Abstract*—In this letter, a mechanism that will make negative bias temperature instability (NBTI) be accelerated by plasma damage in low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs) is presented. The experimental results confirm that the mechanism, traditionally found in the thin gate-oxide devices, does exist also in LTPS TFTs. That is, when performing the NBTI measurement, the LTPS TFTs with a larger antenna ratio will have a higher degree in degradation of the threshold voltage, effective mobility, and drive current under NBTI stress. By extracting the related device parameters, it was demonstrated that the enhancement is mainly attributed to the plasma-damage-modulated creating of interfacial states, grain boundary trap states, and fixed oxide charges. It could be concluded that plasma damage will speed up the NBTI and should be avoided for the LTPS TFT circuitry design.**

***Index Terms*—Low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs), negative bias temperature instability (NBTI), plasma damage.**

I. Introduction

RECENTLY, low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs) have attracted much research interest due to its high potential of realizing system on panel [1]. To achieve a good process repeatability and a precise control of feature sizes, plasma process has been widely used in the manufacture of ULSI and LTPS TFTs. However, plasma damage has been reported to degrade the performance and reliability in thin-film transistors TFTs [2]–[4].

Negative bias temperature instability (NBTI) has been widely studied and was found to be an important reliability issue for the pMOSFETs [5], [6]. Several researchers have showed that the NBTI occurs in p-type-channel TFTs [7]–[12] as well; however, the correlation between plasma damage and NBTI in LTPS TFTs has not been explored.

This letter aims to investigate the effects of plasma damage on the NBTI behaviors in LTPS TFTs; accordingly, p-type-channel TFTs with various antenna structures were designed, and then, NBTI measurement was performed in this letter.

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II. Experimental

The p-channel LTPS TFTs were fabricated on glass substrates, in this letter. First, a 400-Å amorphous-Si layer was deposited and crystallized into poly-Si film by excimer laser annealing. After defining the active region, the 1000-Å SiO_2 was deposited as a gate dielectric. Then, Mo, with a thickness of 3000 Å, was deposited and patterned as the gate electrode. Following source/drain formation, a 5000-Å SiO_2 was deposited as interlayer dielectric and densified. Finally, a 5000-Å Al was deposited and patterned as metal pads. The channel length (L) and width (W) of the devices mainly used were 10 and 20 μm, respectively. The metal pads attached to the gate were designed with an antenna-area ratio (AR) of 100, 500, and 1000. The AR is defined as the ratio between the antenna and gate areas on the active region $(L \times W)$. The schematic cross sectional diagram of the test structure is shown in the inset of Fig. 1. NBTI stress was performed at 150 °C, and a stress voltage of -30 V was applied to the gate with the source/drain grounded. All the measurements were taken at the stress temperature, and the stress was periodically stopped to measure the basic device characteristics. The delay time between the stress and measurement was set at 1 s.

III. Results and Discussion

Fig. 1 shows the NBTI-induced transfer characteristic degradation for the LTPS TFTs with an AR of 100, 500, and 1000. We found that NBTI stress makes the threshold-voltage $(V_{\rm th})$ shift to the negative direction and simultaneously degrades the subthreshold swing (S); additionally, the effects are getting worse for the devices with a larger AR. Therefore, it is reasonable to suppose that the NBTI in LTPS TFTs is modulated by plasma damage. The correlations can be further observed from the threshold-voltage shift $(\Delta V_{\rm th})$ versus the stress time for the LTPS TFTs with different ARs, as shown in Fig. 2. Fig. 2 significantly confirms that the device with a larger AR does induce a greater $\Delta V_{\rm th}$ under NBTI stress. Compared with the $\Delta V_{\rm th}$, the drive current $(I_{\rm ON})$ degradation, revealed in the inset of Fig. 2, presents the same trend that confirms plasma-damage-enhanced NBTI.

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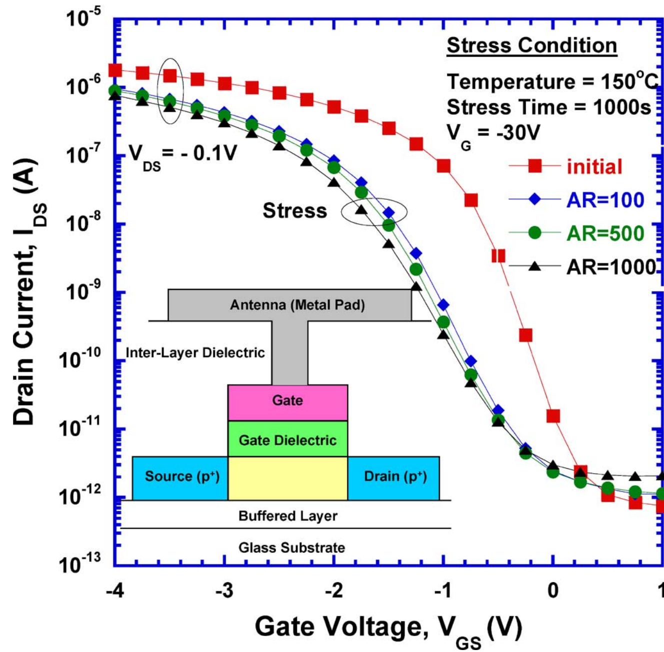

Fig. 1. Transfer characteristics of the LTPS TFTs with an AR of 100, 500, and 1000 before and after a 1000-s NBTI stress. The inset shows the schematic cross sectional diagram of the test device structure used in this letter.

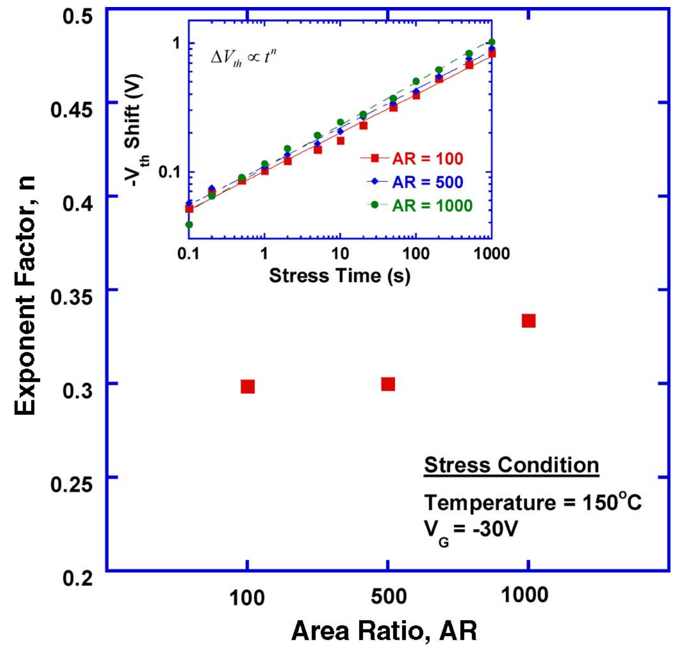

Fig. 3. Exponent factors (n) of the LTPS TFTs with various ARs. The inset shows the linear fit of the log–log plot of the threshold-voltage shift versus the stress time of LTPS TFTs with an AR of 100, 500, and 1000 under NBTI stress.

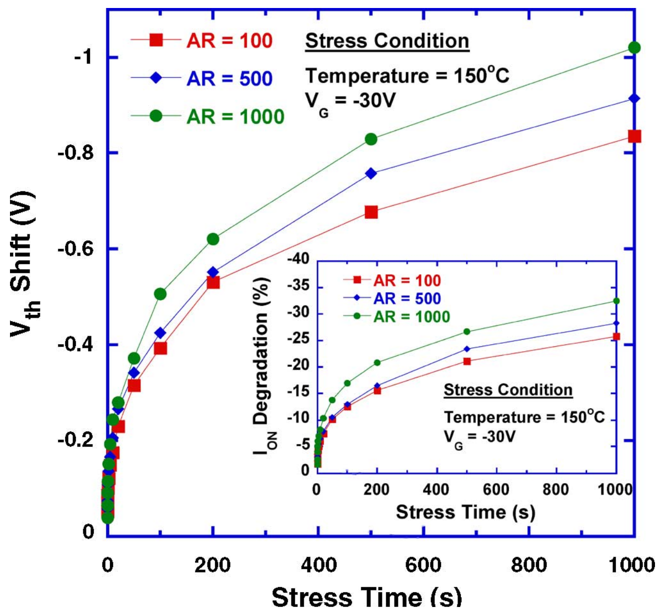

Fig. 2. Dependence of the threshold-voltage shift and drive-current degradation (in the inset) on the stress time for the LTPS TFTs with an AR of 100, 500, and 1000.

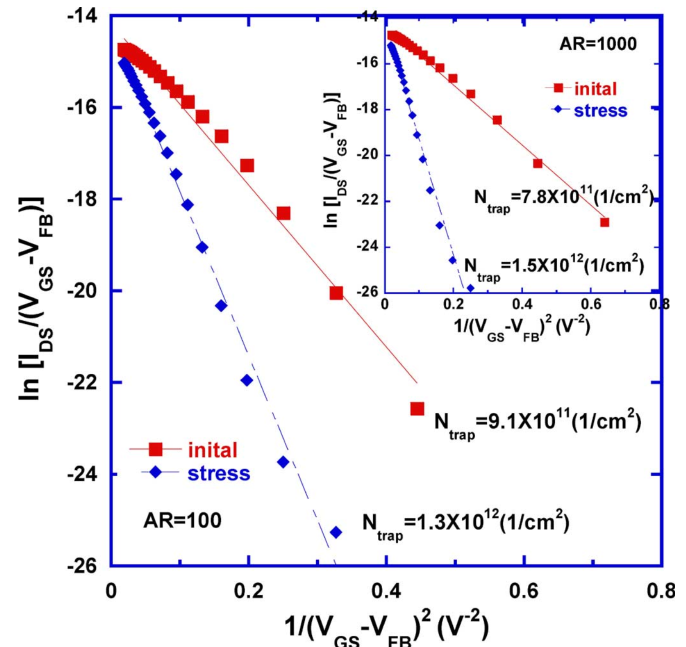

Fig. 4. Extraction of the grain boundary trap state density of LTPS TFTs with an AR of 100 and 1000 (in the inset) before and after a 1000-s NBTI stress.

It is well known that the $\Delta V_{\rm th}$ of pMOSFETs under NBTI stress shows a power-law dependence on the stress time with an exponent factor (n) of 1/3–1/4, which can be illustrated by the diffusion-controlled electrochemical reactions. These reactions are usually explained by the generation of fixed oxide charges and interface states in MOSFETs, leading to the $V_{\rm th}$ shift [13]–[15]. Our experimental results, displayed at the inset of Fig. 3, also follow a similar dependence on the stress time. Fig. 3 exhibits the extracted n values for the LTPS TFTs with different ARs. It is interesting to note that the n value is larger for the device with a larger AR, indicating that plasma damage accelerates NBTI in LTPS TFTs. Accordingly, it proves that plasma damage enhances NBTI in LTPS TFTs. The enhancement is caused by the fact that the samples with plasma damage generates more interfacial states and fixed oxide charges during NBTI stress. Owing to the fact that the LTPS TFTs have a lot of grain boundaries in the channel region, the NBTI mechanisms of the LTPS TFTs will be different from that of MOSFETs. Fig. 4 compares the grain boundary trap state density $(N_{\rm trap})$

TABLE I
COMPARISON OF PARAMETER VARIATION OF THE LTPS TFTS WITH AN AR OF 100, 500, AND 1000 AFTER A 1000-s NBTI STRESS

Stress Condition: $V_G = 30V$, 150°C			
	AR=100	AR=500	AR=1000
$\triangle\mu_{eff}$ (%)	-6.7	-7.9	-9.0
$\triangle S$ (%)	52.3	64.2	78.7
$\triangle V_{th}$ (V)	-0.84	-0.91	-1.02
$\triangle I_{ON}$ (%)	-25.8	-28.3	-32.5
$\triangle N_{trap}$ (%)	42.7	67.8	96.3

estimated by the Levinson and Proano method [16], [17]. By taking the NBTI stress, the $N_{\rm trap}$ increases from 9.1×10^{11} to 1.3×10^{12} $({\rm cm}^{-2})$ and from 7.8×10^{11} to 1.5×10^{12} $({\rm cm}^{-2})$ for the device with an AR of 100 and 1000, respectively. The overall generation of $N_{\rm trap}$ is enhanced for the device with a larger AR; this signifies that plasma damage enhances NBTI not only through the previously mentioned mechanisms but also by accelerating the generation of grain boundary trap states during NBTI stress.

Table I compares the parameter variation of the LTPS TFTs that was stressed by NBTI for 1000 s; the AR of those devices are 100, 500, and 1000, respectively. As AR increases, the devices have a higher degree in degradation of the effective mobility $(\mu_{\rm eff})$, S, $V_{\rm th}$, $N_{\rm trap}$, and $I_{\rm ON}$. All the results confirm that plasma damage enhances the quantity of NBTI in LTPS TFTs. The enhancement could be induced by the fact that the plasma damage degrades the quality of gate oxide, poly-Si/SiO_2 interface, and grain boundaries; those consequences were represented in the NBTI measurement rather than in the initial quality verification.

IV. CONCLUSION

In this letter, we confirmed that plasma damage is a significant factor for NBTI reliability in LTPS TFTs. The experimental results show that the consequence of plasma damage will be represented under NBTI stress in LTPS TFTs. The plasma-damage-correlated NBTI acceleration is mainly attributed to the speeding up of generations in interfacial states, grain boundary trap states, and fixed oxide charges. Therefore, to sustain the LTPS TFTs with both high reliability and high yield, the antenna structures must be carefully designed.

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