A New Lossy Substrate Model for Accurate RF CMOS Noise Extraction and Simulation With Frequency and Bias Dependence

Jyh-Chyurn Guo and Yi-Min Lin

***Abstract*—A lossy substrate model is developed to accurately simulate the measured RF noise of 80-nm super-100-GHz f_T n-MOSFETs. A substrate *RLC* network built in the model plays a key role responsible for the nonlinear frequency response of noise in 1–18-GHz regime, which did not follow the typical thermal noise theory. Good match with the measured S-parameters, Y-parameters, and noise parameters before deembedding proves the lossy substrate model. The intrinsic RF noise can be extracted easily and precisely by the lossy substrate deembedding using circuit simulation. The accuracy has been justified by good agreement in terms of I_d, g_m, Y-parameters, and f_T under a wide range of bias conditions and operating frequencies. Both channel thermal noise and resistance induced excess noises have been implemented in simulation. A white noise γ factor extracted to be higher than $2/3$ accounts for the velocity saturation and channel length modulation effects. The extracted intrinsic $\mathrm{NF}_{\min}$ as low as 0.6–0.7 dB at 10 GHz indicates the advantages of super-100 GHz f_T offered by the sub-100-nm multifinger n-MOSFETs. The frequency dependence of noise resistance R_n suggests the bulk *RC* coupling induced excess channel thermal noise apparent in 1–10-GHz regime. The study provides useful guideline for low noise and low power design by using sub-100-nm RF CMOS technology.**

***Index Terms*—Lossy substrate, noise, RF CMOS, *RLC* network.**

I. Introduction

THE aggressive scaling of CMOS technology to sub-100-nm scale can offer high-speed devices with cutoff frequency f_T and maximum oscillation frequency $f_{\max}$ approaching 100 GHz and above [1]–[7]. It is really a very attractive solution for low cost RF integrated circuit (IC) development. However, the tradeoff among various RF performance parameters such as bandwidth, linearity, gain, power, and noise becomes an important reality to be considered. Potentially, we gain higher f_T and $f_{\max}$ but suffer some loss in the noise performance. The challenge arises to look for an optimized design, which can achieve maximum gain and maintain the noise at minimum. Another challenge coming out to trigger our motivation of this study is how to measure the truly intrinsic noise of sub-100-nm devices precisely. Currently it remains a difficult research subject to extract on-wafer RF CMOS noise accurately while its scalability with device scaling is desirable for low-noise RF circuit design. The difficulty stems from the strong dependence of RF noise on the parasitic and coupling effect associated with the gate, transmission line, pads, and lossy substrate, etc. [8]–[10] Gate-induced thermal noise is one of well-known noise sources, and multifinger structures are generally used to reduce the gate resistance (R_g). Gate leakage current effect on thermal noise is one more special concern for sub-100-nm MOSFETs with ultra-thin gate oxide. Comparison of calculated dc gate leakage and ac gate displacement currents was performed to verify this effect. It indicates that for an 80-nm n-MOSFET with $T_{\mathrm{ox}} = 17$ Å, the dc gate leakage current at 1.0 V is around 0.64 nA/μm, while the ac gate displacement current can reach as high as 7.22–72.2 μA/μm corresponding to frequencies of 1–10 GHz. The obvious dominance of the ac current over the dc leakage current by more than four orders suggests that the gate leakage current effect can be neglected under high frequency in the gigahertz regime.

In our study, more important excess noises were identified to be originated from lossy substrate, lossy pad, and transmission-line coupling effects. The lossy Si substrate generally leads to an extremely complicated *RLC* effect and there is no effective deembedding method to solve it for intrinsic noise extraction. Regarding the lossy pad rendered through pad-to-substrate coupling, the impact is increasing for miniaturized devices and particularly worse for sub-100-nm Si RF CMOS. It is due to the fact that the pad capacitance may overwhelm the intrinsic devices, which we want to measure and model. The increasing pad impact suggests that the RF pad layout is very critical. As for the transmission-line effect, which is becoming significant with increasing frequency, e.g., above 10 GHz and approaching 20 GHz in this study, it is no longer negligible. All the mentioned excess noises dramatically increase with device size scaling and reveal nonlinear frequency dependence. The observation cannot be explained by typical thermal noise theory and formulas in which linear frequency response was predicted [11], [12]. One of the most popular solutions is the noise correlation matrix method, which is based on circuit theory, developed by Haus and Adler in 1959 [13] and the noise correlation matrix derived by Hillbrand and Russer in 1976 [14]. However, the complicated matrices calculation sometimes suffers fluctuation at a very low noise level and poor accuracy in frequency dependence. Previous study on pad deembedding using the matrices correlation method revealed dramatic fluctuation of $\mathrm{NF}_{\min}$ (minimum noise figure) in a

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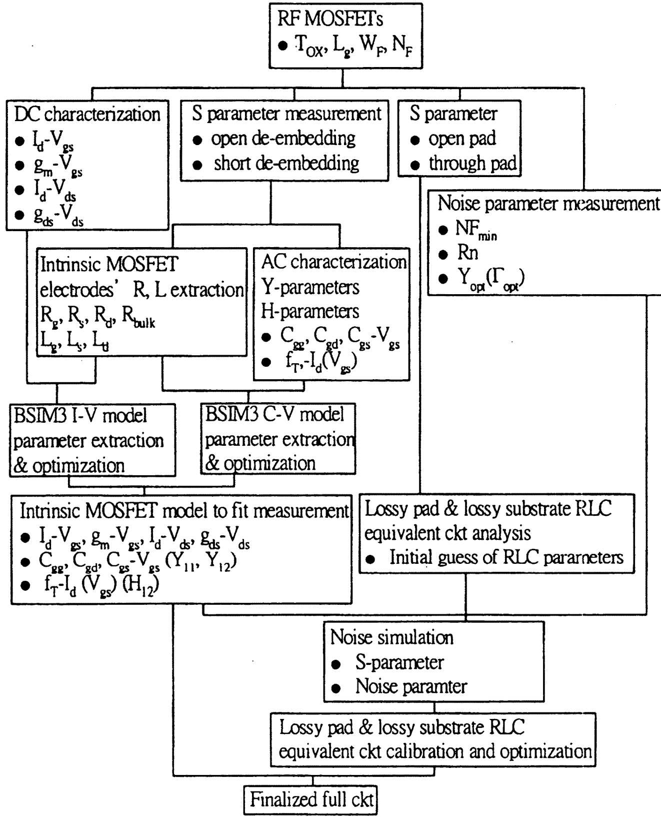


Fig. 1. Flowchart of RF MOSFET characterization and modeling.

wide range of 0.5–1.5 dB. Smoothing was reported to get reasonable frequency dependence [9]. A three-step deembedding method incorporating open, short, and through was proposed to deembed the excess noise, which is caused by pad and transmission line. However, two specially designed dummy pads for through deembedding of two ports are necessary. Besides, matrices correlation method cannot be avoided for intrinsic noise extraction [15]. A new transmission-line deembedding method was published to extract the lossy substrate and lossy pad effect. In this way, the intrinsic $\mathrm{NF}_{\min}$ for sub-100-nm n-MOSFETs can be simulated accurately [10]. However, frequency-dependent substrate resistance was assumed to account for the deviation from the generally used Fukui formula [12] and match the nonlinear frequency response of measured $\mathrm{NF}_{\min}$. Besides, the bias and drain current dependence was not extensively verified. The drain current dependence of noise is quite important for low-power and low-noise RF CMOS design.

In recent research, we proposed an enhanced lossy substrate model in which the complicated frequency dependence can be precisely described by the *RLC* network without assumption of frequency-dependent elements [16]. A good match with measured $\mathrm{NF}_{\min}$ over a wide range of drain currents ($I_d = 0.5$–100 mA) and frequencies (1–18 GHz) has been achieved. As for the extraction of intrinsic $\mathrm{NF}_{\min}$ by using simulation, improvement of the existing BSIM3 model accuracy in terms of mobility, gate capacitance, and the employment of parasitic resistances such as R_g, R_s, R_d, and R_{bulk} with correct values becomes a challenge. In this study, calibration

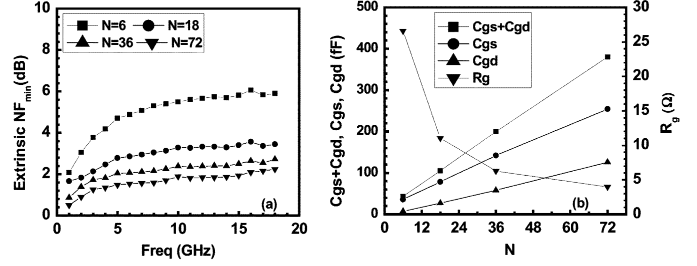


Fig. 2. 80-nm n-MOSFET ($N = 6, 18, 36, 72$) (a) Measured $\mathrm{NF}_{\min}$ (1–18 GHz). (b) R_g extracted from Z-parameters and $(C_{\text{gs}}, C_{\text{gd}}, C_{gg})$ extracted from Y-parameter.

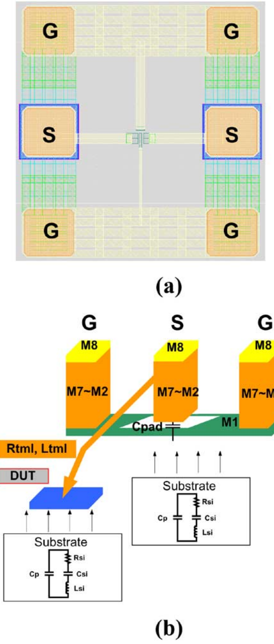
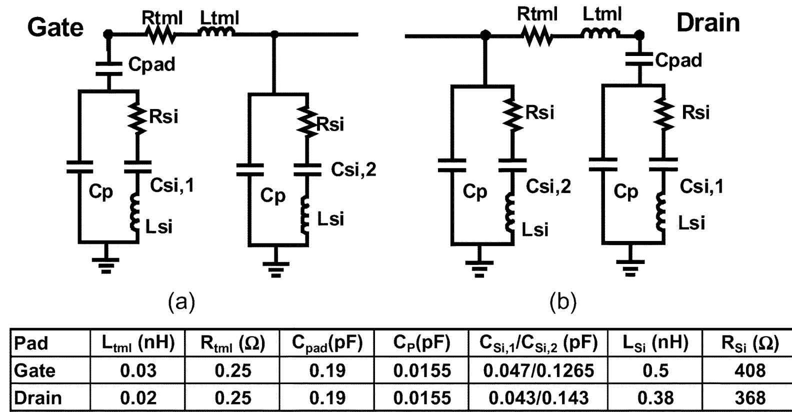


Fig. 3. Open pad. (a) 2-D layout with two signal pads and four ground pads. Two signal pads are used for connection to gate and drain of the MOSFET. Four ground pad are connected together through M1. (b) 3-D structure to show the metal layers for signal (S) and ground (G) pads and interconnection to DUT.

on the existing gate capacitance model, correct extraction of $R_g, R_s, R_d, R_{\text{bulk}}$, and deployment in the original intrinsic MOSFET scheme have been done. Through the mentioned process, a good match is achieved in terms of I_d, g_m, Y-parameters, and f_T over a wide range of drain currents and frequencies and the accuracy of the calculated $\mathrm{NF}_{\min}$ can be justified. The intrinsic $\mathrm{NF}_{\min}$ as low as 0.6–0.7 dB at 10 GHz calculated by the calibrated intrinsic MOSFET model reveals the advantage offered by the sub-100-nm devices.

II. Device Characterization and Modeling Flow

To study the nanoscale CMOS scaling effect on speed and noise, sub-100-nm n-MOSFETs of gate length at 80 nm are used. Multifinger structures are employed to reduce the gate resistance generated RF noise. The finger width is fixed at 4 μm and finger numbers of 6, 18, 36, and 72 ($N = 6, 18, 36, 72$) are designed for study of performance optimization. Fig. 1 illustrates the flowchart to explain the device characterization and modeling procedure for this study. At first, *I–V* characterization was done to extract the transconductance (g_m) that is



Pad	L_{tml} (nH)	R_{tml} (Ω)	C_{pad}(pF)	C_P(pF)	$C_{Si,1}/C_{Si,2}$ (pF)	L_{Si} (nH)	R_{Si} (Ω)
Gate	0.03	0.25	0.19	0.0155	0.047/0.1265	0.5	408
Drain	0.02	0.25	0.19	0.0155	0.043/0.143	0.38	368

Fig. 4. *RLC* network circuits for open pads and lossy substrate coupled through the pad. (a) Gate pad as port-1. (b) Drain pad as port-2.

a key parameter governing f_T and noise figure. The gate bias $(V_{\rm gs})$ corresponding to the maximum g_m for various N was around 0.7 V and drain bias $(V_{\rm ds})$ was fixed at $V_{dd} = 1.0$ V. Following the bias conditions and dc characterization, S-parameters were measured by using an Agilent vector network analyzer up to 40 GHz. Open and short deembedding were done on the measured two-port S-parameters to extract the intrinsic Y-, H-, and Z-parameters. Subsequently, *C–V* model parameters can be extracted from Y-parameters and f_T can be determined from H-parameters. Z-parameters of the intrinsic MOSFETs are used to extract the electrodes' R and L such as R_g, R_s, R_d, L_g, L_s, and L_d. The intrinsic MOSFET incorporating the parasitic R, L as extracted is adopted by ADS simulation to do *I–V* and *C–V* model parameter extraction and optimization simultaneously. The accuracy of the intrinsic MOSFET model has been extensively verified and validated by a good match with the measurement in terms of $I_d - V_{\rm gs}, g_m - V_{\rm gs}, I_d - V_{\rm ds}, g_{\rm ds} - V_{\rm ds}, C_{gg}, C_{\rm gd}, C_{\rm gs} - V_{\rm gs}$, and $f_T - I_d(V_{\rm gs})$, etc.

The noise parameters $(\mathrm{NF}_{\min}, R_n$, and $Y_{\rm opt}$ or $\Gamma_{\rm opt})$ were measured by an ATN-NP5B system to 18 GHz for $V_{\rm gs}$ fixed at maximum g_m and under varying $V_{\rm gs}$ to cover a wide range of drain current ($I_d = 0.5$–100 mA) for a fixed frequency at 2.4, 5.8, and 10 GHz. A through (thru) line was proposed in the equivalent circuit to emulate the transmission line between the RF probe pad and gate terminal. In this study, we proposed a new *RLC* equivalent circuit to model the lossy substrate, lossy pad, and thru line's parasitic to deembed their effect on RF noise. The details of *RLC* equivalent-circuit development for modeling the lossy substrate and lossy pad will be described in Section III. A full-circuit model can be obtained by integrating the intrinsic MOSFET with the pad capacitance, the substrate and thru line related resistance (R), capacitance (C), and inductance (L), which represent the lossy pad and lossy substrate. The extrinsic noise can then be simulated by using the full-circuit model. Through tuning of *RLC* parameters, the best fit to the measured S-parameters and noise parameters can be achieved and the full circuit can be finalized corresponding to optimized *RLC* parameters. The intrinsic MOSFET noise can be extracted by simulation through the lossy substrate and lossy pad deembedding from the validated full circuit.

III. Substrate *RLC* Circuit Network and Extrinsic Noise Model

Fig. 2(a) shows the measured $\mathrm{NF}_{\min}$ for 80-nm n-MOSFETs with various finger numbers $(N = 6, 18, 36, 72)$ and biased under maximum g_m. The RF noise without deembedding decreases remarkably with increasing N. The lower R_g associated with larger N may account for part of the contribution, but cannot explain the dramatic difference up to 4.0 dB between $N = 6$ and $N = 72$ in 10–18 GHz. Fig. 2(b) indicates R_g extracted from Z-parameters and the gate capacitances $(C_{\rm gs}, C_{\rm gd})$ from Y-parameters after deembedding for various N. Obviously, varying N plays a tradeoff between R_g and $(C_{\rm gs}, C_{\rm gd})$, and the resultant f_T is kept at similar level of around 90–105 GHz for $N = 6$ and 72. It suggests that R_g is not the major factor responsible for the dramatic difference in measured $\mathrm{NF}_{\min}$. Regarding the abnormally high $\mathrm{NF}_{\min}$ measured from the smallest device with $N = 6$, the increasing weighting factor played by the lossy substrate is considered as the major cause.

A. Open Pad Layout, Three-Dimensional (3-D) Structure, and Equivalent RLC Parameter-Extraction Method

Fig. 3(a) and (b) exhibits the open pad layout and 3-D structure used for S-parameter deembedding. Herein, metal lines used for connection to the device-under-test (DUT) are stacked from top metal, i.e., M8 and terminated at M3. All DUTs of different N share an identical open pad for deembedding. Due to this fact, a single set of *RLC* equivalent-circuit and model parameters were extracted. This set of *RLC* model parameters suitable for the open pad will be used as initial values for further tuning and optimization. Through the optimization, a new set of *RLC* model parameters can be achieved to fit the full circuit with the DUT (MOSFET) linked with the pads. The details of extraction and optimization flow have been shown in Fig. 1.

Fig. 4(a) and (b) illustrates the equivalent circuits and model parameters that we propose to simulate the lossy substrate effect through gate and drain pads referring to two-dimensional (2-D) layout and 3-D structure in Fig. 3 for clear images. The proposed *RLC* network incorporating pad capacitance $(C_{\rm pad})$,

lossy substrate ($R_{\rm Si}, C_{\rm Si}, L_{\rm Si}$, and C_p), and transmission line ($R_{\rm tml}, L_{\rm tml}$) will be connected to the gate and drain terminals of the intrinsic MOSFET. The transmission-line body is consisted of series resistor ($R_{\rm tml}$) and inductor ($L_{\rm tml}$). The shunt *RLC* path to ground at gate/drain pads is used to simulate the lossy pad and lossy substrate effect. The existence of both capacitive and inductive impedances, i.e., $C_{\rm Si}$ and $L_{\rm Si}$ in series with $R_{\rm Si}$, is quite different from the conventionally used simple shunt *RC* circuit. This new *RLC* network was created to accurately capture the unique frequency response associated with the lossy substrate. The *RLC* network has been extensively verified by comparison with measured results in terms of S-parameters and Y-parameters of open pads for both the gate (port-1) and drain (port-2), respectively.

Fig. 5(a) illustrates the schematic block diagram derived by circuit analysis theory to extract the circuit elements ($R_{\rm Si}, C_{\rm Si}, L_{\rm Si}, C_p, R_{\rm TML}$, and $L_{\rm TML}$). Fig. 5(b) indicates the model parameter-extraction flow based on the circuit analysis. The pad capacitance $C_{\rm pad} = 190$ fF is a physical parameter calculated by layout and process parameters rather than from extraction. $C_{\rm pad}$ is around five times the intrinsic gate capacitance $C_{gg} (= C_{\rm gs} + C_{\rm gd})$ of the smallest device with $N = 6$, which is around 40 fF in Fig. 2(b). Note that the first run of model parameters extracted based on approximation valid under relatively low/high frequencies (0.2/40 GHz in this study) just serve as the initial guess for further optimization. The optimization was done by using ADS simulation to get the best fit to S- and Y-parameters for both open pads and full circuit (pads and intrinsic MOSFET together).

Fig. 6(a) and (b) shows the good agreement in the Smith chart between simulation and measurement for open pad's S_{11} (gate pad as port-1) and S_{22} (drain pad as port-2). Fig. 7(a)–(d) reveals the good fit to measured S_{11} (magnitude and phase) and ${\rm Im}(Y_{11})$ for the gate pad in which the effect of $C_{\rm Si}$ and $L_{\rm Si}$ can be obviously identified. Fig. 8(a)–(d) indicates the good match with measured S_{22} (magnitude and phase) and ${\rm Im}(Y_{22})$ corresponding to drain pads where the $C_{\rm Si}$ and $L_{\rm Si}$ effect is revisited and confirmed.

All the results are demonstrated over a wide range of frequencies up to 40 GHz. The match simultaneously achieved for both S- and Y-parameters manifests the fact that the proposed *RLC* network is accurate to account for the lossy substrate effect. Our study suggests that $R_{\rm Si}, C_{\rm Si}$, and $L_{\rm Si}$ are three key parameters playing the role to capture the lossy substrate's feature over wide bandwidth. $C_{\rm Si}$ is the primary element responsible for the phase and magnitude deviation in the full frequency range, as well as the nonlinear frequency response of ${\rm Im}(Y_{11})$ and ${\rm Im}(Y_{22})$. On the other hand, $L_{\rm Si}$ reveals an increasing effect in higher frequencies. The nonlinear frequency response of ${\rm Im}(Y_{11})$ or ${\rm Im}(Y_{22})$ introduced by $C_{\rm Si}$ accounts for the nonconstant capacitance as extracted by ${\rm Im}(Y_{11})/\omega$ and ${\rm Im}(Y_{22})/\omega$. The obvious two-slope curvature results in larger effective capacitance in lower frequencies corresponding to larger slope and apparently smaller effective capacitance at higher frequencies due to much reduced slope to near saturation.

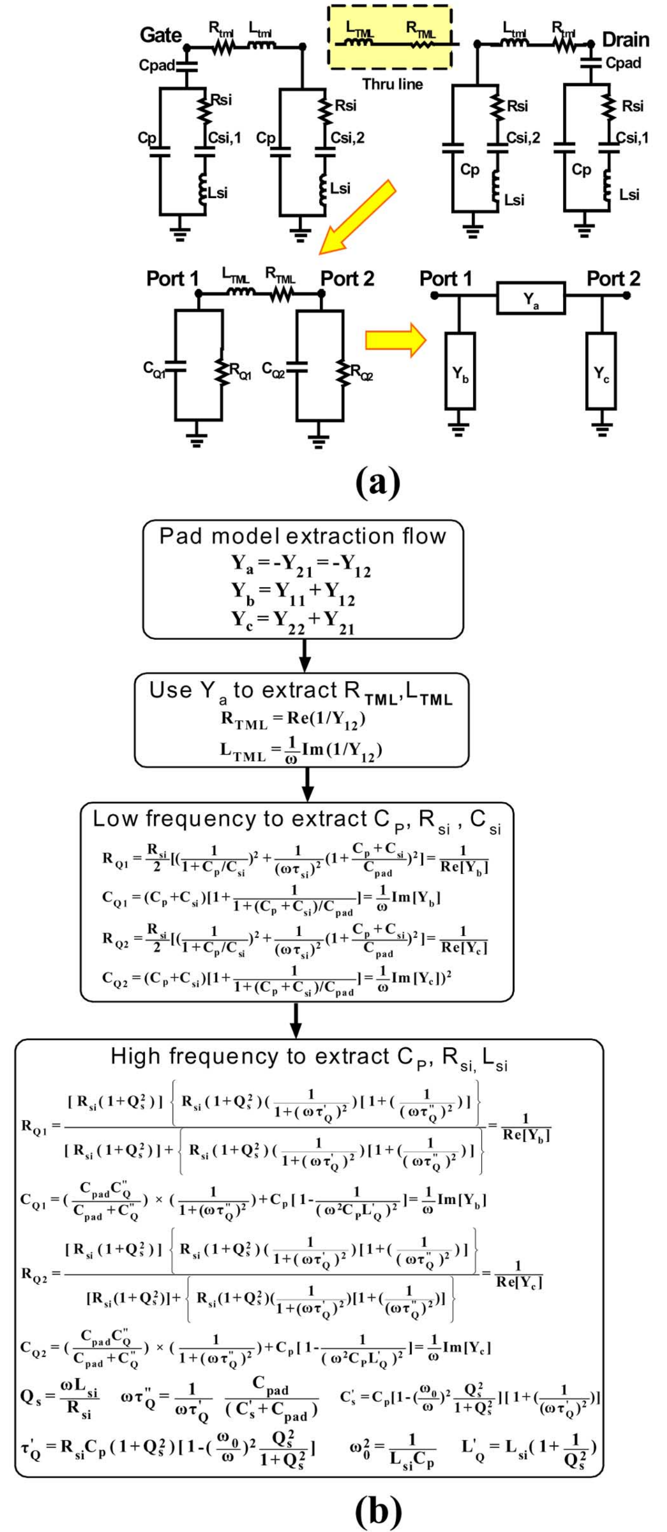


Fig. 5. (a) Schematic block diagram derived by circuit analysis theory to extract the circuit elements. (b) *RLC* circuit model parameter extraction flow.

B. Lossy Substrate RLC Parameter Extraction for Full Circuit Adopting MOSFET and Pads

Fig. 9 depicts the full-circuit model for sub-100-nm MOSFETs in which the *RLC* networks representing the lossy pads, lossy substrate, and transmission line are linked with the

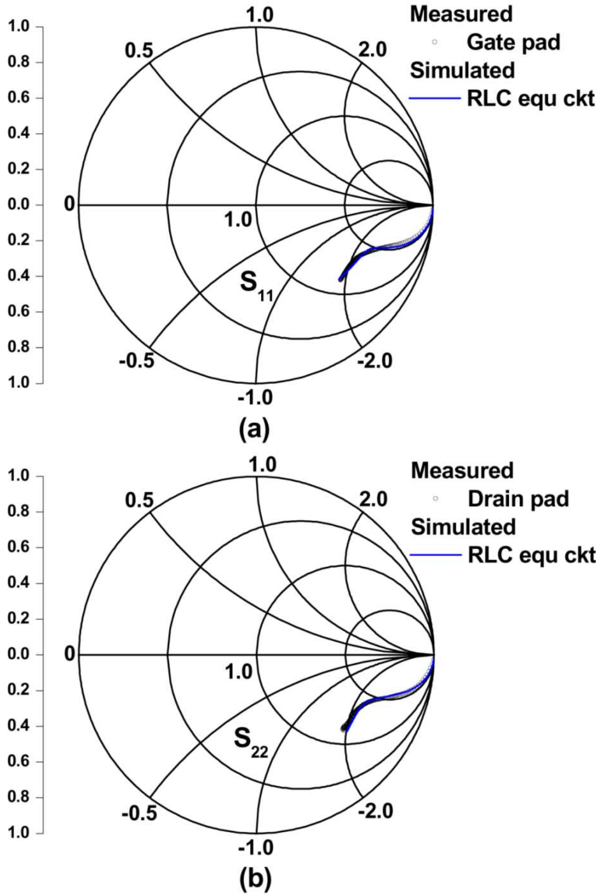


Fig. 6. Smith chart of measured S_{11} and S_{22} for open pad (symbol) and the good match by simulation (line) using the proposed *RLC* circuit. (a) S_{11} for gate pad as port-1. (b) S_{22} for drain pad as port-1.

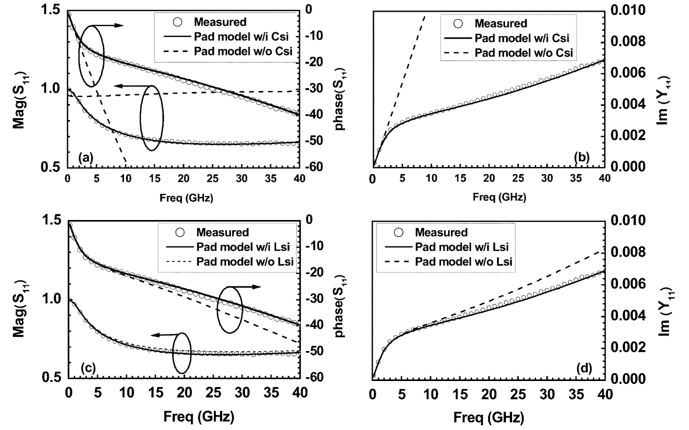


Fig. 7. Measured S_{11} and $\mathrm{Im}(Y_{11})$ for gate pad (symbol) and good fit by simulation (line) using the proposed *RLC* circuit. (a) S_{11} (magnitude and phase) and C_{Si} effect. (b) $\mathrm{Im}(Y_{11})$ and C_{Si} effect. (c) S_{11} (magnitude and phase) and L_{Si} effect. (d) $\mathrm{Im}(Y_{11})$ and L_{Si} effect.

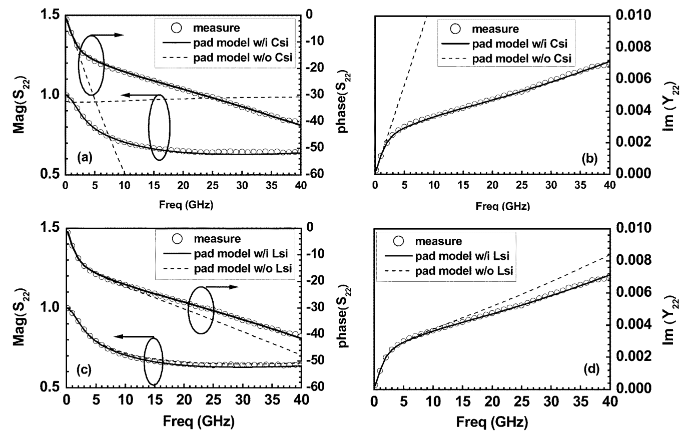
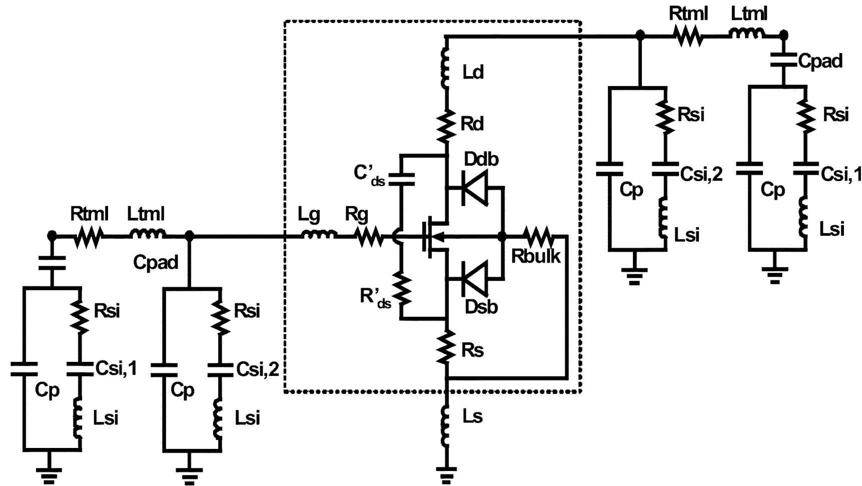


Fig. 8. Measured S_{22} and $\mathrm{Im}(Y_{22})$ for drain pad (symbol) and good fit by simulation (line) using the proposed *RLC* circuit. (a) S_{22} (magnitude and phase) and C_{Si} effect. (b) $\mathrm{Im}(Y_{11})$ and C_{Si} effect. (c) S_{22} (magnitude and phase) and L_{Si} effect. (d) $\mathrm{Im}(Y_{22})$ and L_{Si} effect.

intrinsic MOSFET (dashed box). For accurate RF modeling, the body of the intrinsic MOSFET is obviously different from the conventional one limited for dc modeling. The parasitic R and L associated with MOSFET's electrodes [gate–source–drain (G/S/D)] were extracted by the Z-parameter method [17], [18]. The extracted R_g, R_s, R_d, L_g, L_s, and L_d for various N are tabulated and attached with Fig. 9.

The layout of the intrinsic MOSFET in this study is a three-terminal configuration with source and bulk shorted internally. R_s is a series resistance of metal interconnection to the source and R_{bulk} accounts for the substrate network resistance. L_s represents the inductance of the metal line connecting the source/bulk common node to the ground pad, which is required for accurate high-frequency impedance simulation. Note that the lossy substrate *RLC* parameters were retuned and optimized through the flow shown in Fig. 1 for every MOSFET of various N to fit S-parameter, Y-parameter, and noise parameter before deembedding simultaneously. The difference from the pad-only *RLC* parameters in Fig. 4 and obvious dependence on N account for the additional lossy substrate effect introduced through M3–M1 of the MOSFET, which cannot be extracted from the conventional open-pad deembedding structure with the interconnection line terminated at M3, as mentioned. It is interesting to note that the larger N led to an increase of all three capacitance parameters, i.e., C_P, C_{Si1}, and C_{Si2}, while a decrease of R_{Si} representing an effective substrate resistance.

The full circuit for noise simulation contains the MOSFET body incorporating G/S/D electrodes' R and L as the intrinsic part and the proposed *RLC* networks at two ports as the extrinsic part. Besides the generally considered thermal noises, which are classified as the intrinsic drain current noise, intrinsic induced gate noise, and gate resistance induced excess noise to gate and drain terminals [19], pads' capacitive coupling and substrate loss are identified as more important factors responsible for the abnormally worse RF noise measured without effective deembedding. The R_g associated with the intrinsic MOSFET represents the distributed gate and channel resistances. For devices with a large finger number, e.g., $N = 72, R_g$ is effectively reduced and R_{tml} may become not negligible in determining $\mathrm{NF}_{\mathrm{min}}$. Regarding ultrahigh frequency, e.g., up to 40 GHz in this study, inductive impedance represented by L_g and L_{tml} become important parasitic elements, which can be evidenced by



N	Gate pad RLC parameters for Full circuit							
N	C_P(pF)	$C_{Si,1}$ (pF)	$C_{Si,2}$ (pF)	L_{Si} (nH)	R_{Si} (Ω)	L_{tml} (nH)	R_{tml} (Ω)	C_{pad}(pF)
6	0.01592	0.08429	0.12982	0.48796	376.799	0.03	0.25	0.19
18	0.03365	0.08933	0.16898	0.5482	306.9			
36	0.05221	0.1238	0.21156	0.56296	233.912			
72	0.06042	0.28958	0.23852	0.32032	202.631			

N	Drain pad RLC parameters for Full circuit							
N	C_P(pF)	$C_{Si,1}$ (pF)	$C_{Si,2}$ (pF)	L_{Si} (nH)	R_{Si} (Ω)	L_{tml} (nH)	R_{tml} (Ω)	C_{pad}(pF)
6	0.01464	0.13486	0.16153	0.35664	312.382	0.02	0.25	0.19
18	0.01599	0.23915	0.2141	0.46983	275.697			
36	0.0226	0.39648	0.32253	0.94743	234.547			
72	0.05235	0.71442	0.64582	3.0107	202.208			

N	R_g (Ω)	R_s(Ω)	R_d (Ω)	R_{bulk} (Ω)	L_g(pH)	L_d(pH)	L_s(pH)
6	26.56	1.23	1.26	166.43	33.8	18.6	15.7
18	11.05	0.83	0.42	87.04	31.4	16.4	16.1
36	6.27	0.73	0.21	67.19	32.7	17.5	15.5
72	3.98	0.67	0.10	57.26	30.3	15.1	16

Fig. 9. Full-circuit model with intrinsic MOSFET integrated with *RLC* network in which the R, L, and C parasitics account for lossy pad ($C_{\rm pad}$), lossy substrate ($R_{\rm Si}$, $L_{\rm Si}$, $C_{\rm Si}$, and C_p), and transmission line ($R_{\rm tml}$, $L_{\rm tml}$) connected to the gate and drain of the MOSFET. *RLC* model parameters are listed in the table.

S-parameters to be shown as follows. To certify the effectiveness and accuracy of the proposed *RLC* network for lossy pads and lossy substrate, the S-parameter was calculated by using the full-circuit schematics in Fig. 9 as the fundamental characteristics to be verified.

Fig. 10(a) and (b) demonstrates a good match in S_{11} and S_{22} (0.2–40 GHz) between the measurement and simulation for 80-nm n-MOSFETs with various N. It is revealed in the Smith chart that S_{11} and S_{22} are translated from capacitive to inductive mode under higher frequencies for the devices with large finger number ($N = 72$). It indicates the dominance of parasitic inductance existing in the transmission line connected to the gate electrode and pad (L_g and $L_{\rm tml}$). This result suggests the gate transmission-line effect plays an increasingly important role in high frequencies. The accuracy of the lossy substrate model by the proposed *RLC* network, as well as the effect played by $C_{\rm Si}$ and $L_{\rm Si}$, are further verified by magnitude and phase of S_{11} and S_{22}, ${\rm Im}(Y_{11})$, and ${\rm Im}(Y_{22})$ before deembedding for devices with various N.

Regarding the input characteristics at port-1, Fig. 11(a)–(d) indicates a good fit to the measured S_{11} (magnitude and phase) and ${\rm Im}(Y_{11})$ for $N = 6$. Figs. 12(a)–(d) and 13(a)–(d) demonstrate a good match with the measured S_{11} and ${\rm Im}(Y_{11})$ for $N = 18$ and $N = 36$, respectively. Again, $C_{\rm Si}$ plays a major role in fitting S- and Y-parameters of the full circuit structure in whole frequency range (0.2–40 GHz), while $L_{\rm Si}$ is becoming important in higher frequencies. As for the output feature at port-2, a good fit to the measured S_{22} (magnitude and phase) and ${\rm Im}(Y_{22})$ over a full frequency range (0.2–40 GHz) are shown in Figs. 14–16 corresponding to $N = 6, 18$, and 36, respectively. $C_{\rm Si}$ and L_{Si} effects are exactly consistent with those identified for port-1. The accuracy of the lossy substrate model is further justified by a good match with the measured ${\rm NF}_{\rm min}$ up to 18 GHz, as shown in Fig. 17(a)–(d) for all N.

The *RLC* network can predict the nonlinear frequency response of extrinsic noise and the excessively high ${\rm NF}_{\rm min}$ precisely. The nonlinear frequency response is originated from two obviously different slopes associated with lower and higher frequencies, respectively. In the lower frequency region, the effective substrate impedance is dominated by the capacitive mode represented by $C_{\rm Si}$. As for getting into a higher frequency region, the substrate impedance is dominated by the resistive mode represented by $R_{\rm Si}$. The capacitive mode substrate impedance will enhance the frequency dependence

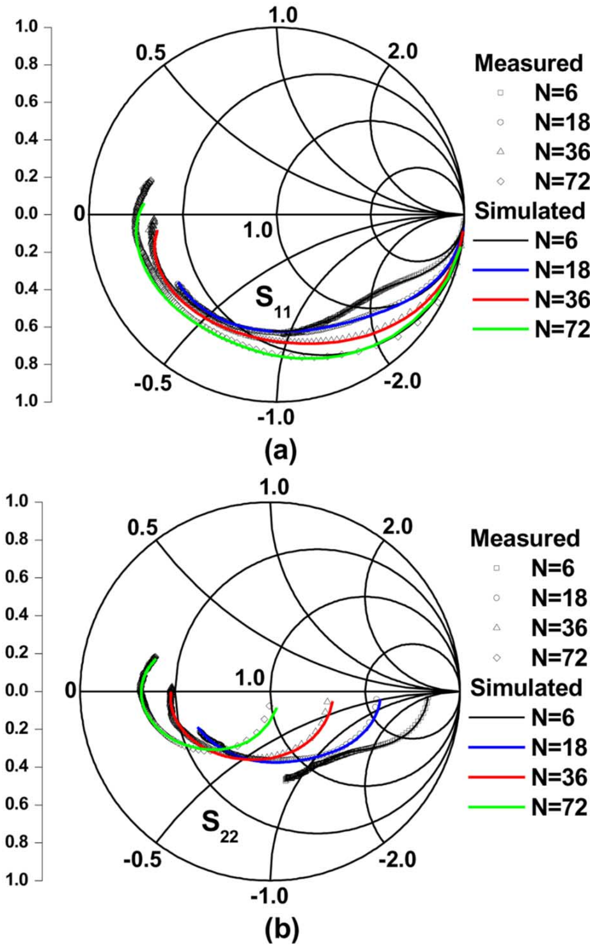


Fig. 10. Smith chart of measured S_{11} and S_{22} for full circuit with intrinsic MOSFET and pads. Good match achieved by simulation using the proposed *RLC* network. (a) S_{11}. (b) S_{22}. n-MOSFETs with $N = 6, 18, 36, 72$, and operating frequencies of 0.2–40 GHz. The symbol is the measured data and the line is the simulation.

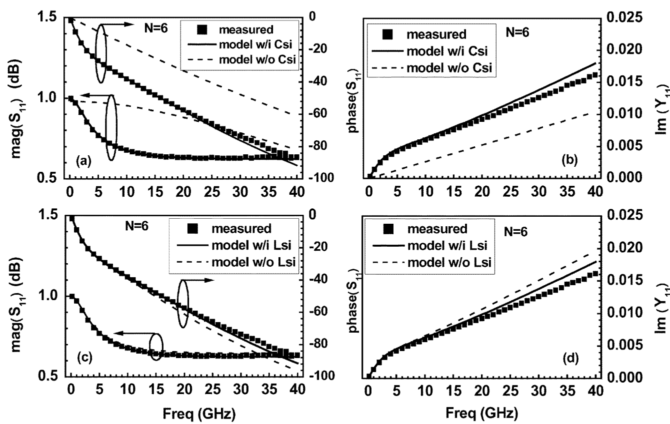


Fig. 11. 80-nm n-MOSFET with $N = 6$. Measured S_{11} and $\mathrm{Im}(Y_{11})$ before deembedding (symbol) and good fit by simulation (line) using the proposed full-circuit schematics. (a) S_{11} (magnitude and phase) and C_{Si} effect. (b) $\mathrm{Im}(Y_{11})$ and C_{Si} effect. (c) S_{11} (magnitude and phase) and L_{Si} effect. (d) $\mathrm{Im}(Y_{11})$ and L_{Si} effect.

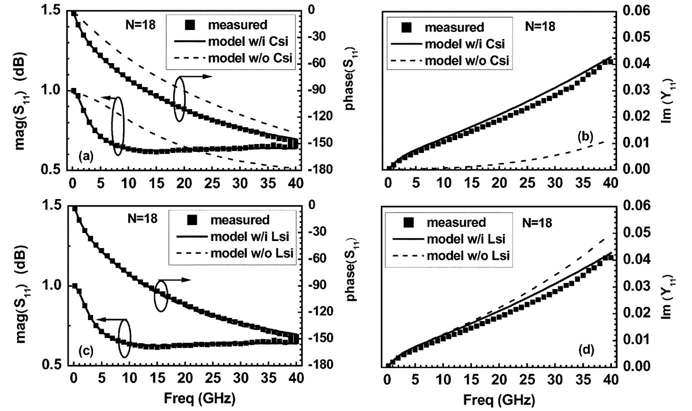


Fig. 12. 80-nm n-MOSFET with $N = 18$. Measured S_{11} and $\mathrm{Im}(Y_{11})$ before deembedding (symbol) and good fit by simulation (line) using the proposed full-circuit schematics. (a) S_{11} (magnitude and phase) and C_{Si} effect. (b) $\mathrm{Im}(Y_{11})$ and C_{Si} effect. (c) S_{11} (magnitude and phase) and L_{Si} effect. (d) $\mathrm{Im}(Y_{11})$ and L_{Si} effect.

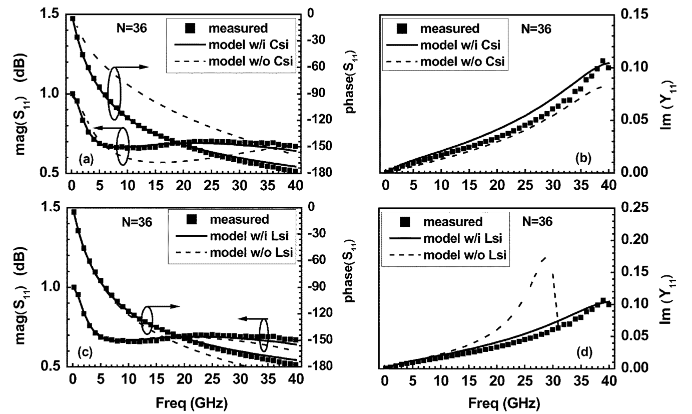


Fig. 13. 80-nm n-MOSFET with $N = 36$. Measured S_{11} and $\mathrm{Im}(Y_{11})$ before deembedding (symbol) and good fit by simulation (line) using the proposed full-circuit schematics. (a) S_{11} (magnitude and phase) and C_{Si} effect. (b) $\mathrm{Im}(Y_{11})$ and C_{Si} effect. (c) S_{11} (magnitude and phase) and L_{Si} effect. (d) $\mathrm{Im}(Y_{11})$ and L_{Si} effect.

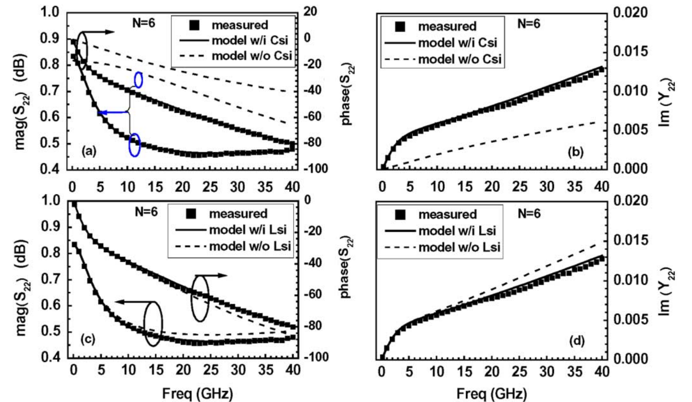


Fig. 14. 80-nm n-MOSFET with $N = 6$. Measured S_{22} and $\mathrm{Im}(Y_{22})$ before deembedding (symbol) and good fit by simulation (line) using the proposed full-circuit schematics. (a) S_{22} (magnitude and phase) and C_{Si} effect. (b) $\mathrm{Im}(Y_{22})$ and C_{Si} effect. (c) S_{22} (magnitude and phase) and L_{Si} effect. (d) $\mathrm{Im}(Y_{22})$ and L_{Si} effect.

of $\mathrm{NF}_{\min}$, which is the major cause responsible for the larger slope w.r.t. frequency and excessively high $\mathrm{NF}_{\min}$ emerging in the low-frequency region. The C_{Si} effect on $\mathrm{NF}_{\min}$ is clearly identified by comparison of two curves simulated with and without C_{Si} illustrated in Fig. 17. L_{Si} plays a minor effect on

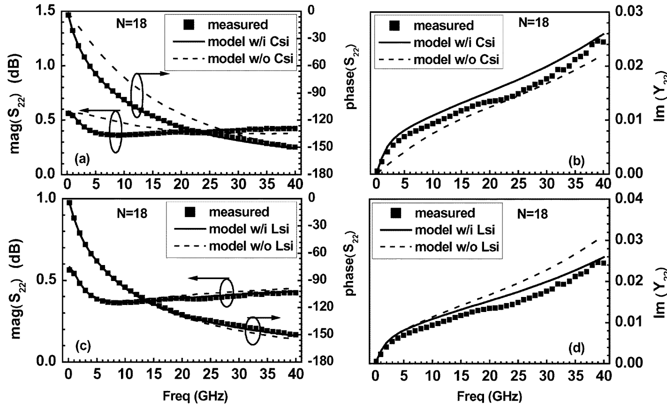


Fig. 15. 80-nm n-MOSFET with $N = 18$. Measured S_{22} and $\mathrm{Im}(Y_{22})$ before deembedding (symbol) and good fit by simulation (line) using the proposed full-circuit schematics. (a) S_{22} (magnitude and phase) and C_{Si} effect. (b) $\mathrm{Im}(Y_{22})$ and C_{Si} effect. (c) S_{22} (magnitude and phase) and L_{Si} effect. (d) $\mathrm{Im}(Y_{22})$ and L_{Si} effect.

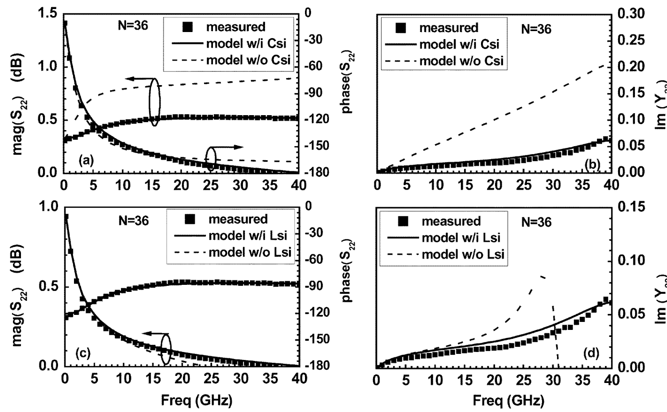


Fig. 16. 80-nm n-MOSFET with $N = 36$. Measured S_{22} and $\mathrm{Im}(Y_{22})$ before deembedding (symbol) and good fit by simulation (line) using the proposed full-circuit schematics. (a) S_{22} (magnitude and phase) and C_{Si} effect. (b) $\mathrm{Im}(Y_{22})$ and C_{Si} effect. (c) S_{22} (magnitude and phase) and L_{Si} effect. (d) $\mathrm{Im}(Y_{22})$ and L_{Si} effect.

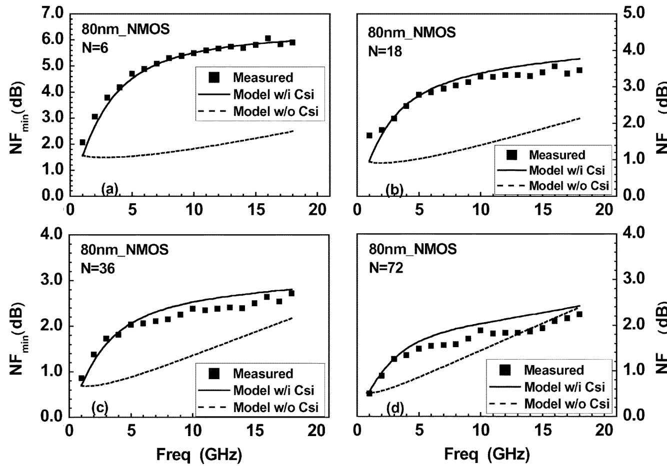


Fig. 17. Comparison of extrinsic $\mathrm{NF}_{\min}$ between measurement (symbol) and simulation (line) for 80-nm n-MOSFETs. (a) $N = 6$. (b) $N = 18$. (c) $N = 36$. (d) $N = 72$. C_{Si} effect is demonstrated for each device.

$\mathrm{NF}_{\min}$ (not shown), but it is an essential element for a precise match with the S- and Y-parameters, particularly to achieve correct phase in high frequencies, as shown previously.

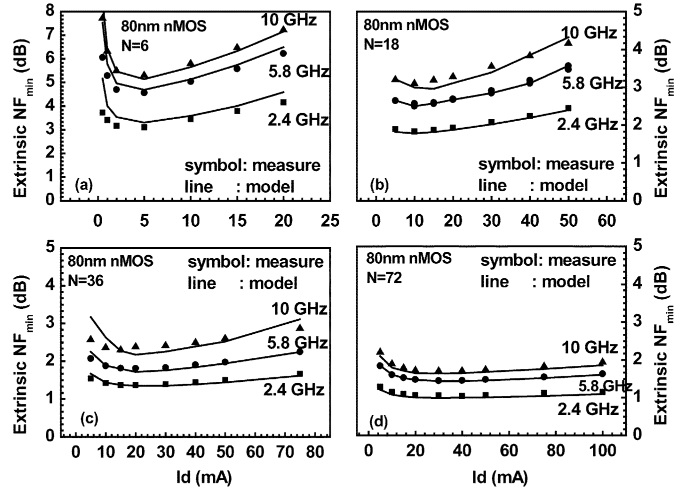


Fig. 18. Measured and modeled extrinsic $\mathrm{NF}_{\min}$ versus drain current I_d for 80-nm n-MOSFETs. (a) $N = 6$. (b) $N = 18$. (c) $N = 36$. (d) $N = 72$ under three frequencies, 2.4, 5.8, and 10 GHz.

Regarding the drain current dependence of $\mathrm{NF}_{\min}$, which is important for low power and low noise design, the comparison of extrinsic noise has been done among various N, as well as that between measurement and modeling employing the proposed lossy substrate network. Fig. 18 demonstrate good agreement achieved between the measured and modeled $\mathrm{NF}_{\min}$ under a wide range of drain currents ($I_d = 0.5$–100 mA) and frequencies (2.4, 5.8, 10 GHz) for all 80-nm n-MOSFETs ($N = 6, 18, 36, 72$). The move of minimum $\mathrm{NF}_{\min}$ toward higher I_d for larger N suggests the penalty of higher power by using larger devices. However, lossy substrate induced excess noise should be deembedded to get the truly intrinsic $\mathrm{NF}_{\min}$ for rigorous study and correct conclusion. One more concern about the large drain current reaching 100 mA for the largest device ($N = 72$) is the potential impact of the dc *I–V* heating effect. Verification by pulse *I–V* measurement indicates a lack of negative resistance in the saturation region and suggests a negligible heating effect. Actually, degradation of saturation current (I_{dsat}) and g_m was identified for the multifinger devices with larger N and can be modeled by an IR drop effect due to source series resistance induced voltage drop.

IV. Lossy Substrate Deembedding and Intrinsic Noise Extraction and Modeling

A. *Intrinsic MOSFET Model for DC and AC Simulation*

Through the extensive verification on the proposed lossy substrate model and the justification of accuracy in terms of the S-parameter, Y-parameter, and noise parameters, the lossy substrate deembedding can be done easily and precisely by removing the substrate *RLC* network from the full-circuit schematics in Fig. 9. The intrinsic noise can be calculated by using ADS simulation after the lossy substrate deembedding. Before that, the intrinsic MOSFET model accuracy needs to be verified in terms of *I–V*, *C–V*, and S- and Y-parameters through dc and high-frequency small-signal simulation. Fig. 19 presents a good match between the model and measurement in

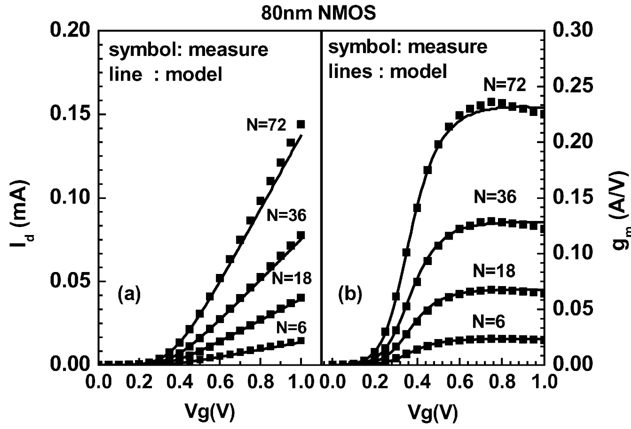


Fig. 19. Comparison of measured and modeled: (a) I_d versus V_g and (b) g_m versus V_g for 80-nm n-MOSFETs with $N = 6, 18, 36, 72$.

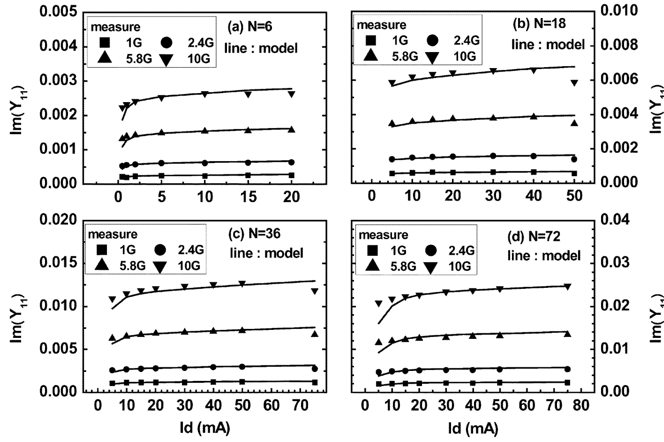


Fig. 20. Comparison of measured and modeled $\mathrm{Im}(Y_{11})$ after deembedding for 80-nm n-MOSFETs under frequencies of 1, 2.4, 5.8, and 10 GHz. (a) $N = 6$. (b) $N = 18$. (c) $N = 36$. (d) $N = 72$.

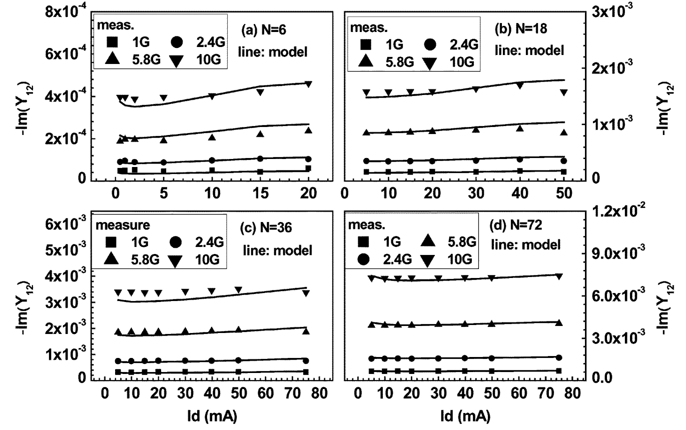


Fig. 21. Comparison of measured and modeled $\mathrm{Im}(Y_{12})$ after deembedding for 80-nm n-MOSFETs under frequencies of 1, 2.4, 5.8, and 10 GHz. (a) $N = 6$. (b) $N = 18$. (c) $N = 36$. (d) $N = 72$.

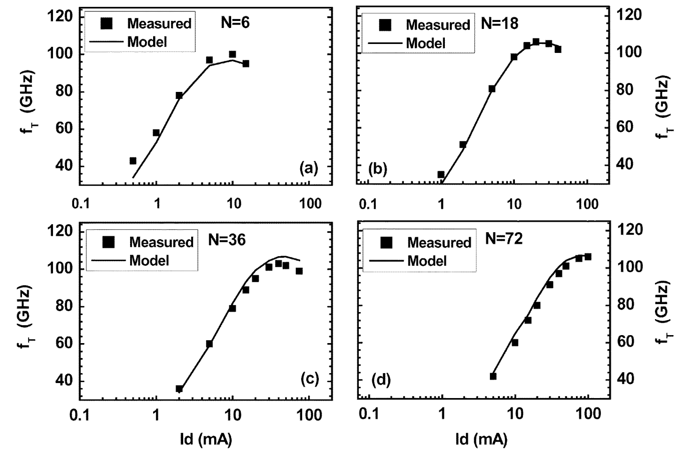


Fig. 22. Measured and modeled f_T versus I_d ($V_{\mathrm{ds}} = 1.0$ V) for 80-nm n-MOSFETs. (a) $N = 6$. (b) $N = 18$. (c) $N = 36$. (d) $N = 72$.

terms of I_d versus V_g and g_m versus V_g under $V_{\mathrm{ds}} = 1.0$ V for all 80-nm n-MOSFETs with different finger numbers ($N = 6, 18, 36, 72$). This good match validates the calibrated intrinsic model in aspect of mobility, short channel effects (SCEs), and parasitic resistances R_s and R_d. Regarding the intrinsic $\mathrm{NF}_{\min}$ of major concern, $C_{\mathrm{gs}}, C_{\mathrm{gd}}$, and R_g are three primary parameters accompanying with g_m to determine f_T and $\mathrm{NF}_{\min}$. The model accuracy in terms of $(C_{\mathrm{gs}}, C_{\mathrm{gd}})$ was generally verified by comparison of Y-parameters based on the equations of $\mathrm{Im}(Y_{11}) = \omega(C_{\mathrm{gs}} + C_{\mathrm{gd}})$ and $-\mathrm{Im}(Y_{12}) = \omega C_{\mathrm{gd}}$. Good agreement with the measurement in terms of $\mathrm{Im}(Y_{11})$, shown in Fig. 20 and $\mathrm{Im}(Y_{12})$ in Fig. 21, justifies the intrinsic model with calibrated gate capacitances.

One more rigorous verification on the intrinsic model accuracy was done by comparison of f_T extracted from the unit current gain, i.e., $H_{21}(f_T) = 1$. Fig. 22 reveals a promisingly good match with the measured f_T. The deviation is maintained below 5% for all devices with various N. The optimized f_T up to 110 GHz corresponding to $N = 18$ suggests the tradeoff among $C_{\mathrm{gs}}, C_{\mathrm{gd}}, g_m$, and other parasitics.

B. Intrinsic MOSFET Noise Model and Simulation

The accuracy of g_m and gate capacitances $(C_{\mathrm{gs}}, C_{\mathrm{gd}}, C_{gg})$ is a prerequisite to predict f_T, and accurate extraction of parasitic resistances at four terminals such as R_g, R_s, R_d, and R_{bulk} is essential to calculate $\mathrm{NF}_{\min}$ with sufficient precision. Regarding the thermal noise models for MOSFET high-frequency noise simulation, channel thermal noise and resistance induced excess noise are considered in this study. Channel thermal noise, also known as intrinsic drain current noise S_{id0}, was calculated by a modified Van der Ziel's model [20] given by (1)–(3) in which velocity saturation and channel length modulation (CLM) effects were implemented through the calibrated BSIM3 *I–V* model. Concerning the resistance induced excess noises, additional drain current noise ΔS_{id} and excess gate current noise ΔS_{ig} were calculated by (4) and (5), respectively [19]. Note that the intrinsic induced gate noise is considered negligible for an 80-nm MOSFET in the operating frequency up to 18 GHz [21]. Fig. 23(a) indicates the simulated intrinsic drain current noise S_{id0} free from R_g and full drain current noise $S_{\mathrm{id}} = S_{\mathrm{id0}} + \Delta S_{\mathrm{id}}$ including resistance induced excess noise for all N. Fig. 23(b) presents the additional drain current noise calculated by simulation and the comparison with the analytical model given by (4). Fig. 23(c) shows the white noise

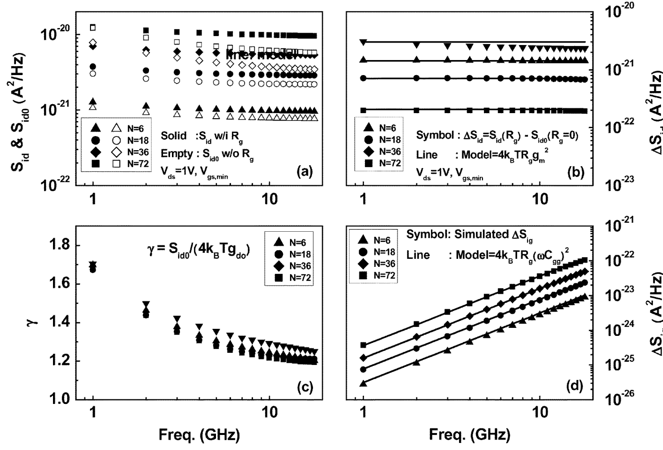


Fig. 23. Drain current noise and gate current noise simulated for 80-nm intrinsic n-MOSFETs after lossy substrate deembedding. Frequencies in 1–18 GHz and biases under $V_{\rm ds} = 1.0$ V, $V_{\rm gs,min}$. (a) Intrinsic and full drain current noise $S_{\rm id0}$ and $S_{\rm id}$. (b) Additional drain current noise $\Delta S_{\rm id}$ due to terminal resistances calculated by simulation and model $\Delta S_{\rm id} = 4k_BTR_gg_m^2$. (c) White noise γ factor for intrinsic drain current noise. (d) Resistance induced excess gate noise $\Delta S_{\rm ig}$ calculated by simulation and model $\Delta S_{\rm ig} = 4k_BTR_g(\omega C_{gg})^2$ for all N (6, 18, 36, 72).

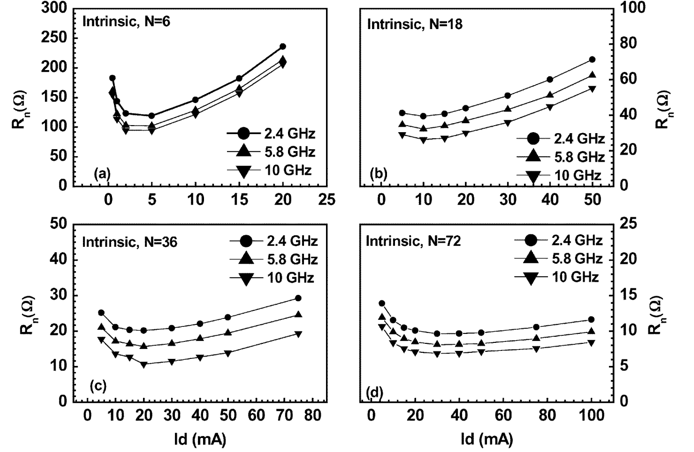


Fig. 24. Intrinsic R_n versus I_d ($V_{\rm ds} = 1.0$ V) for 80-nm n-MOSFETs after lossy substrate deembedding. $f = 2.4, 5.8, 10$ GHz. (a) $N = 6$. (b) $N = 18$. (c) $N = 36$. (d) $N = 72$.

factor γ calculated by $\gamma = S_{\rm id0}/4k_BTg_{do}$ from simulation, which reveals values of much larger than the long-channel value of 2/3 and decreasing with frequency from around 1.7 to 1.2 corresponding to 1–18 GHz. Fig. 23(d) indicates the resistance induced excess gate current noise from simulation and comparison with the model given by (5), which matches ω^2 dependence quite well as follows:

$$S_{\rm id} = \frac{\langle i_d^2 \rangle}{\Delta f} = 4k_BT \cdot g_{do} \cdot \frac{1 - u + u^2/3}{1 - u/2} \quad (1)$$

$$g_{do} = \frac{W_{\rm eff}}{L_{\rm eff}} \cdot \mu_{\rm eff} C_{\rm ox}(V_{\rm GS} - V_T) \quad (2)$$

$$u = \alpha V_{\rm DS}/V_{GT}$$

$$V_{GT} = (V_{GT} - V_T), \alpha : \text{body effect coefficient} \quad (3)$$

$$\Delta S_{\rm id} = 4k_BT \cdot R_g g_m^2 \quad (4)$$

$$\Delta S_{\rm ig} = 4k_BT \cdot R_g(\omega C_{gg})^2. \quad (5)$$

The intrinsic model with the above enhancement can simulate the bias and frequency dependence of noise resistance R_n, as shown in Fig. 24. The bias dependence of R_n translated to I_d dependence for various N can be approximated by the generally used analytical model $R_n = \gamma g_{do}/g_m^2 (g_{do} = \delta I_d/\delta V_d|_{vd\to 0})$ [11] in which the minimum of R_n corresponds to the maximum of g_m. However, the frequency dependence of R_n cannot be explained by the mentioned model, and bulk resistance induced potential fluctuation was proposed as the possible mechanism [22]. Both the measured extrinsic R_n and simulated intrinsic R_n reflected the frequency dependence, and the results suggest the bulk (substrate) *RC* coupling effect apparent in 1–10-GHz range. The deployment of $R_{\rm bulk}$ and junction capacitances (C_{jsb}, C_{jdb}) in the intrinsic MOSFET model accounts for the decrease of R_n with increasing frequency.

After extensive justification of the intrinsic MOSFET model in terms of mobility, SCE, and parasitic *RC* $(R_g, R_s, R_d, R_{\rm bulk}, C_{\rm gs}, C_{\rm gd}, C_{gg})$, etc., intrinsic $\rm NF_{min}$ of major interest are calculated by the calibrated intrinsic model.

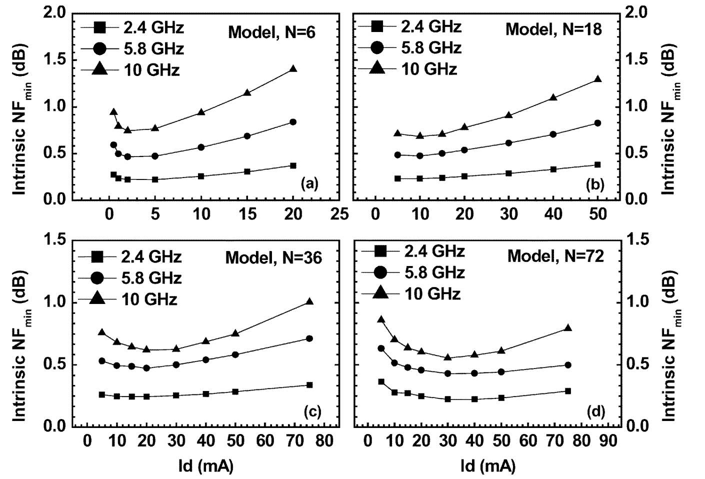


Fig. 25. Intrinsic $\rm NF_{min}$ versus I_d for 80-nm n-MOSFETs after lossy substrate deembedding. $f = 2.4, 5.8, 10$ GHz. (a) $N = 6$. (b) $N = 18$. (c) $N = 36$. (d) $N = 72$.

The results for various N under increasing I_d and frequencies are shown in Fig. 25. The minimum of $\rm NF_{min}$ can be pushed to as low as 0.6–0.7 dB at 10 GHz. Super-100-GHz f_T realized by the 80-nm n-MOSFET makes the major contribution and the trend matches with the Fukui formula [12]. The drain current I_d responsible for the minimal $\rm NF_{min}$ is another major concern for low power. This study suggests the penalty of higher I_d suffered by the bigger device using a larger N or the total width to achieve the same level of $\rm NF_{min}$. Of course, consideration of impedance matching in a real circuit is not covered in this scope.

V. Conclusion

An accurate lossy substrate model has been developed based on deployment of a new *RLC* network for sub-100-nm RF MOSFETs. The accuracy is justified by a good match with the measured S-parameters, Y-parameters, and noise parameters before deembedding. The accuracy of the intrinsic MOSFET model has been proven by good agreement in terms of $I_d, g_m, C_{gg}, C_{\rm gs}, C_{\rm gd}$, and f_T under a wide range of biasing currents and frequencies. The intrinsic noise of 80-nm

n-MOSFETs of various N can be precisely extracted by the lossy substrate deembedding using circuit simulation. The extracted intrinsic $\mathrm{NF}_{\min}$ as low as 0.6–0.7 dB at 1.0 V and 10 GHz reveals the advantage of low noise achievable by the sub-100-nm and super-100-GHz f_T RF n-MOSFETs. The study provides useful guideline for low-noise and low-power design by using RF CMOS technology.

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REFERENCES

[1] P. H. Woerlee, M. J. Knitel, R. van Langevelde, D. B. M. Klaassen, L. F. Tiemeijer, A. J. Scholten, and A. T. A. Zegers-van Duijnhoven, "RF-CMOS performance trends," *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1776–1782, Aug. 2001.

[2] J. C. Guo, W. Y. Lien, M. C. Hung, C. C. Liu, C. W. Chen, C. M. Wu, Y. C. Sun, and P. Yang, "Low-K/Cu CMOS logic based SoC technology for 10 Gb transceiver with 115 GHz fT, 80 GHz $f\max$ RF CMOS, high-Q MiM capacitor, and spiral Cu inductor," in *VLSI Tech. Dig. Symp.*, Jun. 2003, pp. 39–40.

[3] C. H. Chen, C. S. Chang, C. P. Chao, J. F. Kuan, C. L. Chang, S. H. Wang, H. M. Hsu, W. Y. Lien, Y. C. Tsai, H. C. Lin, C. C. Wu, C. F. Huang, S. M. Chen, P. M. Tseng, Y. T. Lin, C. F. Chang, H. J. Lin, J. C. Guo, G. J. Chern, D. Tang, and J. Y. C. Sun, "A 90 nm CMOS MS/RF based foundry SoC technology comprising superb 185 GHz f_T RFMOS and versatile, high-Q passive components for cost/performance optimization," in *Int. Electron Devices Meeting Tech. Dig.*, Dec. 2003, pp. 39–42.

[4] G. Baldwin, J. Ai, K. Benaissa, F. Chen, P. R. Chidambaram, S. Ekbote, S. Ghneim, S. Liu, C. Machala, F. Mehrad, D. Mosher, G. Pollack, T. Tran, B. Williams, J. Yang, S. Yang, and F. S. Johnson, "90 nm CMOS RF technology with 9.0 V I/O capability for single-chip radio," in *VLSI Tech. Dig. Symp.*, Jun. 2003, pp. 87–88.

[5] W. Jeamsaksiri, A. Mercha, J. Ramos, D. Linten, S. Thijs, S. Jenei, C. Detcheverry, P. Wambacq, R. Velghe, and S. Decoutere, "Integration of a 90 nm RF CMOS technology (200 GHz $f_{\max}$–150 GHz f_T NMOS) demonstrated on a 5 GHz LNA," in *VLSI Tech. Dig. Symp.*, Jun. 2004, pp. 100–101.

[6] L. F. Tiemeijer, R. J. Havens, R. deKort, A. J. Scholten, R. van Langevelde, D. B. M. Klaassen, G. T. Sasse, Y. Bouttement, C. Petot, S. Bardy, D. Gloria, P. Scheer, B. Van Haaren, C. Clement, J.-F. Larchanche, I.-S. Lim, A. Zlotnicka, and A. Duvallet, "Record RF performance of standard 90 nm CMOS technology," in *Int. Electron Devices Meeting Tech. Dig.*, Dec. 2004, pp. 441–444.

[7] J. Pekarik, D. Greenberg, B. Jagannathan, R. Groves, J. R. Jones, R. Singh, A. Chinthakindi, X. Wang, M. Breitwisch, D. Coolbaugh, P. Cottrell, J. Florkey, G. Freeman, and R. Krishnasamy, "RFCMOS technology from 0.25 μm to 65 nm: The state of the art," in *Proc. Custom Integrated Circuit Conf.*, 2004, pp. 217–224.

[8] X. Jin, J. J. Ou, C. H. Chen, W. Liu, M. J. Deen, P. R. Gray, and C. Hu, "An effective gate resistance model for CMOS RF and noise modeling," in *Int. Electron Devices Meeting Tech. Dig.*, Dec. 1998, pp. 961–964.

[9] C. E. Bilber, M. L. Schmatz, T. Morf, U. Lott, E. Morifuji, and W. Bachtold, "Technology independent degradation of minimum noise figure due to pad parasitics," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 1998, vol. 1, pp. 145–148.

[10] J. C. Guo, C. H. Huang, W. Y. Lien, and C. M. Wu, "A simple transmission line de-embedding method for accurate RF CMOS noise modeling," in *IEEE RFIC Tech. Dig.*, Jun. 2004, pp. 607–610.

[11] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 1st ed. Cambridge, U.K.: Cambridge Univ. Press, 1998, ch. 10.

[12] H. Fukui, "Optimal noise figure of microwave GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. ED-26, no. 7, pp. 643–650, Jul. 1979.

[13] H. A. Haus and R. B. Adler, *Circuit Theory of Linear Noisy Networks*. Cambridge, MA: MIT Press, 1959.

[14] H. Hillbrand and P. H. Russer, "An efficient method for computer-aided noise analysis of linear amplifier networks," *IEEE Trans. Circuits Syst.*, vol. CAS-23, no. 4, pp. 235–238, Apr. 1976.

[15] C.-H. Chen and M. J. Deen, "A general procedure for high-frequency noise parameter de-embedding of MOSFETs by taking the capacitive effects of metal interconnections into account," in *Proc. IEEE Int. Compon., Manuf. Technol. Symp.*, Kobe, Japan, Mar. 19–22, 2001, pp. 109–114.

[16] J. C. Guo and Y. M. Lin, "A lossy substrate model for sub-100 nm, super-100 GHz f_T RF CMOS noise extraction and modeling," in *IEEE RFIC Tech. Dig.*, Jun. 2005, pp. 145–148.

[17] S. Lee and H. K. Yu, "Parameter extraction technique for the small-signal equivalent circuit model of microwave silicon MOSFETs," in *Proc. High-Speed Semicond. Devices Circuits*, 1997, pp. 182–199.

[18] S. Lee, H. K. Yu, C. S. Kim, J. G. Koo, and K. S. Nam, "A novel approach to extracting small-signal model parameters of silicon MOSFET's," *IEEE Microw. Guided Wave Lett.*, vol. 7, no. 3, pp. 75–77, Mar. 1997.

[19] A. J. Scholten, L. F. Tiemeijer, R. van Langevelde, R. J. Havens, A. T. A. Zegers-van Duijnhoven, and V. C. Venezia, "Noise modeling for RF CMOS circuit simulation," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 618–632, Mar. 2003.

[20] A. van der Ziel, "Thermal noise in field-effect transistors," *Proc. IRE*, vol. 50, no. 8, pp. 1808–1812, Aug. 1962.

[21] S. Asgaran, M. J. Deen, and C.-H. Chen, "Analytical modeling of MOSFETs channel noise and noise parameters," *IEEE Trans. Electron Devices*, vol. 51, no. 12, pp. 2109–2114, Dec. 2004.

[22] J.-S. Goo, S. Donati, C.-H. Choi, Z. Yu, T. H. Lee, and R. W. Dutton, "Impact of substrate resistance on drain current noise in MOSFETs," in *Proc. SiSPAD*, 2001, pp. 182–185.

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