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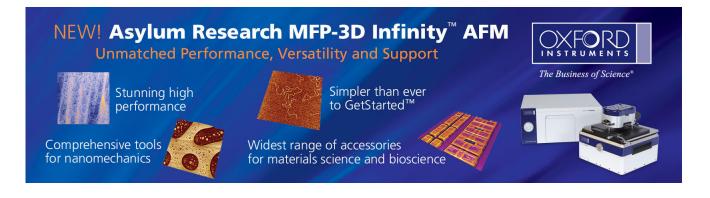
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Extraction of nitride trap density from stress induced leakage current in silicon-oxide-nitride-oxide-silicon flash memory

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The authors propose a technique to extract a silicon nitride trap density from stress induced leakage current in a polycrystalline silicon-oxide-nitride-oxide-silicon flash memory cell. An analytical model based on the Frenkel-Poole emission is developed to correlate a nitride trap density with stress induced leakage current. The extracted nitride trap density is 7.0×10^{12} cm⁻² eV⁻¹. They find that nitride trapped charges have a rather uniform distribution in an energy range of measurement (~0.2 eV). © 2006 American Institute of Physics. [DOI: 10.1063/1.2360180]

Polycrystalline silicon-oxide-nitride-oxide-silicon (SONOS) flash memories have received much interest in recent years for their simpler fabrication process and better scalability as compared to conventional floating gate flash memory.^{1,2} For SONOS cells, programed charges are stored in silicon nitride traps. The cell programming and retention characteristics are intimately related to nitride trap characteristics. Much research effort with respect to silicon nitride process optimization has been conducted to improve nitride trap properties. However, nitride trap characterization techniques are still very limited at present. Lundström and Svensson estimated a nitride trap density with a direct tunneling model.³ Paulsen et al. employed a low-frequency (<1 kHz) charge pumping technique to separate nitride traps from interfacial oxide traps by a difference in their time constants.⁴ Later, they extracted a nitride trap density from reverse modeling of threshold voltage (V_t) retention loss by combining trap-to-band tunneling and thermal excitation of trapped electrons in a nitride.^{5,6} All the above methods, however, are restricted to ultrathin bottom oxides (1.5-2.5 nm). For today's SONOS cells, for example, nitride-read-onlymemory (NROM) (Ref. 7) or Nitride-based multiple bits/cell (Nbit) (Ref. 8) technology, a thicker bottom oxide is usually employed to improve data retention. No appropriate nitride trap characterization methods are available for these cells.

In this work, we observe a high-voltage stress induced gate leakage current in a large area SONOS capacitor. An analytical model to extract a nitride trap density from the stress induced leakage current is developed. The effects of programming window (ΔV_t) and stress condition on the extraction result are evaluated. The nitride trap energy distribution is also profiled.

The SONOS capacitors used in this work have a 9 nm top oxide, a 6 nm silicon nitride, and a 5 nm bottom oxide. The capacitor area is $500 \times 500 \ \mu \text{m}^2$. Uniform Fowler-Nordheim (FN) injection is employed for programming. The measured program-state gate leakage current versus retention time before and after a FN stress is shown in Fig. 1(a). The FN stress is performed at $V_g = -20$ V for 1500 s. The pro-

gram V_t window is 3 V. The corresponding V_t retention loss is shown in Fig. 1(b). A significant stress induced leakage current (SILC) is observed in Fig. 1(a). Unlike in a metal oxide semiconductor capacitor, the SILC in a SONOS exhibits a unique two-stage time dependence. In the first stage, the SILC exhibits a dc-like characteristic and in the second stage it follows a 1/t time dependence. Our numerical simulation has shown that the first stage leakage current is limited by stress created oxide traps and the second stage is determined by the Frenkel-Poole (FP) emission of nitride trapped electrons.⁹ According to the FP emission model, the nitride trapped charge emission time is

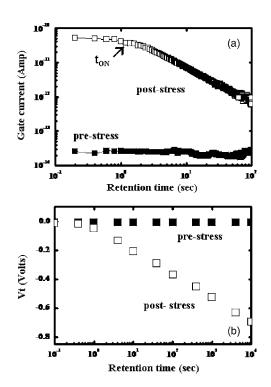


FIG. 1. (a) Measured gate leakage current in a large area SONOS (500 \times 500 μ m²) at V_g =0 V. The stress condition is V_g =-20 V for 1500 s. Both devices are programed to an identical threshold voltage window of 3 V. (b) Corresponding V, retention loss for the two samples.

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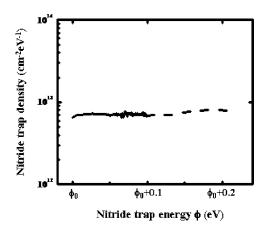


FIG. 2. Extracted nitride trap density distribution vs relative nitride trap energy. ϕ_0 is estimated to be 0.8 eV (Ref. 9).

$$\tau_e(A^*T^2)^{-1}\exp((\phi - q(qE/\pi\varepsilon)^{1/2})/kT) = \tau' \exp(\phi/kT),$$
(1)

where A^* is the Richardson constant, ϕ is the nitride trap energy measured from the conduction band edge, *E* is the electric field, τ' is the proportionality constant, and other variables have their usual definitions. In the FP emission limited condition (second stage), the electron occupation factor (*f*) of a nitride trap state with an energy ϕ has a retention time dependence as follows;^{5,6}

$$f(\phi) = \exp\left[-t/\tau_e(\phi)\right] = \exp\left[(-t/\tau')\exp(-\phi/kT)\right].$$
(2)

Because the above double exponential changes abruptly from 0 to 1 around $\phi_f = (kT) \ln(t/\tau')$, $f(\phi)$ can be approximated by a step function at $\phi = \phi_f$ and thus ϕ_f is referred to as the FP emission front hereafter. This approximation translates into a "clear-cut" picture; at a certain time *t*, trap states above the emission front ϕ_f are completely emptied while the states below ϕ_f are occupied by electrons. The FP emission front moves downward in SiN band gap with a speed of $d\phi_f/dt = kT/t$, or 2.3kT/decade of time. The nitride charge leakage current in the second stage therefore can be expressed as

$$I_g = AqN_t(\phi_f)d\phi_f/dt = AqN_t(\phi_f)kT/t$$
(3a)

and the nitride trap density can be extracted as

$$N_t(\phi_f) = I_g t / AqkT. \tag{3b}$$

Since the emission front stays almost unchanged in the first stage ($\phi_f = \phi_0$) and begins to move at the onset time (t_{on}) of the second stage with a constant speed in a log(t) scale, the relationship between ϕ_f and retention time t is readily obtained,

$$\phi_f = \phi_0 + kT \ln(t/t_{\rm on}),\tag{4}$$

where ϕ_0 is the emission front in the first stage and is determined by the total amount of programed charges. From our numerical simulation, ϕ_0 is estimated to be 0.8 eV for the present SONOS structure and programming window.⁹ From Eqs. (3) and (4), the nitride trap density is characterized, as shown in Fig. 2. The solid line is directly from the SILC [Fig. 1(a)] and the dashed line is extrapolated from the V_t shift [Fig. 1(b)]. Notably, Fig. 2 reveals that the trapped charges have a rather uniform distribution over an energy

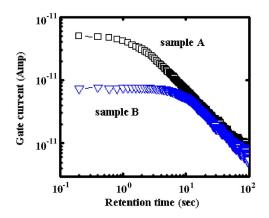


FIG. 3. Measured SILC in two differently stressed samples. Sample A is stressed at V_g =-20 V for 1500 s and sample B is for 5 s. The programming window is 3 V.

To further verify our nitride trap profiling technique, we change the FN stress condition and programming window. Figure 3 shows the SILC for two different FN stresses. The two samples have the same programming window and thus the same ϕ_0 . It can be shown that the effective time for nitride trapped charges at the emission front to escape from the ONO film^{9,10}

$$\tau_{\rm eff} = \frac{\tau_e(\phi_f) + \tau_c(\phi_f)}{\tau_c(\phi_f)} \tau_{\rm ox} \approx \frac{\tau_e(\phi_f)}{\tau_c(\phi_f)} \tau_{\rm ox},\tag{5}$$

where $\tau_e(\phi_f)$ and $\tau_c(\phi_f)$ represent the electron emission time and capture time between the emission front and the nitride conduction band. τ_{ox} is the conduction band electron tunneling time via stress induced oxide traps. The lightly stressed sample (B) has a lower first-stage dc leakage because of less oxide trap creation and thus a longer τ_{ox} . It is worth pointing out that the SILC in the two samples (A and B) converges in the second stage. The reason is that the ϕ_f of the two samples at a certain time in the second stage is only shifted by $KT \ln(t_{on}(B)/t_{on}(A)) \sim 0.06 \text{ eV}$. As mentioned earlier, the nitride trap density N_t is almost a constant in the measurement range. The leakage current, which is proportional to N_t [Eq. 3], is therefore nearly the same in the second stage regardless of stress conditions.

In addition, the SILC for different program windows is shown in Fig. 4. The program window is 3 V for sample A and is 2.5 V for sample C. Sample A has a smaller ϕ_0 for more programed charges. According to the Shockley-Read-

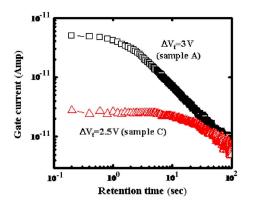


FIG. 4. Measured SILC for two different programming windows. Samples A and C are stressed under the same condition ($V_x = -20$ V for 1500 s) but to IP: have program windows of 3 and 2.5 V, respectively.

TABLE I. Extracted nitride trap density from samples A, B, and C, respectively, by using our technique.

Sample	$N_t ({\rm cm}^{-2}{\rm eV}^{-1})$
А	7.1×10^{12}
В	6.3×10^{12}
С	6.2×10^{12}

Hall theory, $\tau_e / \tau_c \propto \exp(\phi/kT)$ and the difference in ϕ_0 between samples A and C can be estimated from the ratio of the SILC in the first stage, i.e.,

SILC(first stage)
$$\propto 1/\tau_{\rm eff} \propto \exp(-\phi_0/kT)$$

and

$$\phi_0(A) - \phi_0(C) = -kT \ln(\text{SILC}(A)/\text{SILC}(C)).$$
(6)

The ϕ_0 difference is still small. Consequently, samples A and C have almost the same leakage current in the second stage because $N_t(\phi)$ can be considered as a constant for such small ϕ_0 difference. The extracted nitride trap density from samples A–C is listed in Table I. The extracted result is in reasonably good agreement without regard to stress condition and programming window.

In summary, a simple and reliable nitride trap profiling technique for a thicker bottom oxide SONOS is developed.

We find that a SILC in a SONOS exhibits a distinguished two-stage feature. The nearly 1/t dependence in the second stage suggests that the nitride traps have a uniform energy distribution. The extracted nitride trap density is around 7.0 $\times 10^{12}$ cm⁻² eV⁻¹

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- ²M. H. White, D. A. Adams, J. R. Murray, S. Wrazien, Yijie Zhao, Yu Wang, B. Khan, W. Miller, and R. Mehrotra, *Symposium on NVM Technology* (2004), p. 51.
- ³K. I. Lundström and C. M. Svensson, IEEE Trans. Electron Devices **19**, 826 (1972).
- ⁴R. E. Paulsen, R. R. Siergiej, M. L. French, and M. H. White, IEEE Electron Device Lett. **13**, 627 (1992).
- ⁵Y. Yang and M. H. White, Solid-State Electron. **44**, 948 (2000).
- ⁶Yu Wang and M. H. White, Solid-State Electron. 49, 97 (2005).
- ⁷B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, and D. Finzi, IEEE Electron Device Lett. **21**, 543 (2000).
- ⁸Tahui Wang, W. J. Tsai, S. H. Gu, C. T. Chan, C. C. Yeh, N. K. Zous, T. C. Lu, Sam Pan, and Chih-Yuan Lu, Tech. Dig. Int. Electron Devices Meet. **2003**, 169.
- ⁹S. H. Gu, Tahui Wang, Wen-Pin Lu, Yen-Hui Joseph Ku, and Chih-Yuan Lu, IEEE Trans. Electron Devices (to be published).
- ¹⁰C. Main, S. Reynolds, and R. Brüggemann, Phys. Status Solidi C 5, 1194 (2004).

¹M. H. White, IEEE Circuits Devices Mag. 16, 22 (2000).