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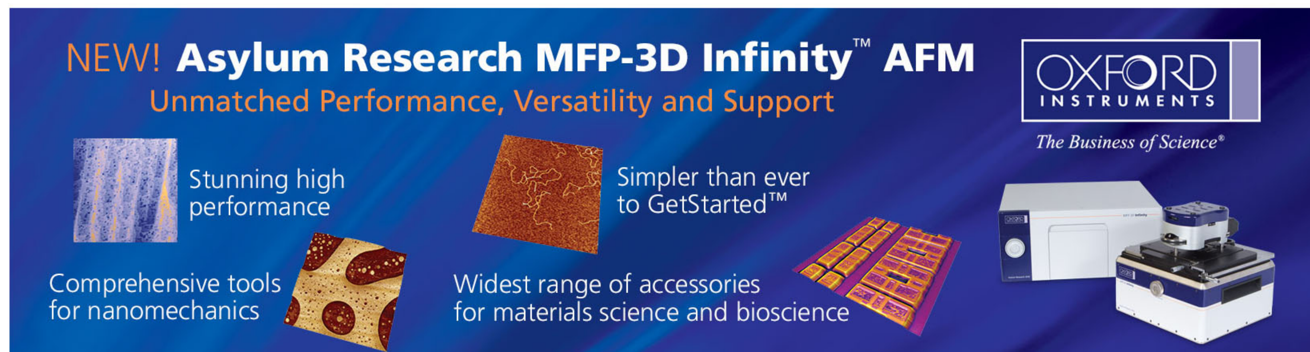

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Improved memory window for Ge nanocrystals embedded in SiON layer

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The formation of germanium (Ge) nanocrystals embedded in silicon oxygen nitride (SiON) is proposed for charge storage elements in this work. The Ge nanocrystals can be nucleated after the oxidation process of silicon germanium nitride (SiGeN) layer at high temperatures. Compared to the control samples of Ge nanocrystals/SiO_2/Si structure and SiON/Si stack memory, the proposed Ge nanocrystals/SiON/Si memory obtained superior memory window, even larger than the typical sum of both. It is considered that the extra interface trap states between Ge and SiON film were generated as Ge nanocrystals were embedded in SiON layer. © *2006 American Institute of Physics*.
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In the past few years, the portable electronic devices have significantly impacted the market of consumer electronics. Because of the low working voltage and nonvolatility, the selection of storage media for most portable electronic devices is the flash memory which almost bases on the structure of the continuous floating gate (FG).[1,2] To date, the stacked-gate FG device structure continues to be the most prevailing nonvolatile memory implementation and is widely used in both independent and embedded memories. The invention of FG memory impacts more than the replacement of magnetic-core memory and creates a moment of portable electronic systems. Despite a huge achievement in commercialization, conventional FG devices have some drawbacks.[2] Hence, the disserted stored center concept for charge trapping layer was proposed, such as poly-Si/oxide/nitride/oxide/Si (SONOS) and nanocrystals. In such proposed nonvolatile memory devices, charges are not stored in a continuous FG poly-Si layer but instead in a discrete, mutually isolated layer. Also, the proposed nonvolatile device can avoid the charge leakage and lower the power consumption when tunneling oxide is thinner.[3–5] The self-assembling of silicon or germanium nanocrystals embedded in SiO_2 layers has been widely studied, and strong memory effects in metal-oxide-semiconductor devices were reported.[3,6,7] Recently, different charge storage elements have been studied to achieve the robust distributed charge storage.[8–13] Whereas research on nanocrystal memory has mainly focused on Si and Ge nanocrystals, it is also of interest for its smaller band gap, inducing a theoretically better and faster writing/erasing times and reliability.[14,15] In this contribution, the SiGeN was investigated to be a self-assembling layer.[16] The self-assembling layer of SiGeN, fabricated by the directly depositing using plasma enhanced chemical vapor deposition (PECVD) system. The following amorphous silicon (*a*-Si) was also deposited in one chamber system by using PECVD. The structure with Ge embedded SiON layer exhibits obvious charge trapping memory effects under electrical measurements.

First, a 5-nm-thick thermal oxide was grown as the tunnel oxide on *p*-type Si substrate by dry oxidation in an atmospheric pressure chemical vapor deposition furnace. Subsequently, 20 nm silicon nitride, silicon germanium, and silicon germanium nitride thin film were prepared on tunnel oxide, respectively. The sequential *a*-Si layer was also deposited. The oxidation process was performed to fabricate the oxygen-incorporated SiO_2 to serve as blocking oxide, and the oxidation temperature was 900 °C. Furthermore, the SiGe-based thin film layer is also oxidized to nucleate the Ge nanocrystals during the blocking oxide formation. Afterward, a steam densification at 900 °C was also performed for 180 s to densify the blocking oxide. The deposition of the charge trapping film was kept at 200 °C in a low pressure of 0.6 mTorr. The low pressure of 0.6 mTorr during deposition leads the mean free path of electrons to be increased and to improve the uniformity of the thin film. Next, the high-temperature thermal oxidation was performed in the thermal furnace in oxygen ambient. The sequent steam oxidation was performed to improve the quality of oxidized *a*-Si layer as the blocking oxide. Finally, the Al gate was patterned and sintered to form a metal-oxide-insulator-oxide-silicon (MOIOS) structure

The MOIOS memory device is utilized to capture the injected carriers from the channel, which causes a variation in the threshold voltage of the memory device. The blocking oxide is utilized to prevent the carriers of gate electrode from injecting into the charge trapping layer by Fowler-Nordheim

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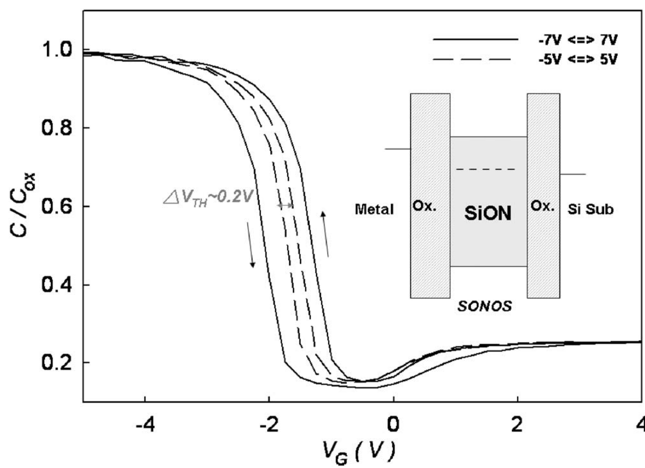

FIG. 1. Capacitance-voltage (C-V) hysteresis of the MOIOS structure for SiON as charge trap center. The electrical C-V measurements are performed by bidirectional voltage sweeping (1) from 7 to −7 V and from −7 to 7 V and (2) from 5 to −5 V and from −5 to 5 V. The insert is the diagram for charge trapping center for SiON layer.

tunneling. Figure 1 shows the capacitance-voltage (C-V) hysteresis of the MOIOS structure for SiON as charge trapping layer. The electrical C-V measurements were performed by bidirectional voltage sweeping. The sweeping conditions were split as follows: (I) operated from 7 to −7 V and vice versa and (II) operated from 5 to −5 V and vice versa. It is clearly shown in Fig. 1 that the threshold-voltage shift (memory window ΔV_{th}) of the MOIOS structure is prominent for 900 °C oxidation. When the device is programed, the electrons directly tunnel from the Si substrate through the tunnel oxide and are trapped in the forbidden gap of silicon nitride layer. For the erasing process, the holes may tunnel from the valence band of the Si substrate and recombine with the electrons trapped in the SiON layer. The memory window of 0.2 V is observed under an operation of 5 V. However, the C-V hysteresis of the MOIOS structure for Ge nanocrystal is shown as Fig. 2. The electrons (holes) directly tunnel from the Si substrate through the tunnel oxide and are trapped (detrapped) in the forbidden gap of Ge nanocrystal. The larger memory window for Ge nanocrystal embedded in

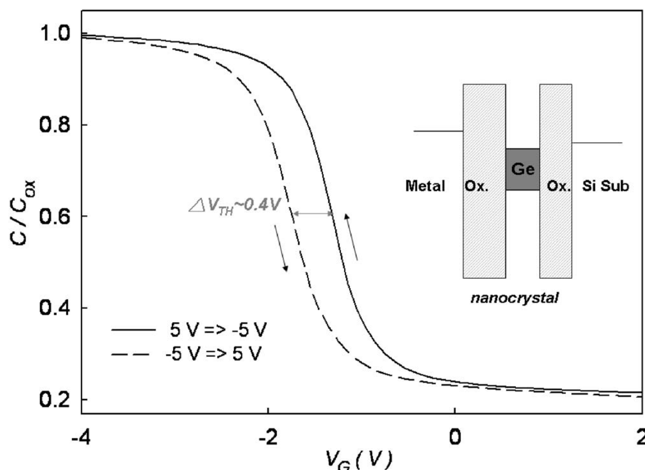

FIG. 2. Capacitance-voltage (C-V) hysteresis of the MOIOS structure for Ge nanocrystal embedded in SiO_2 layer as charge trap center. The electrical C-V measurements are performed by bidirectional voltage sweeping from 5 to −5 V and from −5 to 5 V. The insert is the diagram for charge trapping center for Ge nanocrystal embedded in SiO_2 layer.

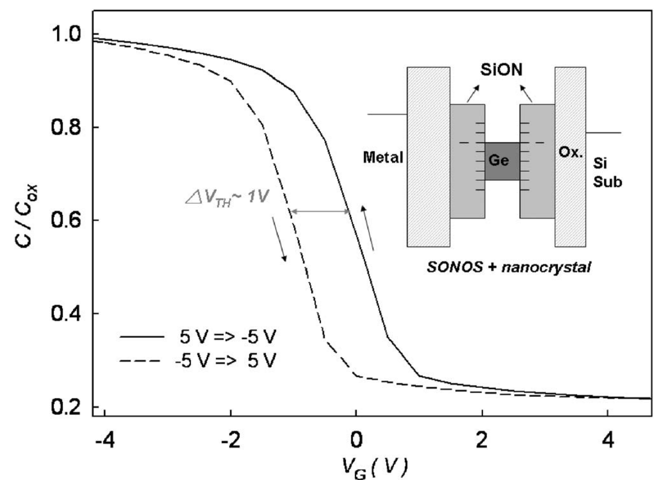

FIG. 3. Capacitance-voltage (C-V) hysteresis of the MOIOS structure for Ge nanocrystal embedded in SiON layer as charge trap center. The electrical C-V measurements are performed by bidirectional voltage sweeping from 5 to −5 V and from −5 to 5 V. The insert is the diagram for charge trapping center for Ge nanocrystal embedded in SiON layer.

SiO_2 layer is obtained than the previous one. This is contributed from the trap state for nanocrystals surrounding the dielectric. Under an operation of 5 V, a memory window of 0.4 V is exhibited after a cycle of programming and erasing process.

The proposed MOIOS structure via a way of oxidizing SiGeN layer as charge trapping layer is also measured under the same operation conditions. The C-V electrical characteristic is shown in Fig. 3. The threshold-voltage shift after the 5 V programming operation is 1 V for the Ge nanocrystals embedded in SiON memory device with a-Si layer oxidized at 900 °C. The large threshold-voltage shift of memory device with an oxidized a-Si film as blocking oxide layer is attributed to the presence of Ge nanocrystals in the SiON film. The memory windows under 5 V operation for the three types of MOIOS structure are listed in Table I. It is clear that the memory window of Ge nanocrystals embedded in SiON memory structure is the largest than both above. Even the memory window value is larger than the sum of those of SiON and Ge nanocrystal MOIOS structures. The Ge nanocrystal embedded in SiON layer exhibits the superior memory characteristics. It is considered that the extra interface trap states between Ge and SiON film were generated as Ge nanocrystals were embedded in SiON layer. The initial SiON trap state density plus the trap state density of Ge nanocrystal surrounding the dielectric cause more larger memory effect. The proposed diagram is inserted in the Fig. 3. The proposed Ge nanocrystals embedded in SiON stack layer with high-temperature oxidized a-Si layer, therefore, contribute both larger memory window and the additional blocking oxide deposition for the nonvolatile memory application promisingly.

TABLE I. Memory windows for three types of nonvolatile memory devices.

Nonvolatile memory	ΔV_{th} under 5 V operation
SiON	0.2
Ge nanocrystal embedded in SiO_2	0.4
Ge nanocrystal embedded in SiON	1

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In conclusion, an easy nanocrystal memory technology has been demonstrated by oxidizing SiGeN film to form Ge distributed storage elements embedded in SiON layer. The memory window is obviously larger than the MOIOS structures with SiON layer alone or with Ge nanocrystals embedded in SiO_2 layer and even larger than the sum of both. The exhibition of memory windows after programming is resulted from the formation of Ge nanocrystals embedded in SiON layer and extra interface trap states between Ge and SiON film. Therefore, the material of SiGeN served as self-assembling layer and has more potential for the application in the nanocrystal nonvolatile memory technology.

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