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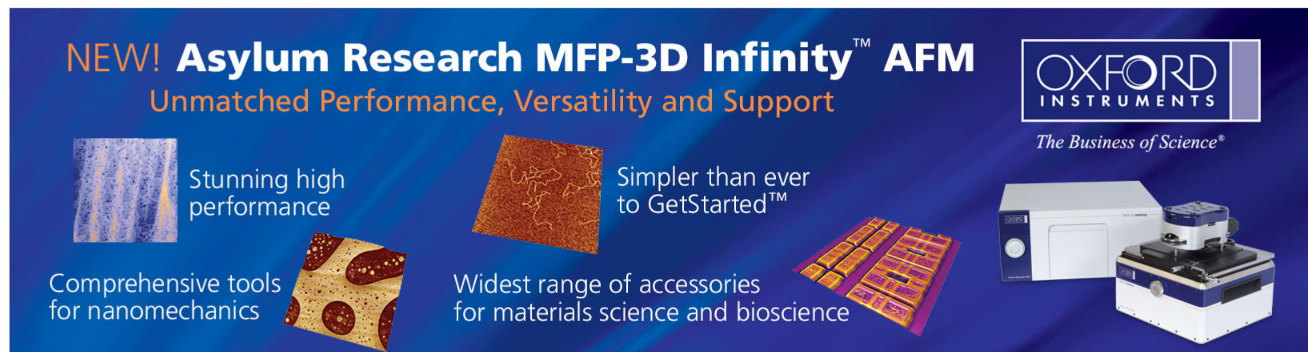

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Spatial and energetic distribution of border traps in the dual-layer HfO_2/SiO_2 high-*k* gate stack by low-frequency capacitance-voltage measurement

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Threshold voltage instability measured by the pulse current-voltage technique has been recognized as the transient charging and discharging of the preexisting bulk traps in Hf-based high-*k* gate dielectrics, and these high-*k* traps or called border traps can instantly exchange charge carriers with the underlying Si substrate by tunneling through the thin interfacial oxide. Based on an elastic tunneling model through trapezoidal potential barriers, the spatial and energetic distribution of border traps in the HfO_2/SiO_2 high-*k* gate stack can be profiled as a smoothed, three-dimensional mesh by measuring the low-frequency capacitance-voltage characteristics of high-*k* metal-oxide-semiconductor capacitors with *n*-type Si substrate. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2364064]

As the continuous scaling of gate dielectric thickness is leading to the intolerable tunneling gate leakage and power consumption, Hf-based high-*k* dielectric has been recognized as the most promising candidate for future advanced gate stacks in sub-45-nm node technologies. However, mobility degradation and other reliability issues such as transient V_t instability are still the major problems needed to be overcome. These problems can be addressed as the transient charging and discharging of the preexisting traps in Hf-based high-*k* dielectrics by using the pulse I_d-V_g technique,[1,2] which may originate from the direct tunneling between the injected charge carriers and preexisting high-*k* traps. The tunneling model through the thin interfacial oxide is similar to the one of tunneling into near-interface oxide traps that has already been studied and proposed.[3–5] These near-interface oxide traps are defined as the oxide traps located near the interface that can exchange charge carriers with the underlying Si substrate through direct tunneling and are suggested to be named as "border traps" to be distinguished from the conventional interface states and oxide traps.[6,7] In this work, an elastic tunneling model through trapezoidal potential barriers has been proposed to profile the spatial and energetic distribution of border traps in the HfO_2/SiO_2 high-*k* gate stack by low-frequency capacitance-voltage measurements.

Figure 1 shows the capacitance-voltage characteristics of the $TiN/HfO_2(3.2\ nm)/SiO_2(0.8\ nm)/n$-Si metal-oxide-semiconductor (MOS) capacitor with gate area $=10\,000\ \mu m^2$ measured and corrected at various frequencies, and the details of device fabrication process could be found elsewhere.[8] The capacitance increase in accumulation region could be observed at low-frequency *C-V* curves, and the low-frequency dielectric capacitance increases with the decrease of measurement frequency and the increase of gate bias voltage. To eliminate the influences of parasitic components such as the substrate/well resistance R_s and external inductance L_s on the measured dielectric capacitance C_p, two-frequency *C-V* correction method using a five-element circuit model[9] has been used to correct the faulty *C-V* curves at high frequencies (⩾500 kHz). Also, it has been demonstrated that the influences of these parasitic components on the measured dielectric capacitance could be ignored at frequencies lower than 500 kHz by formulating C_p as a function of the frequency, ideal dielectric capacitance C_0, and other parasitic components $(C_p \sim C_0(1-\omega^2 C_0 L_s)/[(1-\omega^2 C_0 L_s)^2+(\omega C_0 R_s)^2])$. In addition, the dielectric capacitance increase at low-frequency *C-V* curves could not be observed in conventional SiO_2 or SiON gate dielectrics with tunneling leakage current density much higher than that of

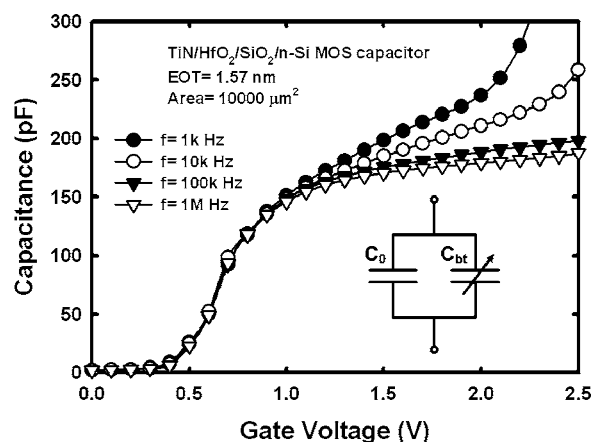

FIG. 1. Capacitance-voltage curves of the $TiN/HfO_2/SiO_2/n$-Si MOS capacitor at various frequencies. The capacitance increase at lower frequencies could be explained by proposing a frequency- and voltage-dependent border trap capacitance C_{bt} in parallel with the ideal dielectric capacitance C_0 as shown in the inset.

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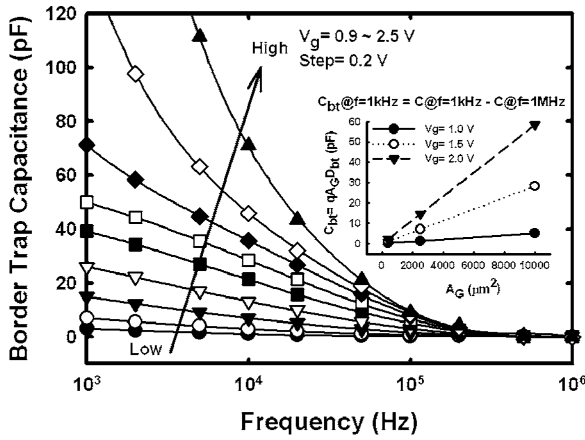

FIG. 2. Border trap capacitance C_{bt} as a function of measurement frequency at various gate bias voltages. The inset shows that the C_{bt} is linearly proportional to the gate area as proposed.

the above high-k gate stack (J_g at $V_g=+2.5$ V is merely 8.31×10^{-2} A/cm^2). Note that this low-frequency capacitance increase of Hf-based high-k gate dielectrics could only be observed in high-k MOS capacitors with n-type Si substrate biased in the accumulation region or in high-k n-channel metal-oxide-semiconductor field-effect transistors biased in the inversion region. In other words, the charge carriers tunneling through the thin interfacial oxide must be electrons due to their smaller effective mass and energy barrier height as compared to holes.

The dielectric capacitance increase at low frequencies could be explained by proposing a frequency- and voltage-dependent border trap capacitance C_{bt} in parallel with the ideal dielectric capacitance C_0 as shown in the inset of Fig. 1. If the charging and discharging of border traps in the HfO_2 high-k dielectric can immediately follow the small-signal frequency, these border traps would contribute an additional dielectric capacitance C_{bt}. Moreover, C_0 can be obtained by measuring at high frequencies ($\geqslant$500 kHz) with the appropriate correction of parasitic components, since C_{bt} is negligible at such high frequencies. Figure 2 shows the extracted border trap capacitance C_{bt} as a function of measurement frequency under various gate bias voltages, and these frequency and voltage dependences of C_{bt} can be transformed into the relations of tunneling distance from the Si substrate and trap energy depth from HfO_2 conduction band edge, respectively. These findings are similar to those of near-interface oxide traps observed by low-frequency charge pumping method or the transient capacitance signal by tunneling deep-level transient spectroscopy.[10–12]

Figure 3 shows the schematic band diagram of the $TiN/HfO_2/SiO_2/n$-Si MOS capacitor biased in accumulation region with the illustrations of tunneling distance and carrier energy coordinates. Similar to the interface state capacitance C_{it}, the border trap capacitance C_{bt} may result from an equivalent surface density of border traps D_{bt} (cm^{-2} eV^{-1}), which is the integration of the border trap volume density from the base oxide thickness x_1 to the maximum tunneling distance $x_{\max}$ in the HfO_2 high-k dielectric if there is negligible border traps in the thermally grown interfacial oxide:

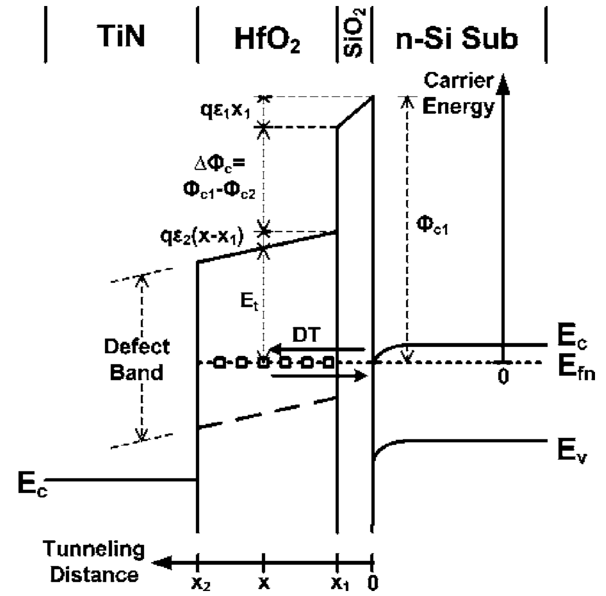

FIG. 3. Schematic band diagram of the $TiN/HfO_2/SiO_2/n$-Si MOS capacitor biased in the accumulation region with the illustrations of tunneling distance and carrier energy coordinates.

$$C_{\mathrm{bt}} = qA_G\int_{x_1}^{x_{\max}} N_{\mathrm{bt}}(x,E_t)dx, \tag{1}$$

where q is the electron charge, A_G is the gate area, and N_{bt} is the border trap volume density (cm^{-3} eV^{-1}) as a function of the tunneling distance x and trap energy depth E_t. In addition, the inset of Fig. 2 shows that C_{bt} is linearly proportional to the gate area as proposed. Assume that the charging and discharging of border traps mainly occur at the Si conduction band edge through direct tunneling and that these border traps are widely distributed over a defect band, not at a single energy level, in the HfO_2 high-k dielectric.[1] Then the trap energy depth E_t from the HfO_2 conduction band edge could be approximately obtained under various gate bias voltages if the two-band structure (SiO_2 and HfO_2) with trapezoidal potential barriers has been considered:

$$E_t(x,\varepsilon) = \phi_{c2} - q\varepsilon_1 x_1 - q\varepsilon_2(x-x_1), \tag{2}$$

where Φ_{c2} (1.9 eV) is the conduction band offset of HfO_2,[13] ε_1 and ε_2 are the electric fields in the SiO_2 and HfO_2 dielectrics, and x_1 is the base oxide thickness (0.8 nm). Assume that the above tunneling transition is an elastic tunneling process with symmetric forward and reverse tunneling probabilities, then the tunneling time constants between the available Si conduction band states and localized border traps should be equal to or less than a quarter of measurement period $1/f$:

$$\frac{1}{4f} = \tau_0 \exp\left(2\int_0^{x_1}\frac{\sqrt{2m_1^*(\phi_{c1}-q\varepsilon_1 x')}}{\hbar}dx' + 2\int_{x_1}^{x}\frac{\sqrt{2m_2^* E_t(x',\varepsilon)}}{\hbar}dx'\right), \tag{3}$$

where f is the measurement frequency, τ_0 is the preexponential factor ($\sim10^{-10}$ s) which is relatively insensitive to the tunneling distance and trap energy depth,[14] $\hbar$ is the reduced Planck constant, Φ_{c1} (3.1 eV) is the conduction band offset of SiO_2, and m_1^* ($0.42m_0$) and m_2^* ($0.18m_0$) are the effective

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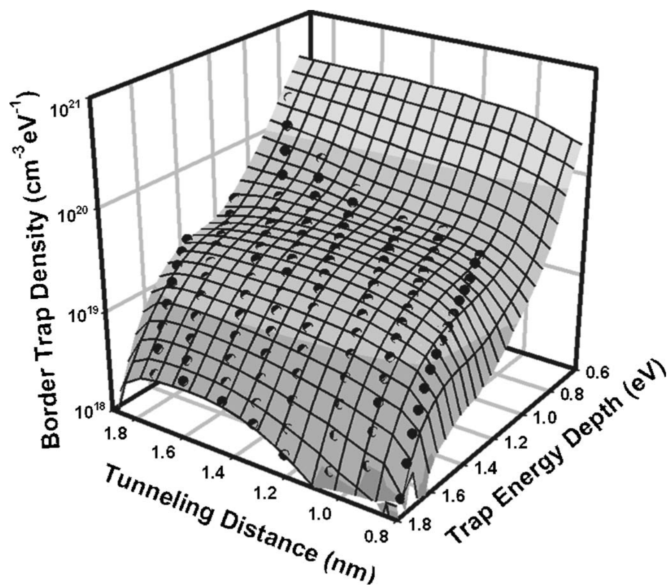

FIG. 4. Spatial and energetic distribution of the border trap volume density in the dual-layer HfO_2/SiO_2 high-k gate stack. Symbols are model-extracted data points, and 3D mesh is the smoothed surface profiling of these points.

masses of electrons in SiO_2 and HfO_2 dielectrics.[4,13] Subsequently, the maximum tunneling distance x_{max} that can be reached during the measurement cycle could be extracted from Eq. (3) with the given parameters above. Finally, the spatial and energetic distribution of the border trap volume density could also be obtained as follows:

$$N_{bt}(x,E_t) = \frac{-2\sqrt{2m_2^* E_t(x,\varepsilon)}}{qA_G\hbar}\frac{dC_{bt}}{d\ln(f)}. \quad (4)$$

Figure 4 shows the spatial and energetic distribution of the border trap volume density N_{bt} ($\sim 10^{18}-10^{20}$ cm^{-3} eV^{-1}) in the dual-layer HfO_2/SiO_2 high-k gate stack. Symbols are model-extracted data points, and three-dimensional (3D) mesh is the smoothed surface profiling of these points. As the tunneling distance reaches the HfO_2 high-k dielectrics ($x > 0.8$ nm), N_{bt} begins to increase gradually and eventually becomes saturated. Furthermore, N_{bt} increases exponentially with the decrease of trap energy depth E_t, and it appears to be insensitive to the tunneling distance. These results suggest that most of the preexisting high-k traps are located in the HfO_2 bulk layer and that considerable parts of these traps are positioned at the shallow energy levels.

Dielectric capacitance increase of the dual-layer HfO_2/SiO_2 high-k gate stack has been observed by the low-frequency C-V measurements. This phenomenon could be well explained by proposing a frequency- and voltage-dependent border tarp capacitance in parallel with the ideal dielectric capacitance as long as the transient charging and discharging of these border tarps could immediately follow the measurement frequency. In addition, these frequency and voltage dependences of the border trap capacitance could be transformed into the relations of the tunneling distance and trap energy depth by using an elastic tunneling model between the Si conduction band states and localized border traps through trapezoidal potential barriers. Based on this physical model, the spatial and energetic distribution of the border trap volume density in the HfO_2 high-k dielectric could be profiled as a smoothed 3D mesh. This technique can be easily integrated into the routine measurement and analysis procedure to monitor the quality of Hf-based high-k dielectrics, since only the MOS capacitors with n-type Si substrate are needed.

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