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Letter

Low-voltage organic thin-film transistors with polymeric nanocomposite dielectrics

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Abstract

High performance organic thin-film transistors (OTFTs) incorporated with high dielectric nanoparticles in the dielectric layers have been demonstrated. The dielectric insulator consists of cross-linked poly-4-vinylphenol (PVP) and titanium dioxide (TiO_2) nanoparticles. In order to obtain highly soluble TiO_2 nanoparticles in organic solutions, the surface of nanoparticles was modified with organosiloxane. Moreover, the concern of higher leakage current, while using the high dielectric nanocomposite insulators, has been overcome by further applying another poly(α-methylstrylene) layer. As a result, we have demonstrated low-voltage OTFTs, which can be operated within 10 V.
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Organic thin-film transistors (OTFTs) have been recognized as promising technology for next generation electronics due to their unique advantages, such as light-weight, flexibility, and low-cost fabrication [1–3]. Potential applications include flexible displays [4,5], radiofrequency identification (RFID) tags [6], "smart" cards, and other consumer electronics [7,8]. However, the major challenge to realize the commercialization of related products comes from their high threshold and operating voltages, due to the intrinsic low charge motilities of organic semiconductors. Because the field-induced current is proportional to the field-induced charge density, one feasible approach to achieve low-voltage operation in OTFTs is to use high dielectric constant (high-κ) materials as the gate insulators, which can afford greater surface charge density at the semiconductor-dielectric interface. Several works, especially those adopting inorganic high-κ materials, have demonstrated successfully the reduction of the OTFTs operating voltages using this concept [9,10]. However, these inorganic materials are usually expensive to fabricate and not compatible with

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plastic substrates due to the high-annealing-temperature processes and their fragility.

Using a solution-processable method high-κ polymers can be easily fabricated and used as dielectrics for OTFTs without the complications associated with sputtering high-κ materials and the high-temperature annealing [11]. Nanocomposite materials, consisting of titanium dioxide (TiO$_2$) nanoparticles and cross-linked poly-4-vinylphenol (PVP), were dispersed well in organic solvents. Upon spin-coating and thermal annealing, a composite insulator film was obtained. Due to the limited solubility of TiO$_2$ nanoparticles, the dielectric constant only increased from 3.5 to 5.4 after blending high-κ nanoparticles into the polymer matrix. In this work, surface modified TiO$_2$ nanoparticles with organosiloxane was used in order to increase the solubility in organic solvents. With the higher content of TiO$_2$ incorporated, a dielectric constant higher than 11 is achieved. More importantly, we will show that the current leakage problem through the gate dielectrics can be overcome by further applying another thin organic polymer insulator. As a result, we have also demonstrated low-voltage OTFTs, which can operate within 10 V.

Titanium dioxide exists naturally as three possible crystal types, namely, rutile, anatase and brookite [12]. In this study, we employed TiO$_2$ with rutile structure due to its higher dielectric constant ($\kappa = 114$) than that of other structures. In addition, rutile TiO$_2$ has much lower photocatalytic activity; possible photoreactions can be avoided. Nanocomposite dielectric layers, consisting of TiO$_2$ nanoparticles, whose surface was further modified with organosiloxane (Ishihara Sangyo Kaisha LTD., Japan), and cross-linked PVP were prepared for OTFT gate insulators. PVP (11 wt%) and poly (melamine-co-formaldehyde) methylated (4 wt%), as a cross-linking agent, were dissolved in propylene glycol monomethyl ether acetate (PGMEA), [13] and

blended with different concentrations of TiO$_2$ nanoparticles. The composite solution was then spin-coated onto indium–tin-oxide (ITO) patterned glass substrates which were used as gate electrodes. The thickness of these insulators is $\sim$700 nm. Pentacene was thermally evaporated as the semiconductor layer. Finally, gold metal was thermally evaporated through the shadow mask and used as the source and drain electrodes (top-contact). The channel length (L) and width (W) are 160 and 2000 μm, respectively. The film thickness and roughness were measured by DI 3100 series atomic force microscopy (AFM). The current–voltage (I–V) characteristics of OTFTs were measured by a HP 4156 A semiconductor parameter analyzer. The devices with metal–insulator–metal (MIM) structure, consisting of different dielectric materials sandwiched between ITO and Al electrodes, were used for capacitance measurements. The capacitance measurements were conducted with a HP 4284 A Precision LCR meter.

For a pure cross-linked PVP film, the dielectric constant is 4.3 at 1 kHz, which is close to the value reported earlier [11,14]. From Table 1, we can see that the dielectric constant increases with the amount of the TiO$_2$ nanoparticle embedded in the thin films. For the dielectric film with 15 wt% of TiO$_2$ nanoparticle, the dielectric constant increased to 10.8, due to the higher solubility of the organosiloxane surface modified TiO$_2$ fillers, compared to that reported earlier [11].

The drain–source current (I_D) vs. drain–source voltage (V_D) of OTFTs with different TiO$_2$ concentrations incorporated in the gate insulators is shown in Fig. 1. The carrier mobility was calculated in the saturation regime using the following equation:

$$I_{DS} = (WC_i/2L)\mu(V_G - V_T)^2 \qquad (1)$$

where C_i is the capacitance per unit area of the insulator, and V_T is the threshold voltage. For the de-

Table 1
Electrical parameters of the OTFTs in this study

TiO$_2$ wt%	Dielectric constant	Mobility μ_{sat} (cm^2/Vs)	Threshold voltage V_{th} (V)	Surface roughness[a] (nm)	On/Off ratio
0	4.3	0.42	−5.2	0.30	5×10^4
1	4.8	0.39	−14.4	9.76	4×10^4
5	6.7	0.42	−10.9	16.19	9×10^3
10	8.5	0.34	−3.3	26.99	6×10^3
15	10.8	0.32	+5.9	31.43	1×10^3
15%/PαMS[b]	11.6	0.41	−3.0	13.30	3×10^4

[a] Surface roughness of the dielectric layers.
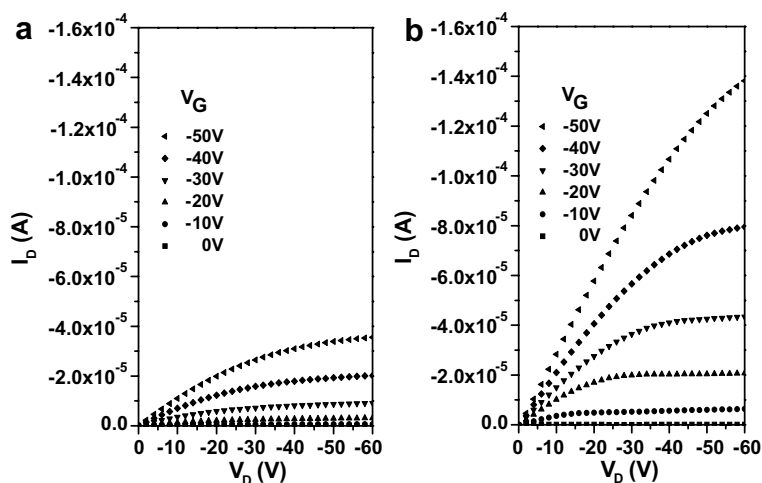[b] PαMS: poly(α-methylstyrene).

Fig. 1. The output characteristics (drain current, I_D vs. drain voltage, V_D,) of OTFTs with (a) a neat PVP insulator; (b) a composite insulator with 15 wt% TiO$_2$ nanocomposite insulators.

vice with a neat PVP gate insulator, (Fig. 1a) the mobility in the saturation region and the threshold voltage of the OTFT are 0.42 cm^2 V^{-1} s^{-1} and −5.2 V, respectively. The on–off ratio is more than 10^4. With 15 wt% of TiO$_2$ nanoparticles blended into the dielectric layer, (Fig. 1b) the device exhibits more than triplet the field-induced current compared with that of the device using the pure PVP insulator which is attributed to the higher surface capacitance. Fig. 1 reveals that the drain–source current increased by increasing the content of TiO$_2$ nanoparticles in the gate insulators. The parameters of the dielectric materials as well as the corresponding electrical characteristics of the OTFTs with different amount of TiO$_2$ nanoparticles embedded in the gate insulators are summarized in Table 1.

On the other hand, we also observe that the threshold voltage (V_{th}) decreases and then increases when more nanoparticles were added (Table 1). From the surface morphology study by AFM, the insulator roughness increased with the increasing concentration of TiO$_2$ blended. Consequently, the shift of V_{th} to higher values may be the result of the insulators surface roughness. The interface between the organic semiconductor and the insulator is affected by the incorporation of TiO$_2$ nanoparticles.

Additionally, we can also find that the on–off ratio decreases while the concentration of TiO$_2$ increases (Table 1). Fig. 2 shows clearly that the device with 15 wt% TiO$_2$ has much higher leakage

current than that with 1 wt% nanoparticles. The leakage problem is probably due to the low-band gap of TiO$_2$. In addition, structure defects induced by the present of high concentration TiO$_2$ might also result in the higher leakage current, which has been confirmed from the fact that the surface roughness of the insulators increased with the content of nanoparticles (Table 1).
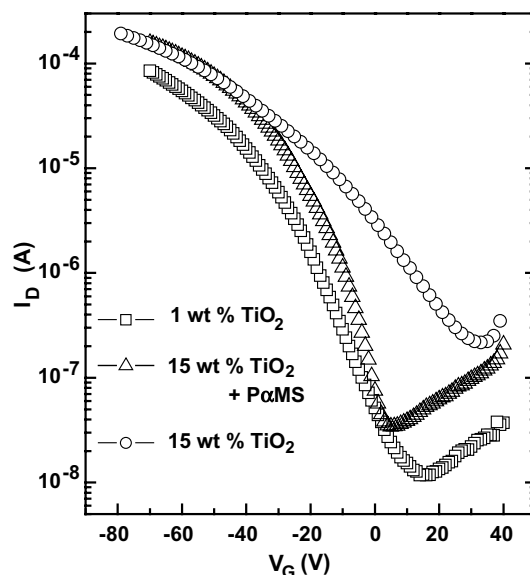

Fig. 2. The transfer characteristic (drain current, I_D vs. gate voltage, V_G) at constant $V_D = -40$ V for OTFTs with 1 wt%, 15 wt% of TiO$_2$ nanocomposite insulators, and nanocomposite insulators with the PαMS interfacial layer.

In order to rectify this problem, the insulator layer was covered with a poly(α-methylstrylene) (PαMS) layer. Due to the robustness of cross-linked polymers, the underlayer was not affected by this process. As shown in Fig. 2, the device off current is dramatically suppressed after spin-coating ∼30 nm PαMS on the nanoparticle/cross-linked PVP insulator. The over-coating of another interfacial layer can reduce the concentration of surface defects of the dielectrics and smooth the dielectric surface. In addition the dielectric constant of the insulator modified with PαMS is higher than that without modification. This further supports the fact that PαMS can inhibit the leakage current and enhance the dielectric strength of the composite polymer.

On the other hand, the smooth dielectric surface might also induce the formation of a more orderly crystalline pentacene film, and subsequently, increase the device mobility as shown in Table 1. Table 1 apparently shows that the surface roughness of the dielectric layer affects the device mobility in the saturation regime. While the concentration of TiO_2 is more than 5 wt%, the mobility drops dramatically. The rough dielectric surface probably interferes with the formation of an ordered crystal structure. Fig. 3 shows the surface morphology of pentacene deposited on different dielectrics. In contrast to the clear crystal formation on the neat cross-linked PVP, the grain size of pentacene on the 15 wt% TiO_2 filled-PVP film is rather small. The higher concentration of grain boundary might limit the charge transport in the organic films. However, after over-coating the PαMS layer, typical lamella morphology appears again, which implies the formation of an ordered crystal structure. In summary,

the PαMS layer not only suppresses the leakage current by reducing the concentration of defects in the dielectric layer, but also induces pentacene to form a more ordered molecular conformation thus maintaining the high mobility in the conducting channel.

Since the leakage problem has been overcome by incorporating an interfacial layer, thinner dielectric layers will be allowed to achieve a greater capacitance value. Fig. 4 shows the output characteristics for an OTFT with a 270 nm nanocomposite insulator, consisting of one layer of 15 wt% TiO_2 filled-PVP film and another thin PαMS. The dielectric constant of this composite is 10.5, which is slightly lower than that of previous one. The device exhibits mobility of ∼0.4 $cm^2 V^{-1} s^{-1}$. The sub-threshold slope is 1.0 V/decade and the threshold voltage is −2.9 V. The on–off ratio is more than 3.0×10^4.
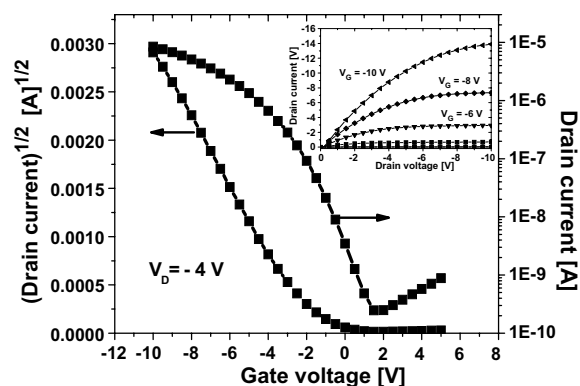

Fig. 4. The transfer characteristics of the OTFT with a thinner gate insulator. The inset shows the corresponding output characteristic from $V_G = 0$ V to −10 V.
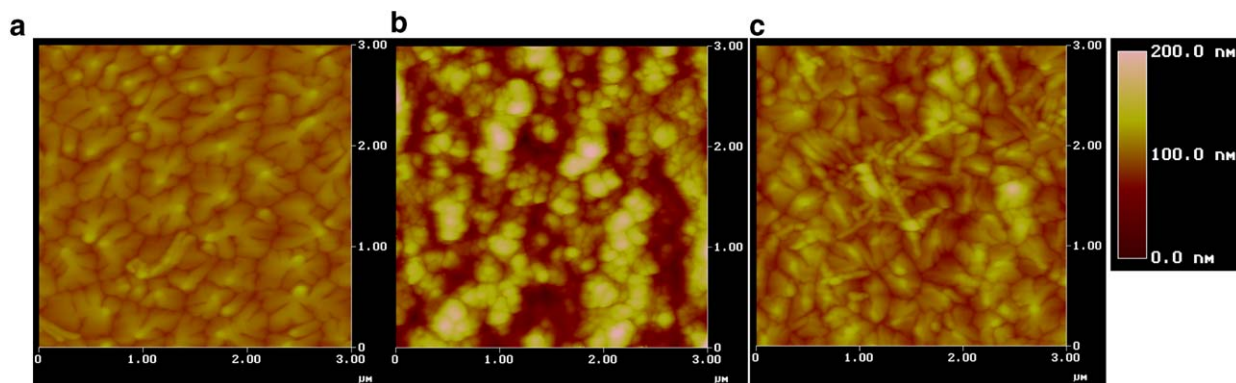

Fig. 3. AFM height-mode images of pentacene deposited on the surface of (a) neat cross-linked PVP; (b) cross-linked PVP blended with 15 wt% TiO_2 nanoparticles; (c) cross-linked PVP blended with 15 wt% TiO_2 nanoparticles and further modification with PαMS interfacial layer.

From Fig. 4, it is apparent that low-voltage OTFTs can be fabricated by using nanocomposite dielectric polymers with simple and solution-processable processes.

In conclusion, high performance organic thin-film transistors incorporated with high dielectric nanoparticles in the dielectric layers have been demonstrated successfully. Moreover, the problem of leakage current of OTFTs, while using the nanocomposite insulators, has been overcome using over-coat of another thin interfacial layer. This method offers a feasible and economic way to deposit gate insulators for OTFTs with high capacitance without the complications associated with sputtering of high dielectric materials and high-temperature annealing. Finally, one low-voltage OTFT, which can operate within 10 V, has also been achieved by this method.

Acknowledgements

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