Design on Power-Rail ESD Clamp Circuit for 3.3-V I/O Interface by Using Only 1-V/2.5-V Low-Voltage Devices in a 130-nm CMOS Process

Ming-Dou Ker, *Senior Member, IEEE*, Wen-Yi Chen, and Kuo-Chun Hsu, *Member, IEEE*

***Abstract*—A new power-rail electrostatic discharge (ESD) clamp circuit for application in 3.3-V mixed-voltage input–output (I/O) interface is proposed and verified in a 130-nm 1-V/2.5-V CMOS process. The devices in this power-rail ESD clamp circuit are all 1-V or 2.5-V low-voltage nMOS/pMOS devices, which are specially designed without suffering the gate-oxide reliability issue under 3.3-V I/O interface applications. A special ESD detection circuit realized with the low-voltage devices is designed and added in the power-rail ESD clamp circuit to improve ESD robustness of ESD clamp devices by substrate-triggered technique. The experimental results verified in a 130-nm CMOS process have proven the excellent effectiveness of this new proposed power-rail ESD clamp circuit.**

***Index Terms*—Electrostatic discharge (ESD), ESD protection circuit, high-voltage tolerant, power-rail ESD clamp circuit, substrate-triggered technique.**

I. Introduction

ELECTROSTATIC (ESD) has been an important reliability issue for modern integrated circuit (IC) products in the scaled-down CMOS technologies. Since the stored electrostatic charges could be either positive or negative, there are four different ESD-testing modes at input–output (I/O) pins with respect to the grounded V_{DD} or V_{SS} pins [1], [2]. Besides the four ESD-testing modes at I/O pins, two additional ESD-testing modes, the pin-to-pin and the V_{DD}-to-V_{SS} ESD stresses, had been also specified to verify the whole-chip ESD robustness [1], [2]. These two additional ESD-testing modes often lead to some unexpected ESD current through the I/O ESD protection circuits and the power lines into the internal circuits and result in ESD damage on the internal circuits [3], [4]. As a result, an effective power-rail ESD clamp circuit between the V_{DD} and V_{SS} power lines is necessary for the whole-chip ESD protection [4].

When CMOS technologies are scaled down toward nanometer generation, the power supply voltage is also decreased as well to reduce the power consumption. However, some peripheral components or other ICs on the system board are still operated with the higher voltage levels such as 3.3 V to meet the system specification. Therefore, the mixed-voltage I/O design is needed for the interface of semiconductor chips or sub-systems with different power-supply voltages [5]–[7]. In such mixed-voltage I/O interfaces, the ESD protection circuits are requested to be designed with only low-voltage devices of a given technology without suffering the gate-oxide reliability issue [8], [9]. To achieve a good whole-chip ESD protection scheme for the mixed-voltage I/O applications, it is required to design the power-rail ESD clamp circuit with only low-voltage devices that can sustain the high power-supply voltage without suffering the gate-oxide reliability issue [10]. Besides the gate-oxide reliability issue, the standby leakage current of the power-rail ESD clamp circuit during normal circuit operating conditions is another concern [11], [12], especially for the portable electronic products. Thus, how to design a turn-on-efficient power-rail ESD clamp circuit with only low-voltage devices to sustain the high-voltage input signals or the high power-supply voltages becomes a quite significant challenge to the nano-scale mixed-voltage CMOS ICs.

In this work, a novel power-rail ESD clamp circuit implemented with only 1-V/2.5-V nMOS/pMOS devices is proposed for application in the 3.3-V I/O interfaces without suffering the gate-oxide reliability issue [13]. This new power-rail ESD clamp circuit has an efficient ESD detection circuit to trigger on the ESD clamp device, so that the turn-on efficiency of the power-rail ESD clamp device can be substantially increased. The proposed power-rail ESD clamp circuit has been successfully verified in a 130-nm 1-V/2.5-V CMOS process with excellent ESD protection capability and extremely low standby leakage current.

II. ESD Protection Scheme for 1-V/3.3-V Mixed-Voltage I/O Interface

A. ESD Protection Scheme

For the mixed-voltage I/O applications, there are separated power lines with different power supply voltages. So, the internal circuits of mixed-voltage ICs are more easily damaged under the pin-to-pin ESD stress [14]. As a result of different power supply voltages, some ESD protection techniques for ICs with separated power lines, such as the bi-directional back-to-back diodes [15], are not applicable. Therefore, the dummy supply ESD bus has been proposed [16], which is an effective method to quickly discharge the ESD current away

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M.-D. Ker is with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan 300, R.O.C. (e-mail: mdker@ieee.org).

W.-Y. Chen was with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan 300, R.O.C. He is now with the Chinese Army.

K.-C. Hsu was with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan 300, R.O.C. He is now with Global UniChip Corporation, Science-Based Industrial Park, Hsinchu, Taiwan 300, R.O.C.

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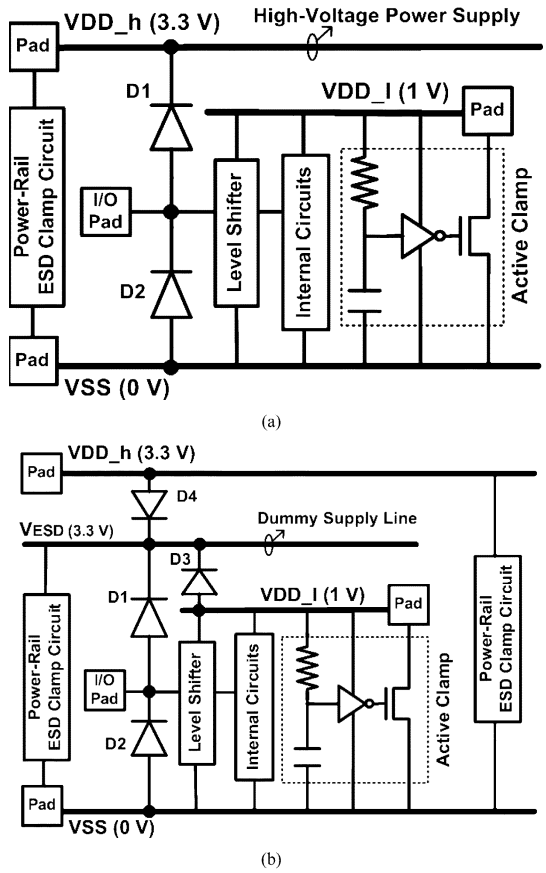

Fig. 1. ESD protection schemes for mixed-voltage I/O interfaces (a) without, and (b) with, the dummy supply line V_{ESD}.

from the internal circuits, especially under the pin-to-pin ESD stress.

Two modified successful whole-chip ESD protection schemes for 1-V/3.3-V mixed-voltage I/O interfaces are shown in Fig. 1(a) and (b) [16]–[19]. In Fig. 1(a), diodes D1 and D2 and the power-rail ESD clamp circuit are designed to achieve ESD protection in the I/O pad with 3.3-V input signals. The ESD current at I/O pads under positive-to-V_{SS} (PS mode) ESD stress is discharged through the diode D1 and the power-rail ESD clamp circuit between V_{DD}_h and V_{SS} power lines. In Fig. 1(a), the extra bond pad for external 3.3-V power supply (marked as V_{DD}_h) is optional, depending on the system specification and the circuit requirement. For circuits without external 3.3-V power supply pins, the V_{DD}_h line shown in Fig. 1(a) can be treated as a dummy supply line and the extra bond pad is dispensable.

For chips with power-down mode operation, which is an important power-saving technology in nowadays systems-on-chip (SOC) or portable devices [20], an extra dummy supply line (marked as V_{ESD}) is added into the chip for cooperation with the power-rail ESD clamp circuit to achieve ESD protection in the I/O pad with 3.3-V input signals, as shown in Fig. 1(b). The diode D4 between the V_{DD}_h power line and the V_{ESD} dummy supply line can prevent the circuit, which has entered the power-down mode, being awakened by the input signal at I/O pads. In this ESD protection scheme, the ESD current at I/O pads under positive-to-V_{SS} (PS mode) ESD stress is discharged through the diode D1 and the power-rail ESD clamp circuit between V_{ESD} and V_{SS} power lines. For positive-to-V_{DD} (PD mode) ESD stress on I/O pads, the ESD current can be discharged through the diode D1, the power-rail ESD clamp circuit between V_{ESD} and V_{SS} power lines, and then the parasitic diode of the power-rail ESD clamp circuit between the V_{DD}_h and the V_{SS} power lines (the active clamp between V_{DD}_l and V_{SS}) to the grounded V_{DD}_h (V_{DD}_l). For V_{DD}_h-to-V_{DD}_l ESD stress, the ESD current is discharged through the diode D4, the power-rail ESD clamp circuit between the V_{ESD} and the V_{SS} power lines, and then the parasitic diode of the active clamp between V_{DD}_l and V_{SS} power lines.

In these successful designs, the power-rail ESD clamp circuits must sustain the high-voltage (3.3-V) stress in the mixed-voltage I/O interfaces during normal circuit operating conditions without the gate-oxide reliability issue. About the active clamp for the internal circuits shown in Fig. 1(a) and (b), it can be realized by the traditional *RC*-based ESD detection circuits with 1-V devices [4].

B. Review on High-Voltage-Tolerant Power-Rail ESD Clamp Circuit

With the increasing demand for the mixed-voltage I/O interface circuits, several prior arts about the high-voltage-tolerant power-rail ESD clamp circuits had been reported, such as the diode string, the stacked-pMOS clamp with voltage divider, and the stacked-nMOS configuration [8]–[10], [21]–[24]. Because the forward-biased p-n junction diode can sustain quite high ESD current without the gate oxide reliability issue, the diode string with multiple stacked diodes had been developed to protect the mixed-voltage I/O [24], or as the power-rail ESD clamp circuit [21]–[23]. However, the main disadvantage of using the forward-biased stacked diodes as the power-rail ESD clamp circuit is the huge standby leakage current which results from the parasitic p-n-p bipolar junction transistor (BJT). The Darlington beta gain makes the leakage current of the parasitic BJTs increase dramatically at high operating temperature [25]. To reduce the leakage current of the diode string, especially for ICs operating under the high temperature condition, some modified designs, such as the Cladded diode string, Boosted diode string, and Cantilever diode string, were reported in [22]. An improved design by using silicon-controlled-rectified (SCR) device to stop the leakage current through the diode string was also reported to achieve an ultra low leakage level in the high temperature condition [25].

Since the gate-oxide reliability issue results from the over-induced electric field across the gate–drain, gate–source, and gate–bulk terminals of MOSFET devices, the voltage divider that divides the high power-supply voltage (V_{cc}) to be $1/3\,V_{\mathrm{cc}}$ or $2/3\,V_{\mathrm{cc}}$ is incorporated to some of the ESD protection circuits to reduce the voltage across the gate–drain, gate–source, and gate–bulk terminals [10]. The voltage divider is useful to avoid the gate-oxide reliability issue but the divider itself provides a standby current path from the power supply to ground, causing leakage current in the order of several micron-amps. In [10], the leakage current of the stacked-pMOS ESD protection circuit under 25 °C (125 °C) and 3.3-V power supply voltage is roughly

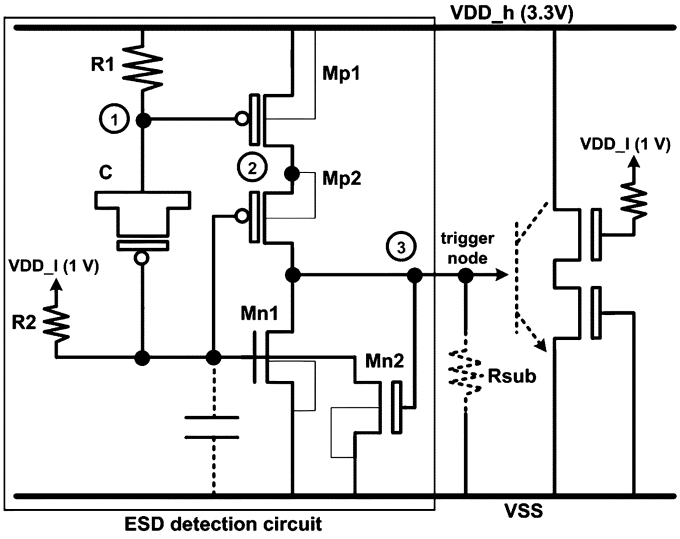

Fig. 2. New proposed power-rail ESD clamp circuit with only 1-V and 2.5-V devices for operating under high-voltage $V_{\rm DD}$_h of 3.3 V.

0.8 μA (8 μA), which could be still too large for most portable microelectronic products and low-power IC products.

Another well-known and widely used high-voltage-tolerant structure is the stacked-nMOS configuration [8], where the top gate of the stacked nMOS is biased at a relatively low voltage to drop the drain voltage of the bottom nMOS and to safely meet the reliability limitation during normal circuit operating conditions. Unfortunately, the stacked nMOS has been found to have some disadvantages of ESD protection capability, including the nonuniform turn-on behaviors, slower turn-on speed, and the lower ESD robustness. Therefore, to uniformly and quickly turn on the stacked nMOS in the mixed-voltage I/O buffers under ESD stress conditions, some ESD detection circuits are therefore developed to trigger the stacked nMOS [26], [27]. In this work, a novel low-leakage power-rail ESD clamp circuit, which contains a high-voltage tolerant ESD detection circuit to substantially increase the ESD protection efficiency of stacked nMOS, is proposed.

III. Novel Power-Rail ESD Clamp Circuit for High-Voltage Applications

The novel power-rail ESD clamp circuit which contains ESD clamp device and ESD detection circuit is shown in Fig. 2, where the ESD clamp device is realized by a substrate-triggered stacked nMOS (STnMOS). The new proposed power-rail ESD clamp circuit is realized with only 1-V and 2.5-V devices to operate at 3.3-V I/O interface without the risk of gate oxide reliability. Under normal circuit operating conditions, the ESD detection circuit is inactive and doesn't interfere with the functions of internal circuits. But, it is active to provide the substrate-triggered current to quickly trigger on the STnMOS device under ESD stress conditions. The STnMOS is formed by two stacked nMOS transistors with 2.5-V gate oxide in the 130-nm 1-V/2.5-V CMOS process. The gate of the top nMOS transistor of STnMOS is biased at $V_{\rm DD}$_l of 1 V through a resistor, and that of the bottom nMOS transistor is directly connected to $V_{\rm SS}$. The voltage level at the shared $N+$ diffusion region between the top and bottom nMOS transistors of STnMOS device will be kept at $V_{\rm DD}$-$V_{\rm th}$ during normal circuit operating conditions, where $V_{\rm th}$ is the threshold voltage of the 2.5-V nMOS transistor. Therefore, the STnMOS is free from the gate-oxide reliability issue under high power-supply voltage $V_{\rm DD}$_h of 3.3 V. The ESD detection circuit is formed by Mp1, Mp2, and *C* of 2.5-V pMOS devices, Mn1 of 1-V nMOS device, Mn2 of 2.5-V nMOS device, and an n-well resistor *R1*. The selected device dimensions of the proposed ESD detection circuit in this work is listed in Table I.

TABLE I
Device Dimensions of ESD Protection Circuit in This Work

	Device parameter (each finger)	Number of fingers
Mp1	30 μm/0.28 μm	4
Mp2	30 μm/0.28 μm	4
Mn1	20 μm/0.28 μm	1
Mn2	10 μm/0.28 μm	1
C	20 μm/3.5 μm	4
R1	50 kΩ	
R2	1 kΩ	

A. Circuit Operation Under Normal Power-On Transition

When the 3.3-V $V_{\rm DD}$_h and 1-V $V_{\rm DD}$_l have been powered on, the gate of Mp1 (node 1 in Fig. 2) is biased at 3.3 V through the resistor *R1*, and the gate of Mp2 is biased at 1 V through the resistor *R2* of 1 kΩ. With a gate-to-source bias of 0 V, the Mp1 should be kept off. With a gate-to-source bias of 1 V, the Mn1 is turned on. So, no trigger current will be generated from the ESD detection circuit into the trigger node (node 3 in Fig. 2) of the STnMOS. The turned-on Mn1 can guarantee the off-state of STnMOS during normal circuit operating conditions. Because the gate of Mp2 is biased at $V_{\rm DD}$_l through the resistor *R2*, the drain voltage of Mp1 (node 2 in Fig. 2) is kept at $(1\ {\rm V} + |V_{\rm tp}|)$, where $V_{\rm tp}$ is the threshold voltage of the 2.5-V pMOS transistor. By such arrangement, all low-voltage devices in the new proposed power-rail ESD clamp circuit are free from the gate-oxide reliability issue under normal circuit operating conditions with $V_{\rm DD}$_h of 3.3 V in the mixed-voltage I/O interfaces. Fig. 3(a) shows the Hspice-simulated voltages on nodes of the ESD detection circuit. In this simulation, the $V_{\rm DD}$_h and $V_{\rm DD}$_l are, respectively, powered-on to 3.3 V and 1 V with a simultaneous rise time of 1 ms. The Hspice-simulated results show that the voltages across the gate–drain, gate–source, and gate–bulk terminals of every device do not exceed the process limitation. Moreover, the gate voltage of pMOS Mp1 in the ESD detection circuit with the selected *R1-C* value can follow up the power-on transition of $V_{\rm DD}$_h to turn off the pMOS Mp1.

B. Circuit Operation Under ESD Transition

When ESD transient voltage is applied to $V_{\rm DD}$_h with $V_{\rm SS}$ relatively grounded, the gate of Mp1 (node 1 in Fig. 2) is initially kept at a low voltage level (around 0 V) due to the *RC* delay of *R1* and *C* in the ESD detection circuit. The $V_{\rm DD}$_l node is initially floating with an initial voltage level of 0 V, before the ESD

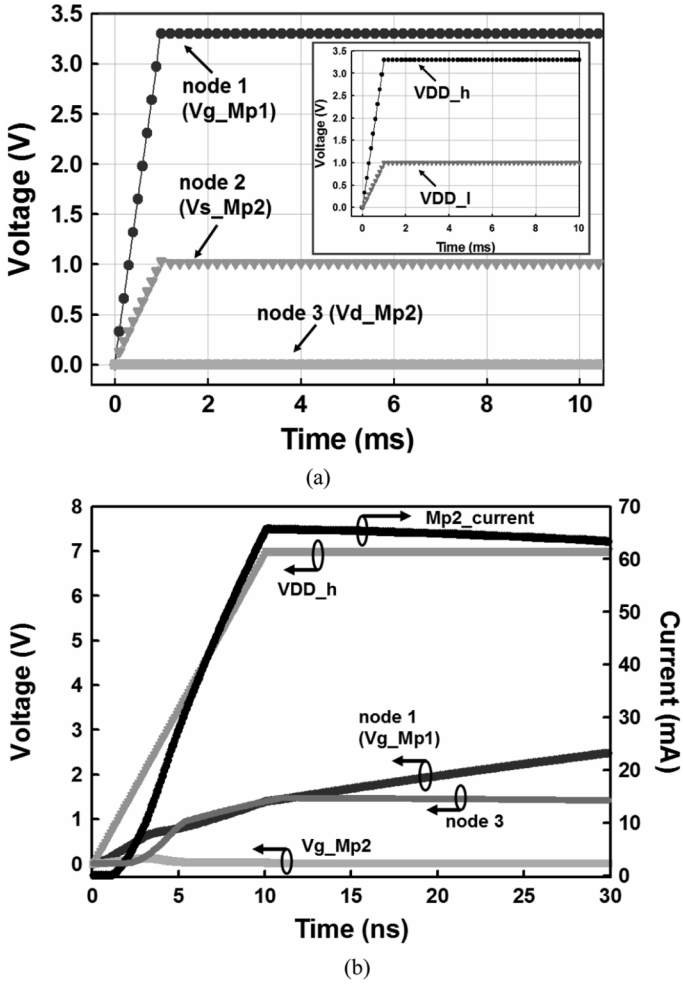

Fig. 3. Hspice simulation on the new proposed ESD detection circuit under (a) normal power-on transition with a rise time of 1 ms and (b) 0-to-7 V ESD-like transition with a rise time of 10 ns.

voltage is applied across $V_{\rm DD}$_h and $V_{\rm SS}$. Some ESD transient voltage would be coupled to $V_{\rm DD}$_l through the parasitic capacitance when ESD stress is zapped on $V_{\rm DD}$_h, but the R2 and the parasitic capacitance at the gates of Mn1 and Mp2 will keep the gate of Mp2 at 0 V for a long time period. So, Mp1 and Mp2 with initial gate voltages at $\sim$0 V can be quickly turned on by the ESD energy to generate the trigger current into the trigger node (node 3 in Fig. 2) of STnMOS. As long as the base-emitter voltage of the lateral n-p-n BJT inherent in the STnMOS device is greater than its cut-in voltage of $\sim$0.7 V, the STnMOS can be triggered on to discharge ESD current from $V_{\rm DD}$_h to grounded $V_{\rm SS}$. Fig. 3(b) shows the Hspice-simulated voltages and current of the ESD detection circuit under ESD transition. A 0-to-7 V ESD-like voltage pulse with rise time of 10 ns is applied to the $V_{\rm DD}$_h to simulate the ESD transition before junction breakdown on the devices. The Hspice-simulated results show that the gate voltage of Mp1 is kept low due to the time delay of *R1* and *C*. The pMOS Mp1 and Mp2 can provide the substrate-triggered current larger than 60 mA within 10 ns when the 0-to-7 V transient voltage is applied to $V_{\rm DD}$_h. Simulation on the voltage of node 3 in Fig. 3(b) also verifies that the substrate bias can be achieved by the substrate-triggered current generated from the proposed ESD detection circuit. By selecting the device dimensions, the substrate-triggered current can be designed to meet different applications or specifications. The time constant of *R1* and *C* should be designed around the order of $\sim$1 μs to distinguish the power-on transition (with a rise time of several milliseconds) from the ESD transition (with a rise time of several nanoseconds) [4].

If Mn1 is turned on during ESD transition by unexpected coupling effect to its gate through the parasitic capacitance in the layout, the base voltage of the lateral BJT could be pulled down to zero to turn off the lateral BJT in the STnMOS device. To avoid such possible condition during ESD transition, the Mn2 is added in the ESD detection circuit to keep the gate of Mn1 and Mp2 at 0 V, when the base voltage of lateral BJT in the STnMOS device is charged up by the current flowing through Mp1 and Mp2.

IV. Experimental Results

The proposed power-rail ESD clamp circuit has been designed and fabricated in a 130-nm 1-V/2.5-V CMOS process. The stand-alone STnMOS with the same device dimension and layout has been also fabricated in the same chip for reference. In the test structures, all the STnMOS devices are salicide-blocked whereas all the ESD detection circuits are fully salicided. The stand-alone 2.5-V STnMOS has a bipolar trigger voltage ($V_{\rm t1}$) of 11.7 V and a holding voltage larger than the high power-supply voltage (3.3 V). Therefore, the stand-alone STnMOS is not a good power-rail ESD clamp device due to its high bipolar trigger voltage. In this section, the experimental results will show that the new proposed ESD detection circuit can effectively lower the $V_{\rm t1}$ and substantially increase the ESD robustness of STnMOS. Moreover, the experimental results also show that the proposed ESD detection circuit can successfully distinguish the normal power-on transition and the ESD transition. Therefore, ICs with the new proposed high-voltage-tolerant power-rail ESD clamp circuit have no risk of latch-up issue.

A. Standby Leakage Current

To save the power consumption of portable devices or low-power applications, especially chips that are driven by small batteries, the standby leakage current becomes one of major concerns [11], [12]. The measured leakage currents of the fabricated power-rail ESD clamp circuit under different temperatures are shown in Fig. 4, where the STnMOS is drawn with a device dimension (W/L) of 300 μm/0.3 μm. With a leakage current of $\sim$20 nA under the temperature of 125 °C, leakage current of the new proposed power-rail ESD clamp circuit is quite small as comparing to those of the prior arts. Table II summarizes the comparison on the leakage current between the new proposed power-rail ESD clamp circuit and the prior arts [10], [25]. In [22], diode strings were fabricated on p-substrate with epitaxial layer, which can suppress the beta gain of parasitic BJT and therefore reduce the overall leakage current of diode strings. However, epitaxy is a quite costly process step, so that most consumer IC products are not fabricated on epitaxial substrate if they have to compromise with their costs. Therefore, diode strings fabricated on a 0.35-μm CMOS process without

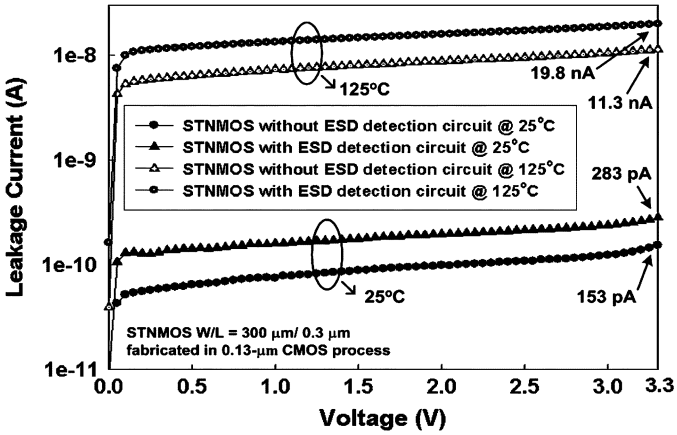

Fig. 4. Leakage currents of STnMOS with or without the ESD detection circuit under different temperatures.

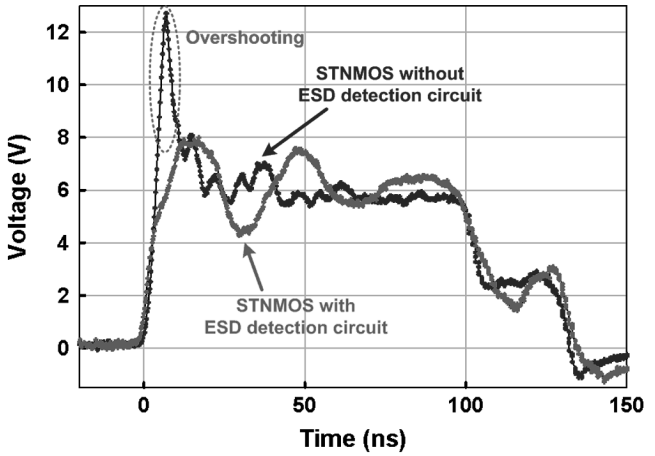

Fig. 5. The clamped voltage waveforms by STnMOS with or without the ESD detection circuit under the voltage pulse stress with the pulse height of 20 V and the rise time of 10 ns.

TABLE II
LEAKAGE CURRENT OF PRIOR ARTS AND THE NEW PROPOSED POWER-RAIL ESD CLAMP CIRCUIT

	Temperature		Number of diodes	Operating voltage
	25°C	125°C		
pure diode string	12.45 μA	3.45 mA	6	3.3 V
Cladded diode string	3.5 μA	3.33 mA	6	3.3 V
Boosted diode string	44.03 μA	0.61 mA	8	3.3 V
Cantilever diode string	4.96 μA	1.25 mA	6	3.3 V
stacked-PMOS clamp	~ 0.8 μA	~ 8 μA		3.3 V
this work	283 pA	19.8 nA		3.3 V

epitaxial layer in [25] is compared with the proposed design of this work instead of diode strings in [22].

B. Turn-On Verification

One of the main benefits of the new proposed power-rail ESD clamp circuit is to enhance the turn-on speed of ESD clamp device (STnMOS) during ESD stress conditions. The turn-on speed of the STnMOS device with or without ESD detection circuit is measured in Fig. 5, where a voltage pulse with pulse height of 20 V and rise time of 10 ns is applied to the $V_{\rm DD}$_h. The time to clamp the 20-V voltage pulse to the holding voltage level ($\sim$5.8 V) by the stand-alone STnMOS device is about $\sim$20 ns, as shown in Fig. 5. Moreover, the overshooting peak voltage of the stand-alone STnMOS in Fig. 5 is about $\sim$13 V, which could be higher than the gate-oxide breakdown voltage of the low-voltage devices in the internal circuits. On the contrary, the 20-V voltage pulse can be quickly clamped by the STnMOS with ESD detection circuit to a low voltage level without overshooting. This result verifies that the turn-on speed of the STnMOS can be indeed improved by the proposed ESD detection circuit. The clamped voltage level will be limited by the snapback holding voltage of the STnMOS device, after the lateral n-p-n BJT in the STnMOS device is triggered on by the ESD detection circuit. From the measured voltage waveforms in Fig. 5, the excellent turn-on efficiency of the new proposed power-rail ESD clamp circuit has been successfully verified. Therefore, the internal circuits can be effectively protected by the new proposed power-rail ESD clamp circuit in cooperation with the whole-chip ESD protection schemes shown in Fig. 1.

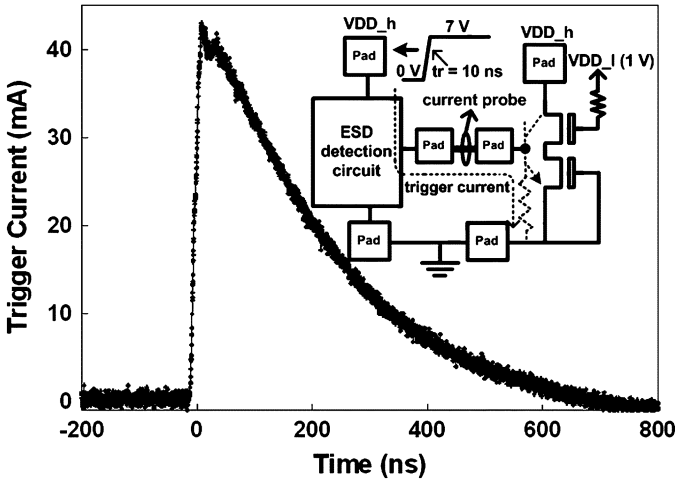

Fig. 6. The measured substrate-triggered current generated by the ESD detection circuit under 0-to-7 V voltage pulse with a rise time of 10 ns on the $V_{\rm DD}$_h pin.

To verify the effectiveness of the ESD detection circuit in the proposed power-rail ESD clamp circuit, a measurement setup is shown in the inset of Fig. 6 to observe the substrate-triggered current. In the specially drawn testchip, the output node of a stand-alone ESD detection circuit is also connected to another pad. The substrate trigger node of a stand-alone STnMOS is connected to a pad. In the circuit board, the output node of a stand-alone ESD detection circuit is connected to the substrate trigger node of a stand-alone STnMOS by a wired line. A current probe is used to measure the transient current flowing through this wired line. With such measurement setup, the measured substrate-triggered current generated by the ESD detection circuit under 0-to-7 V voltage pulse with a rise time of 10 ns on the $V_{\rm DD}$_h pin is shown in Fig. 6. The substrate-triggered current almost simultaneously appears with a peak current of $\sim$43 mA, when the 0-to-7 V voltage pulse is applied to $V_{\rm DD}$_h pin. So, the STnMOS with ESD detection circuit can be quickly triggered on to clamp the overstress ESD voltage, as the clamped voltage waveform shown in Fig. 5. After 800 ns, the voltage at the gate of the pMOS Mp1 follows up the given 0-to-7 V voltage

TABLE III
ESD ROBUSTNESS OF STNMOS DEVICES WITH OR WITHOUT THE NEW PROPOSED ESD DETECTION CIRCUIT

STNMOS W/L (μm/μm)	HBM ESD Level (kV)		MM ESD Level (V)	
	without detection circuit	with detection circuit	without detection circuit	with detection circuit
300/0.3	1	3.75	150	250
400/0.3	1.5	5	175	325
600/0.3		6.5		375

transient. Therefore, the ESD detection circuit is turned-off and the measured trigger current drops to zero. The timing for the gate voltage of Mp1 to follow up the transient voltage applied to $V_{\rm DD}$_h pin can be controlled by changing the *R1* and *C* values and is designed to distinguish between the power-on transition and the ESD transition.

C. ESD Robustness

With sufficient substrate-triggered current, the STnMOS can be directly triggered into its holding region without snapback switching. Therefore, the turn-on speed of the proposed power-rail ESD clamp circuit can be significantly improved to effectively protect the internal circuits with low-voltage devices and thin gate oxide [28]. Moreover, the substrate-triggered current can uniformly trigger on the STnMOS under ESD stress, so that the STnMOS with a larger device dimension results in a smaller turn-on resistance in the pulsed *I–V* response. To keep a lower overshooting voltage during ESD stress, the STnMOS with large enough device dimension should be chosen when the internal circuits are implemented with the low-voltage devices [28]. Table III summarizes the human-body- model (HBM) [1] ESD robustness and the machine-model (MM) [2] ESD robustness of the STnMOS devices with and without the ESD detection circuit. Measurement results have shown great improvement on ESD robustness of the STnMOS with the ESD detection circuit, as comparing with that of the stand-alone STnMOS devices. The HBM and MM ESD levels are measured by KeyTek ZapMaster and the devices are judged ESD failure if their *I–V* characteristic curves shift over 20% after three continuous ESD zaps at every ESD test level.

D. SCR as ESD Clamp Device

The SCR device, which is composed of cross-coupled n-p-n and p-n-p BJTs with regenerative feedback, has been found to play an important role for ESD protection in very deep sub-micron CMOS technologies. However, main concerns of the SCR device as ESD clamp device are the slow turn-on speed and the higher switching voltage ($V_{\rm t1}$). The substrate-triggered technique has been reported as an effective method to lower the $V_{\rm t1}$ and to increase the turn-on speed of SCR devices [29]. Therefore, as another choice of high-voltage tolerant ESD clamp device, the ESD detection circuit in this work was applied on triggering the substrate of SCR devices. The SCR devices, both stand-alone and substrate-triggered, are in series with three diodes to increase its overall holding voltage to 3.8 V to avoid the latch-up issue [30] The TLP measured *I–V* curves of SCR with or without the proposed ESD detection circuit are shown in Fig. 7. In Fig. 7, the stand-alone SCR has a $V_{\rm t1}$ as high as 15.9 V, which is unqualified for protecting internal circuits during ESD transition. With the proposed ESD detection circuit, the $V_{\rm t1}$ can be greatly lowered to 5.6 V. When the substrate-triggered SCR is 30 μm in width, the measured It2 is $\sim$3.4 A. It is increased to be greater than 6 A when the substrate-triggered SCR is 90 μm in width. As a result of the lowered $V_{\rm t1}$ and the increased turn-on speed, SCR device with the proposed ESD detection circuit is also an useful power-rail ESD clamp circuit to the 3.3-V mixed-voltage I/O interfaces.

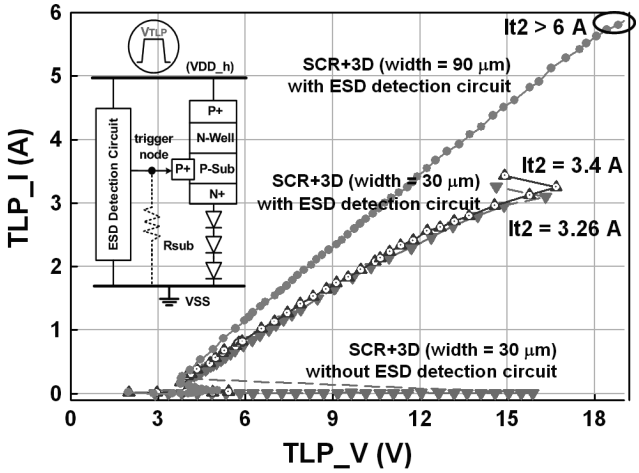

Fig. 7. TLP-measured *I–V* characteristics of both SCR with and without ESD detection circuit.

V. CONCLUSION

A new power-rail ESD clamp circuit realized with low-voltage devices for 1-V/3.3-V mixed-voltage I/O interface has been successfully verified in a 130-nm 1-V/2.5-V CMOS process. As comparing to the stand-alone STnMOS, the turn-on speed of the STnMOS can be effectively improved by the proposed ESD detection circuit. As well as, its HBM (MM) ESD level can be improved from 1 kV (150 V) to 3.75 kV (250 V) for the STnMOS with a device dimension (W/L) of 300 μm/0.3 μm. The ESD detection circuit has also shown significant help on lowering the $V_{\rm t1}$ of SCR devices. This new proposed power-rail ESD clamp circuit with the advantages of very low leakage current, fast turn-on speed, higher ESD robustness, and no gate-oxide reliability issue is an excellent ESD protection solution to the mixed-voltage I/O interface with high-voltage I/O signals.

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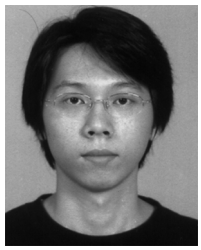
Ming-Dou Ker (S'92–M'94–SM'97) received the B.S. degree in electronics engineering and the M.S. and Ph.D. degrees in electronics from the National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1986, 1988, and 1993, respectively.

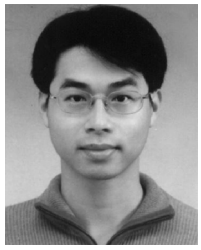
In 1994, he joined the Very Large Scale Integration (VLSI) Design Department, Computer and Communication Research Laboratories (CCL), Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan, R.O.C., as a Circuit Design Engineer. In 1998, he became a Department Manager with the VLSI Design Division, CCL/ITRI. Currently he is a Full Professor in the Department of Electronics Engineering, National Chiao-Tung University. He has been invited to teach or help electrostatic discharge (ESD) protection design and latchup prevention by hundreds of design houses and semiconductor companies in Taiwan, R.O.C.; Silicon Valley, San Jose, CA.; Singapore; and Mainland China. His research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed or mixed-voltage I/O interface circuits, special sensor circuits, and thin-film transistor (TFT) circuts. In the field of reliability and quality design for CMOS integrated circuits (ICs), he has authored or coauthored over 270 technical papers in international journals and conferences. He has invented hundreds of patents on reliability and quality design for ICs, which have been granted with 112 U.S. patents and 122 Taiwan patents. His inventions on ESD protection designs and latchup prevention methods have been widely used in modern IC products.

Dr. Ker has serviced as member of the Technical Program Committee, Sub-Committee Chair, and Session Chair of numerous international conferences. He is currently serving as Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He was elected as the first President of the Taiwan ESD Association in 2001. He has also been the recipient of numerous research awards presented by ITRI, the National Science Council, National Chiao-Tung University, and the Dragon Thesis Award presented by the Acer Foundation. In 2003, he was selected as one of the Ten Outstanding Young Persons in Taiwan, R.O.C., by the Junior Chamber International (JCI). One of his inventions has been awarded with Taiwan National Invention Award in 2005.



Wen-Yi Chen was born in Taiwan in 1981. He received the B.S. degree in electronics engineering and the M.S. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 2003 and 2005, respectively.

He is currently with the Chinese army for military service. His researches are related to on-chip ESD protection design in CMOS integrated circuts, especially in the field of high-voltage tolerant applications.



Kuo-Chun Hsu (S'01–M'03) received the B.S. degree in electronics engineering from National Chung-Hsing University, Taichung, Taiwan, R.O.C., in 1998 and the M.S. and Ph.D. degrees from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 2000 and 2003, respectively.

In 2004, he joined the Mixed-Signal Design Department, Global UniChip Corporation, Science-Based Industrial Park, Hsinchu, Taiwan, R.O.C., as a Principal Engineer. His main research includes mixed-signal circuit design and electrostatic discharge protection circuit design.

Dr. Hsu was awarded with the *Dragon Thesis Award* by Acer Foundation, Taiwan, in 200 for his Ph.D. dissertation. He was elected an honorary member of the Phi Tau Phi Society.