Investigation of Programming Charge Distribution in Nonoverlapped Implantation nMOSFETs

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Abstract—Novel gate-to-drain nonoverlapped-implantation (NOI) nMOSFETs have been developed as potential multibit-per-cell nonvolatile-memory (NVM) devices. The lateral charge distribution of the NOI NVM device programmed by channel hot electron injection is investigated by charge-pumping (CP) techniques with presumed interface trap distributions. For the first time, the CP results have revealed the lateral charge distribution and trapping density at the NOI's programmed state. The maximum trapping charge density locates near its drain junction. The charge distribution is estimated about 90 nm in length and spread widely over the NOI region. Two-dimensional simulators with charge bars using the same charge trapping distribution confirm the experimental results by fitting their $I_{\mathrm{DS}} - V_G$ curves.

Index Terms—Channel hot electron injection (CHEI), charge-pumping, nonoverlapped implantation (NOI), nonvolatile memory (NVM).

I. INTRODUCTION

RECENTLY, the discrete charge trapping nonvolatile-memory (NVM) devices received much attention due to their potential multibit storage in a unit cell. In contrast to those floating gate memories, oxide–nitride–oxide (ONO) charge trapping structures are explored to store charges in NROM [1] and TwinMONOS [2] for high-density NVM devices. Newly developed gate-to-drain nonoverlapped-implantation (NOI) MOSFETs are proposed by using the silicon nitride (SiN) spacers as charge trapping media [3]. They are fully compatible with existing industrial CMOS fabrications without adding process modification and mask tooling cost. Channel hot electron injection (CHEI) and band-to-band hot hole enhanced injection (HHEI) are used to program and erase the NOI device for NVM operations. However, the exact lateral locations of charge injection as well as the trapping distributions in the NOI devices have never been characterized. In 1998, Chen and Ma proposed an improved charge-pumping (CP) method to directly profile the hot-carrier-induced oxide charge for the investigation of the oxide damage in electrically erasable programmable read-only memory (EEPROM)

devices [4]. They presented a maximum lateral trapped charge-density distribution of 4×10^{12} cm^{-2} in the gate oxide by a CP. However, Eitan and co-workers argued the CP accuracy in profiling the trapped charges since the CP techniques require a uniform interface-state distribution, which is not always a true assumption [5]. Therefore, it is challenging for the CP to overcome the nonuniform interface states. The goal for the proposed CP method in this paper is to clarify whether the distribution uniformity of interface states has a severe or limited impact on the accuracy of lateral charge profiling in the NOI nMOSFETs. If this effect is found minor, the CP technique may be still satisfactory for analyzing NOI devices. Furthermore, the NOI's charge-profiling investigation is extremely valuable to fully understand its carrier injection mechanism, future scalability, and reliability degradation caused by channel hot electrons.

II. EXPERIMENTS

The NOI nMOSFETs for CP experiments are fabricated by a typical 0.25-μm CMOS processing. Their channel width/length is designed as 1/0.25 μm for resembling a real array cell and detectable CP current level. A gate oxide thickness of 7 nm is chosen for 7-V programming operations. And the length of N+ overlapped region under the SiN spacer, i.e., the lateral drive-in distance, is 50 nm. In the 0.25-μm CMOS processing, the spacer length is about 125 nm. Therefore, the length of nonoverlap region under the SiN spacer is calculated about 75 nm.

The basic experimental system setup for CP is illustrated in Fig. 1. The trapezoidal pulses with alterable high voltage V_h are generated by a pulse generator and applied to the gate of a NOI device. The base level V_b of pulses is fixed at -2 V, which is below the flatband voltage (V_{FB}) in the channel in order to prevent the trapped charge from disturbing. The applied pulsewidth is set at 1 μs with 50% duty cycle, while the rise/fall time is 50 ns. The NOI NVM device operating conditions of program/read/CP are summarized in Table I.

The following are the steps involved in measuring the CP currents and deducing the related local threshold-voltage shifts.

1) Sampling the CP current I_{CP} of a virgin NOI device by a semiconductor parameter analyzer from ground either at drain-side or source-side junction by leaving the other side electrically floating.
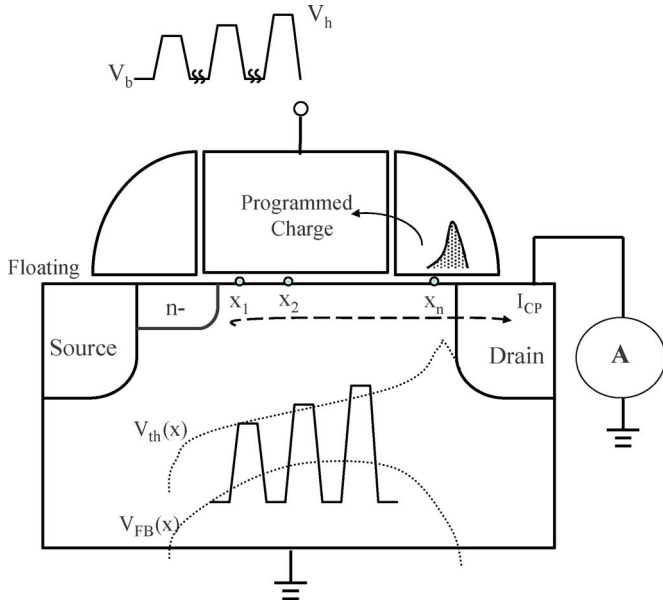
Fig. 1.　Experimental setup for NOI CP measurement.

TABLE I
OPERATION CONDITIONS OF PROGRAM/READ/CHARGE-PUMPING
FOR NOI DEVICES

	V_G (V)	V_D (V)	V_S (V)
Program	7	6	Ground
Read	1.5	Ground	1.5
Charge Pumping	V_h: -1~2V, (swept, step 0.05V) V_b: -2V, (fixed) f: 0.5MHz, 50% duty cycle Rise/Fall time:50nS	Ground (when V_S floating)	Ground (when V_D floating)

2) Based on the presumption of interface-state distribution N_{it}, the N_{it} can be derived theoretically from the measured $I_{CP,max}$.

3) Creating the transfer curve or lookup table for determining each x correspondent to each $I_{CP}(V_h)$.

4) Deriving the $V_{th}(x)\_D$ and $V_{th}(x)\_S$ from CP currents measured from drain-side and source-side junctions, respectively.

5) Combining the $V_{th}(x)\_D$ and $V_{th}(x)\_S$ by ruling out far-end inaccuracy to obtain the local threshold voltage $V_{th}(x)$ in the NOI device.

6) Programming the NOI NVM device and measuring its CP currents from drain side and source side again.

7) Repeating the above procedures from steps 2) to 5), and deriving the local threshold voltage $V_{th}(x)$ at the programmed state.

8) Subtracting initial local $V_{th}(x)$ by programmed local $V_{th}(x)$ and then obtaining the local $\Delta V_{th}(x)$.

The CP currents I_{CP} will be generated within each lateral distance x, where the swept high voltage $V_h \geqq V_{th}(x)$. All of the $I_{CP}(V_h)$ are collected at a grounded S/D junction by sweeping the pulse chain having V_h from -1–2 V with
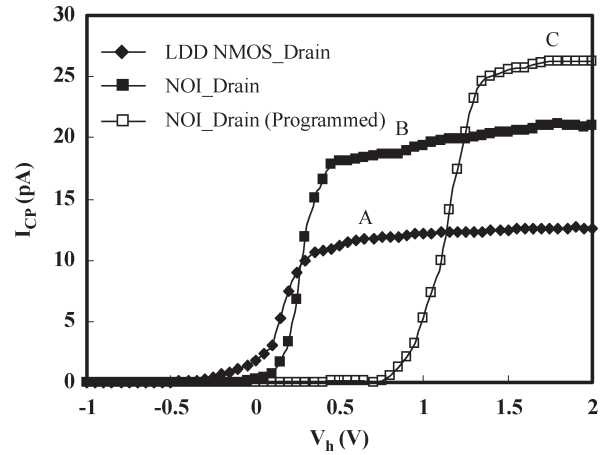

Fig. 2.　Initial/programmed CP current collected from the drain side. Curve c indicates electrons trapped in SiN spacer and additional interface states generated after programming NOI NVM device.
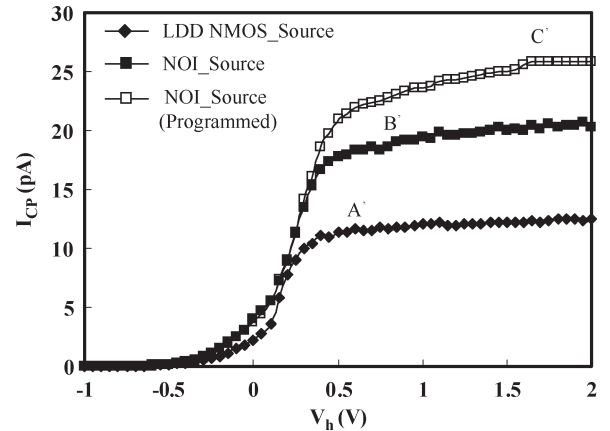

Fig. 3.　Initial/programmed CP current collected from the source side.

0.05-V per step. Eventually, as the swept high voltage V_h exceeding the local V_{th} in the channel, the CP current will saturate to $I_{CP,max}$. In the following sections, the lateral charge-profiling methodology will be discussed and derived from CP current I_{CP}. After CP experiments, the derived charge distribution will be put into a two-dimensional (2-D) simulator and fitted with experimental $I_{DS} - V_G$ curves for final verifications.

To avoid the 2-bit charge trapping effect, only one side of the NOI region is formed under the SiN spacer and programmed to 0.8-V threshold-voltage shift (program conditions: $V_G = 7$ V, $V_D = 6$ V, V_S and V_B ground). Fig. 2 shows the CP currents I_{CP}, which are collected from drain sides of a NOI device at initial and programmed states as well as a standard lightly doped drain (LDD) nMOSFET for reference. Those measured I_{CP} currents from their source sides in the same devices are separately shown in Fig. 3. In comparison with a standard LDD nMOSFET as found in Fig. 2, the I_{CP} of the initial NOI device shifts to higher local V_{th} and higher $I_{CP,max}$ due to the increased N_{it} in the nonoverlapped region. As also indicated in Fig. 2, the program stress not only generates additional N_{it} but also introduces negative charge (electrons) in SiN spacer and further shifts I_{CP} curve to the highest local V_{th}. Fig. 3 again
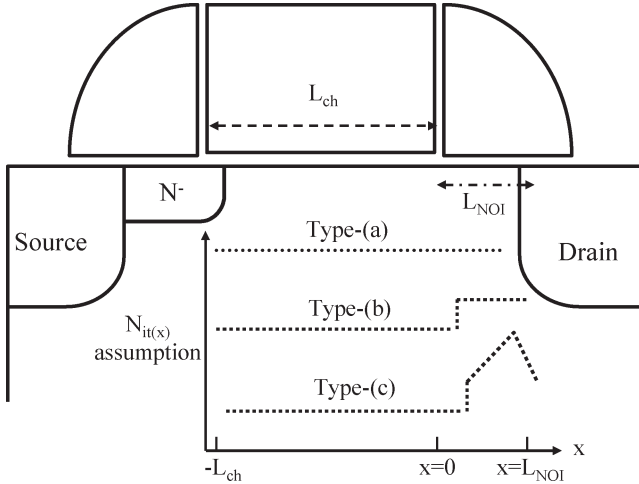
Fig. 4. N_{it} assumption for various types. Type (a): Initial state $N_{it}(x)$ (uniform distribution), Type (b): Initial/Programmed state $N_{it}(x)$ (low–high distribution), and Type (c): Programmed state $N_{it}(x)$ (linear distribution).

confirms these similar findings in the standard LDD nMOSFET and the NOI device at its initial and program states.

In the conventional CP method proposed by Ma *et al.*, the lateral charge profile is derived by assuming a uniform N_{it} distribution. However, Eitan *et al.* pointed out the CP discrepancy in positioning the trapped charges, since the CP techniques to characterize the localized charge-trapping NVM device are based upon a spatially uniform N_{it} distribution, which is inevitably changed by hot carrier injections. Results shown in Figs. 2 and 3 are also indicating that N_{it} in NOI channel region is higher than that of normal channel regions under the gate. From the above discussion, a low–high N_{it} distribution is proposed for an initial NOI device as illustrated in the type-b distribution of Fig. 4. In order to represent a realistic N_{it} profile damaged by local charge injections, a type-c N_{it} distribution has been proposed for a programmed NOI device as also shown in Fig. 4.

III. CHARGE PROFILING AND DISCUSSION

In measuring the CP current of a standard LDD nMOSFET and NOI devices by sweeping $V_h = V_{th}(x)$ and constantly keeping $V_b < V_{FB}$, the CP current $I_{CP}(V_h)$ is generated by $N_{it}(x)$ at a lateral distance x, within which $V_{th}(x) \leqq V_h$ [6]–[9]. For a low–high N_{it} distribution in the type-b curve where N_{it} is equal to N_{itL} at the normal channel and N_{itH} at the NOI channel, $I_{CP}(V_h)$ collected from source side ($x = -L_{ch}$) can be calculated in the following integration:

$$I_{CP}(V_h) = qfW \int_{-L_{ch}}^{x} N_{itL}(x)dx, \qquad -L_{ch} \leqq x \leqq 0$$

$$= qfW N_{itL} \cdot L_{ch} + qfW \int_{0}^{x} N_{itH}(x)dx,$$

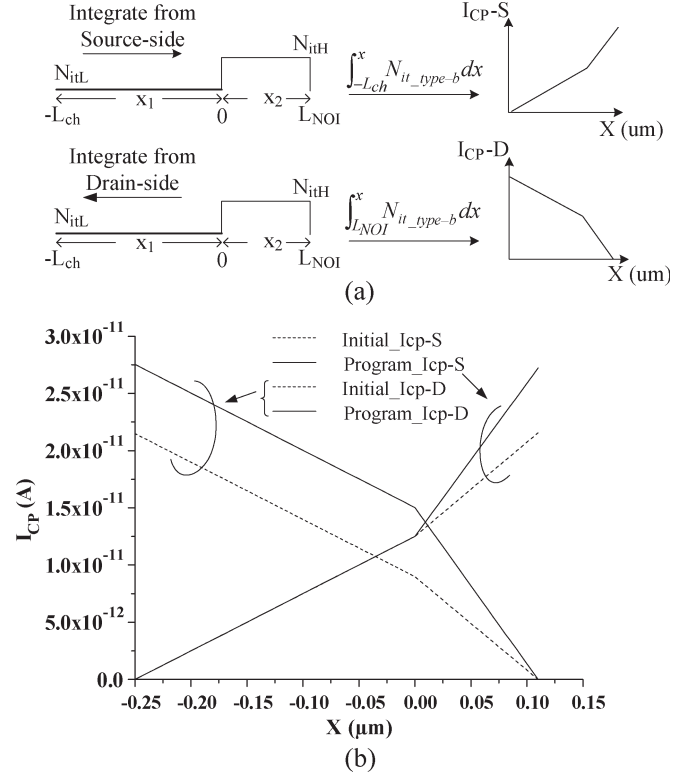$$0 \leqq x \leqq L_{NOI}. \qquad (1)$$

Fig. 5. (a) Formation of transfer curve by integrating type-b $N_{it}(x)$ assumption. (b) Initial/Program state transfer curves for type-b $N_{it}(x)$ assumption.

Two local maximum CP currents, i.e., $I_{CP,\max L}$ and $I_{CP,\max H}$ at the normal and NOI channels are derived from (1) as follows:

$$I_{CP,\max L} = qfW \int_{-L_{ch}}^{0} N_{itL}(x)dx = qfW N_{itL} \cdot L_{ch} \qquad (2)$$

$$I_{CP,\max H} = qfW \int_{-L_{ch}}^{0} N_{itL}(x)dx + qfW \int_{0}^{L_{NOI}} N_{itH}(x)dx$$

$$= qfW N_{itL} \cdot L_{ch} + qfW N_{itH} \cdot L_{NOI}. \qquad (3)$$

Consequently, N_{itL} and N_{itH} can then be obtained in the following equations:

$$N_{itL} = \frac{I_{CP,\max L}}{qfW L_{ch}} \qquad (4)$$

$$N_{itH} = \frac{I_{CP,\max H} - qfW N_{itL} L_{ch}}{qfW L_{NOI}}. \qquad (5)$$

The N_{itL} in (4) is first found by measuring the maximum chare pumping current $I_{CP,\max L}$ in a standard LDD nMOSFET without introducing any NOI channel. On the other hand, the N_{itH} in (5) is later calculated from the previously derived $I_{CP,\max L}$ measured from a standard LDD nMOSFET and $I_{CP,\max H}$ measured from the NOI device. After obtaining N_{itL} and N_{itH}, an I_{CP}-position(x) transfer curve can be theoretically generated by (1). As illustrated in Fig. 5(a), transfer curves are obtained by integrating type-b $N_{it}(x)$ from the source
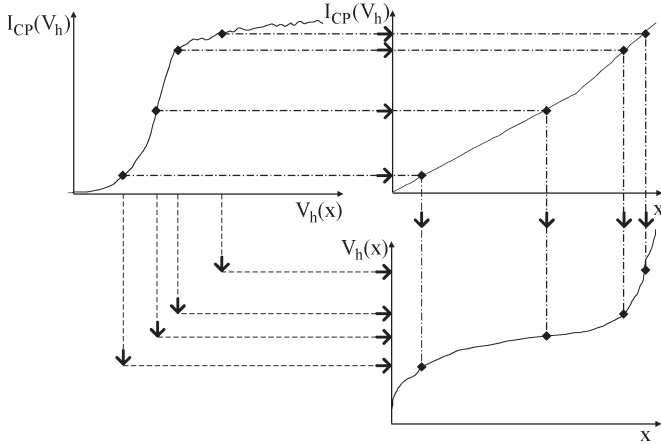
Fig. 6.   Transferring scheme from $I_{\mathrm{CP}}(V_h)$ to a local threshold $V_{\mathrm{th}}(x)$.

junction toward the drain junction and from the drain junction toward the source junction, respectively. These transfer curves are used to determine each x corresponding to each $I_{\mathrm{CP}}(V_h)$. The first transfer curve is representing the relationship between $I_{\mathrm{CP}}(V_h)\_S$ and position(x) measured at the source side for an initial NOI device. From the drain side of measurements, the second I_{cp}_D-position(x) transfer curve can be derived. Two other transfer curves, i.e., $I_{\mathrm{CP}}(V_h)\_S$ and $I_{\mathrm{CP}}(V_h)\_D$, for a programmed NOI device are also established by following the same procedures. Fig. 5(b) shows all four transfer curves as described above. Compared to the initial curve, the slope of the programmed curve increases as N_{it} increases after programming NOI device. Fig. 6 demonstrates point-to-point transferring examples from $I_{\mathrm{CP}} - V_h$ to V_h-position(x) through an I_{CP}-position(x) transfer curve. However, according to the studies in [5], the interface states will distribute nonuniformly using the CHEI to program a virgin NVM device. As also found in Figs. 2 and 3, a nonuniform N_{it} distribution needs to be considered in case of programmed devices. The type-c distribution in Fig. 4 defines a linearly increased N_{it} in a programmed NOI device. In the same way, as illustrated in Fig. 7(a), the transfer curves of $I_{\mathrm{CP}}(V_h) - x$ are obtained by integrating type-c $N_{\mathrm{it}}(x)$. Four I_{CP}-position(x) transfer curves for the type-c distribution can therefore be determined according to the maximum CP currents at initial and programmed states as shown in Fig. 7(b). And the positioning mismatch between Figs. 5(b) and 7 (b) is found less significant, since the change of N_{it} on NOI channel is insensitive in two cases, i.e., type (b) and type (c). This is also indicated that CP remains valid if N_{it} can be assumed properly.

Apart from the conventional CP technique, a complete local threshold voltages $V_{\mathrm{th}}(x)$ is obtained by combining the $V_{\mathrm{th}}(x)\_D$ and $V_{\mathrm{th}}(x)\_S$, which are derived from the drain side and source side I_{CP}, respectively. The method of combining $V_{\mathrm{th}}(x)\_D$ and $V_{\mathrm{th}}(x)\_S$ is adopting valid portions of $V_{\mathrm{th}}(x)\_D$ and $V_{\mathrm{th}}(x)\_S$, rather than their weighted summation. Nevertheless, it is the weighted correction of nonuniform N_{it} distributions, such as type (b) and (c) in Fig. 4. As illustrated in Fig. 8, the far-end curve inaccuracy of individual $V_{\mathrm{th}}(x)\_D$ and $V_{\mathrm{th}}(x)\_S$ will be ruled out for establishing the entire local threshold-voltage distribution. The far-end error of
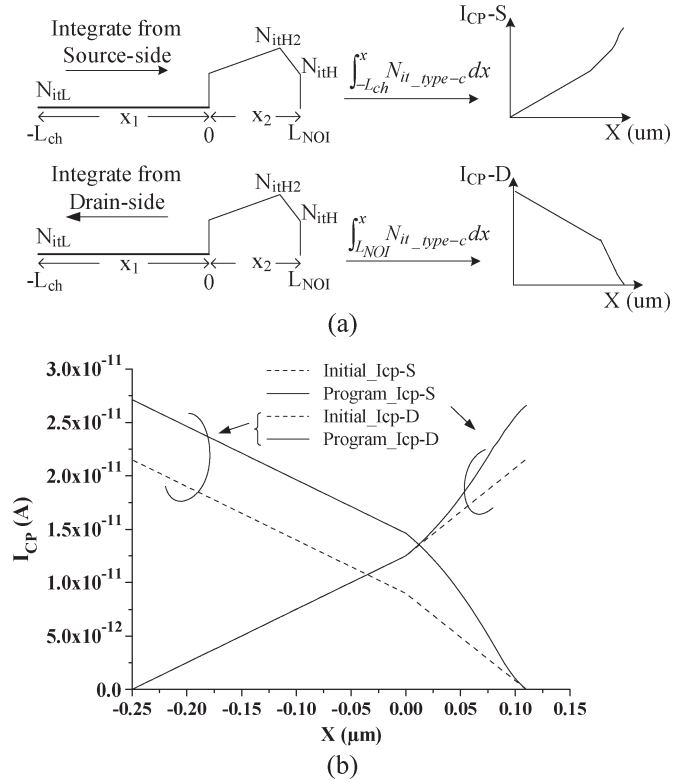

Fig. 7.   (a) Formation of transfer curve by integrating type-c $N_{\mathrm{it}}(x)$ assumption. (b) Initial/Program state transfer curves for type-c $N_{\mathrm{it}}(x)$ assumption.
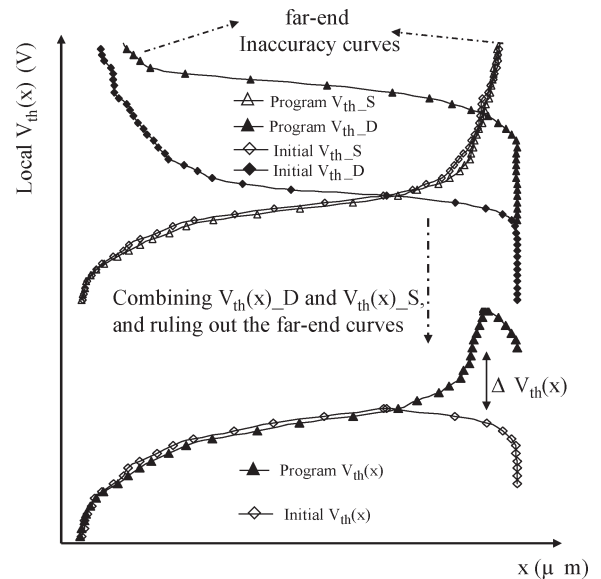

Fig. 8.   Combining the $V_{\mathrm{th}}(x)\_D$ and $V_{\mathrm{th}}(x)\_S$ and ruling out the far-end inaccuracy to complete the initial/programmed local threshold voltage $V_{\mathrm{th}}(x)$ in the NOI device.

the local $V_{\mathrm{th}}(x)$ derived from single-side $I_{\mathrm{CP}}(V_h)$ is introduced once the local $V_{\mathrm{th}}(x)$ is decreasing other than gradually increasing along the channel. By combining two $V_{\mathrm{th}}(x)$ curves from both S/D sides, a complete local threshold voltage $V_{\mathrm{th}}(x)$ can be accomplished. Here, a monotonically increased local V_{th} from the source side and drain side is presumed and holds valid, only if there is only one locally maximum V_{th} existing in the NOI channel. Both $V_{\mathrm{th}}(x)\_D$ and $V_{\mathrm{th}}(x)\_S$ curves of Fig. 8
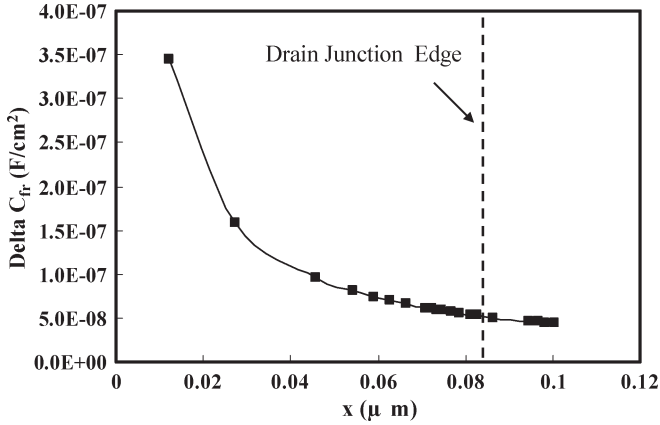
Fig. 9. Fringing capacitance ΔC_{fr} corresponds to each distance x in the SiN spacer.

Fig. 10. Local threshold voltage $V_{\mathrm{th}}(x)$ for N_{it} assumption of three types along the lateral position in a programmed NOI device. Positioning mismatch between different $N_{\mathrm{it}}(x)$ is indicated as Δx.

increase monotonically from the starting (or I_{CP} measuring) junction toward the far-end (or floating) junction. However, these local $V_{\mathrm{th}}(x)$ curves fail to locate correct positions beyond the point of the maximum local V_{th}, because the channel current adding to the recombination currents I_{CP} after V_h is higher than the maximum local V_{th} [10]. The intersection of $V_{\mathrm{th}}(x)\_D$ and $V_{\mathrm{th}}(x)\_S$ is the only maximum V_{th} that can fulfill both monotonous functions, since only one local maximum V_{th} is presumed. By using valid portions of those $V_{\mathrm{th}}(x)\_D$ with $V_{\mathrm{th}}(x)\_S$ curves whose V_{th} are lower than the maximum V_{th}, Mahapatra et al. also reported similar local maximum V_{th} using CP techniques in their lateral asymmetric channel MOSFETs [11].

After obtaining the initial and programmed state $V_{\mathrm{th}}(x)$, the trapped charge distribution can be deduced by the local $\Delta V_{\mathrm{th}}(x)$, i.e., the difference between the initial and programmed local $V_{\mathrm{th}}(x)$. The local $\Delta V_{\mathrm{th}}(x)$ is influenced by nitride trapped charges $Q_{\mathrm{nt}}(x)$, and C_{fr}, which is the fringing capacitance per unit area between the gate electrode and NOI channel. The $Q_{\mathrm{nt}}(x)$ is simplified as a thin charge sheet located right above the interface between the SiN spacer and tunneling oxide without considering the effect of vertical charge distributions. Consequently, the programmed charge distribution $N_{\mathrm{nt}}(x)$ can be determined by multiplying the local $\Delta V_{\mathrm{th}}(x)$ and $\Delta C_{\mathrm{fr}}(x)$ corresponding to each lateral position (x)

$$N_{\mathrm{nt}}(x) = \frac{Q_{\mathrm{nt}}(x)}{q} = \frac{\Delta C_{\mathrm{fr}} \cdot \Delta V_{\mathrm{th}}(x)}{q}$$

where ΔC_{fr} represents the local fringing capacitance per unit area from position x to $x + \Delta x$ as shown in Fig. 9, and it can be approximated as follows [12]–[14]:

$$\Delta C_{\mathrm{fr}} = \frac{2\varepsilon_{\mathrm{SiN}}}{\pi} \ln(1 + \frac{\Delta x}{x}), \qquad 0 \leqq x \leqq L_{\mathrm{NOI}}.$$

Fig. 10 shows local $V_{\mathrm{th}}(x)$ distribution curves of the programmed state for type-a, type-b, and type-c N_{it} assumptions, and their mismatch is also indicated. The maximum positioning difference between type b and type c is about 5 nm near the center of NOI channel. However, there is a 22-nm positioning mismatch between type b and type a. This also indicates a
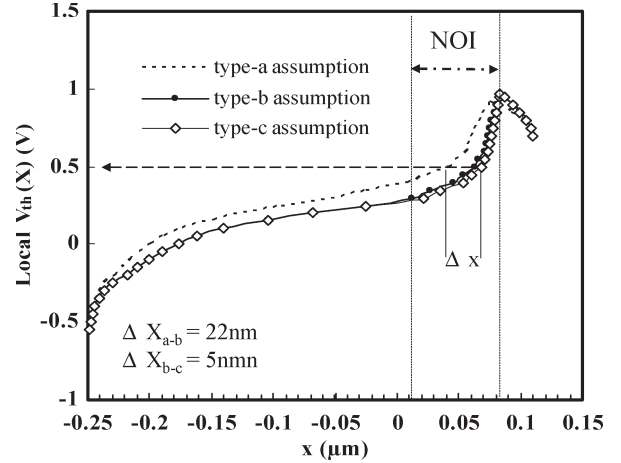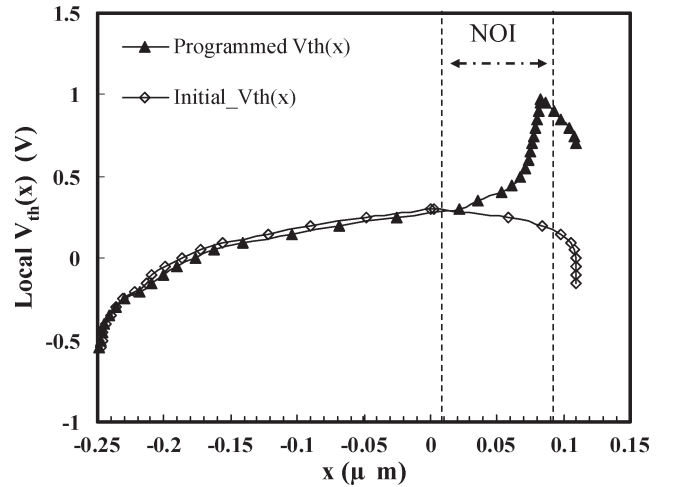

Fig. 11. Local threshold voltage $V_{\mathrm{th}}(x)$ of the programmed and initial states for obtaining the $\Delta V_{\mathrm{th}}(x)$. The maximum $V_{\mathrm{th}}(x)$ is near the drain junction.

little profiling inaccuracy by both nonuniform N_{it} in the NOI devices. By assuming type-c N_{it} distributions for the initial and programmed NOI device, respectively, the spatial distributions of the local $V_{\mathrm{th}}(x)$ along the channel are derived and shown in Fig. 11. After taking the fringing capacitance, local ΔV_{th}, and Δx into account, the lateral charge trapping distribution can be calculated for each measured CP position(x) as shown in Fig. 12. It is found that the charge trapping density peaks close to the drain junction edge even though the fringing field is significantly decreased along the nonoverlapped channel away from the gate edge. In contrast to NROM device, which was reported about 40 nm for their charge trapping length [15], NOI devices here demonstrate that their trapped charges widely spread over a large portion of the SiN spacer for more than 90 nm in length above the nonoverlapped channel region.

IV. SIMULATION

In order to verify the lateral trapped charge distribution in NOI devices by the new CP technique, simulated charge bars are laterally placed in the commercially available 2-D
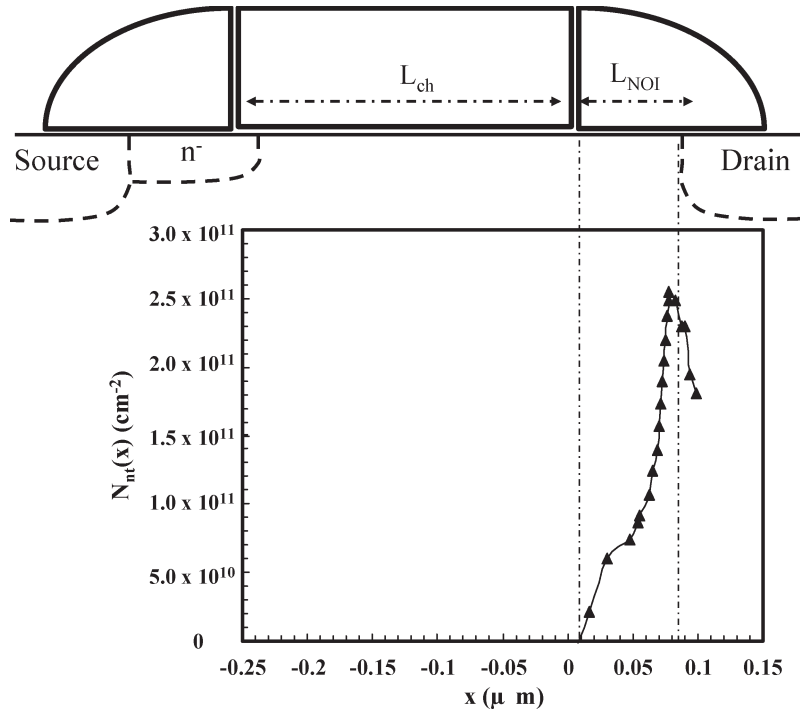
Fig. 12.   Trapped charge distribution with relative positions of NOI MOSFETs. $N_{nt}(x)$ also peaks near the drain-junction edge.

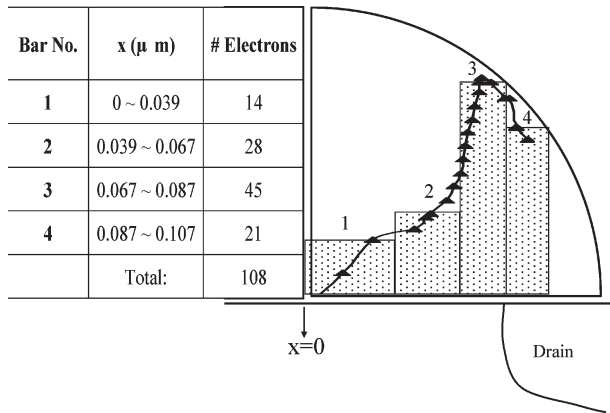| Bar No.	x (µ m)	# Electrons
1	0 ~ 0.039	14
2	0.039 ~ 0.067	28
3	0.067 ~ 0.087	45
4	0.087 ~ 0.107	21
	Total:	108

Fig. 13.   Simulated charge bars related to experimental charge distribution density.
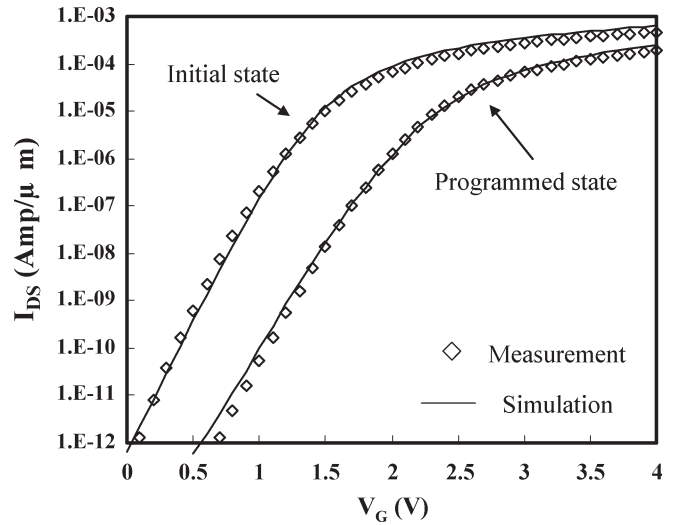

Fig. 14. $I_{DS} - V_G$ comparison of the simulated and experimental results.

simulator. The charge density in these bars is based upon the charge distribution previously derived from the CP current $I_{CP}(V_h)$ [15]. The $I_{DS} - V_G$ characteristic at initial state in a NOI device has been fitted first. The simulation of $I_{DS} - V_G$ at programmed state $(\Delta V_{th} = 0.8$ V$)$ is then carried out by closely placing rectangular charge bars in the SiN spacer without spacing. The width of each charge bar, which ranges from about 20 to 40 nm, is determined by the square root of the NOI trapped charge density. The height of charge bars is tuned in simulations for the best fitting with measured electrical data. The electron trapping concentration used in each charge bar is obtained by integrating the distribution curve of Fig. 12. The charge bar having the maximum electron trap density is located over NOI channel region and closed to the drain junction. Each charge-bar position and its charge concentration used in the

simulation are summarized in Fig. 13. As a result, total four charge bars are placed in the SiN spacer where three of them are placed over the NOI channel region, and the fourth one is over the drain region. For a programmed cell with a width of 1 μm (i.e., $\Delta V_{th} = 0.8$ V), it is estimated that there is a total of 108 trapped electrons in these 2-nm-high charge bars, which contain 14, 28, 45, and 21 electrons, respectively. By placing these bars in the simulator, the $I_{DS} - V_G$ simulation of the programmed NOI device shows a good agreement with its measured $I_{DS} - V_G$ characteristics as illustrated in Fig. 14. However, the amount of trapped charges may be underestimated, since a uniform thin charge sheet having 2-nm-high charge bars is presumably representing those charge trapping

sites. As the injected charges spread further into SiN spacers vertically, these charges are proportionally increased to achieve the same V_{th} shift. A programmed NOI device (i.e., $\Delta V_{\text{th}} = 0.8$ V) with a vertical charge penetration of 26 nm contains only 324 trapped electrons in its charge-bar simulation. Eitan and co-workers reported about 1700 electrons trapped in their 0.5/0.35-μm (W/L) NROM device simulation [15]. Having considered the minimum rules of the current 0.25-μm technology, a 0.3/0.25-μm (W/L) NOI device merely stores less than 100 electrons for 0.8-V V_{th} shift. These relative few electrons become effectively influential on the NOI device's V_{th} due to the largely decreased local fringing capacitance near NOI's drain junction. The NOI device simulation clearly agrees with the CP result and confirms that these submicrometer NOI nMOSFETs are promising as few-electron NVM devices.

V. CONCLUSION

In summary, the spatial characterization of CHEI in NOI NVM devices has been investigated by CP techniques. Various transfer curves with different N_{it} assumptions are proposed for better describing the $I_{\text{CP}}(V_h)$ corresponding to each position x in this improved charge-profiling method. Moreover, the CP result shows that the injected charges widely distribute in the NOI's SiN spacer over the NOI region. The lateral distribution of NOI's trapped charge density peaks near the drain-junction edge after the CHEI. It is the first time to characterize the lateral position of the injected channel hot electrons under the influence of the fringing field in the NOI device. The charge distribution in a SiN spacer is estimated about 90 nm in length and spread widely over the NOI region.

To profile the lateral distribution after the CHEI is becoming very important for those novel multisite-trapping NVM devices such as SONOS, NROM, and NOIs to comprehensively understand their charge transportation, retention, and cycling issues. In comparison with the previous results [16], the interface states on the NOI channel induced by CHEI are found more than that of the NROM cell due to processing damages during the gate and LDD spacer formations. Its N_{it} is further enhanced by hot carrier injection. Therefore, I_{CP} significantly increases after programming, since fringing field induce hot carriers widely spread over SiN spacer for the entire NOI region. Even though the CHEI electrons widely distribute over the SiN spacer above the NOI region, this device requires relatively few electrons in programming for its low fringing capacitance. The improvement of NOI devices requires further study on their lateral and vertical charge distributions at programmed and erased states.

Finally, by incorporating the similar spatial distribution of $N_{\text{nt}}(x)$ in the 2-D device simulator, a good agreement between the simulation and measurement is achieved for NOI's $I_{\text{DS}} - V_G$ characteristics. The simulation has also supported that this CP technique is effective with presumed N_{it} distributions to laterally characterize the trapped charge distribution in NOI devices. Both measured and simulated results successfully demonstrate that the 0.25-μm NOI devices are truly potential few-electron NVM devices for embedded memory applications.

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