Design of Mixed-Voltage I/O Buffer by Using NMOS-Blocking Technique

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***Abstract*—An nMOS-blocking technique for mixed-voltage I/O buffer realized with only $1\times V_{DD}$ devices can receive $2\times V_{DD}$, $3\times V_{DD}$, and even $4\times V_{DD}$ input signal without the gate-oxide reliability issue is proposed. In this paper, the $2\times V_{DD}$ input tolerant mixed-voltage I/O buffer by using the nMOS-blocking technique has been verified in a 0.25-μm 2.5-V CMOS process to serve 2.5/5-V mixed-voltage interface. The $3\times V_{DD}$ input tolerant mixed-voltage I/O buffer by using the nMOS-blocking technique has been verified in a 0.13-μm 1-V CMOS process to serve 1/3-V mixed-voltage interface. The proposed nMOS-blocking technique can be extended to design the $4\times V_{DD}$, $5\times V_{DD}$, and even $6\times V_{DD}$ input tolerant mixed-voltage I/O buffers. The limitation of the nMOS-blocking technique is the breakdown voltage of the pn-junction in the given CMOS process.**

***Index Terms*—Gate-oxide reliability, hot-carrier degradation, interface, junction breakdown, mixed-voltage I/O buffer.**

I. Introduction

THE device dimension of transistors has been scaled toward the nanometer region and the power supply voltage of chips has been also decreased in the nanoscale CMOS technologies [1]. Obviously, the dimension of the shrunk devices makes the chip area smaller to save silicon cost. The lower power supply voltage results in lower power consumption. Therefore, circuit design quickly migrates to the lower voltage level such as 1 V with the advancement of the nanoscale CMOS technology. However, some peripheral components or other integrated circuits (ICs) in an electronic system are still operated at the higher voltage levels, such as 3.3 V or 5 V [2]–[4]. In other words, an electronic system could have several chips operated at different voltage levels. In order to interface these chips with different voltage levels, the conventional I/O buffer is no longer suitable. Several problems arise in the I/O interface between these ICs, such as the gate-oxide breakdown [5]–[8], the hot-carrier degradation [9], and the undesirable leakage current paths [10], [11]. Thus, the I/O circuits applied in the mixed-voltage interface must be designed carefully to avoid these problems.

Fig. 1 shows the conventional tri-state I/O buffer realized with the $1\times V_{DD}$ devices in the mixed-voltage interface, which will suffer the circuit leakage and gate-oxide reliability issues. In the receive mode, the gate voltages of the pull-up pMOS device and the pull-down nMOS device in the conventional tri-state I/O buffer are traditionally biased at V_{DD} and GND to turn off the pull-up pMOS device and the pull-down nMOS device by the pre-driver circuit, respectively. If the input signal at the I/O pad rises up to $2\times V_{DD}$ in the receive mode, the parasitic drain-to-well pn-junction diode in the pull-up pMOS device will be forward biased. Therefore, an undesired leakage current path occurs from the I/O pad to the power supply voltage (V_{DD}) through this parasitic pn-junction diode. Besides, because the gate voltage of the pull-up pMOS device is biased at V_{DD} and the input signal on the I/O pad is $2\times V_{DD}$, the channel of the pull-up pMOS device will be also turned on in the receive mode to conduct another undesired leakage current path from the I/O pad to V_{DD}. Such undesired leakage currents cause not only more power consumption in the electronic system but also possible malfunction in the whole system. In order to avoid the gate-oxide reliability issue, the devices which suffer the gate-oxide overstress were replaced by the thick-oxide devices in some mixed-voltage I/O circuits [12]–[14]. However, using both the thick-oxide and thin-oxide devices in a chip will increase the fabrication cost of this chip.

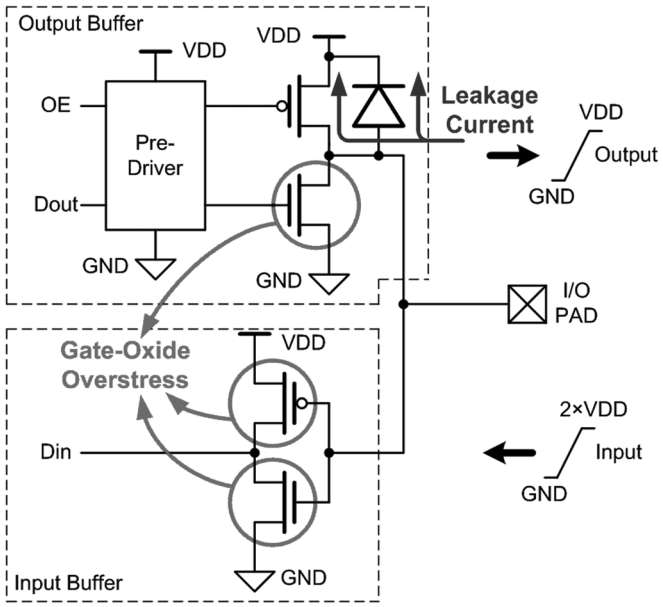

Fig. 1. Conventional tri-state I/O buffer suffering the circuit leakage and gate-oxide reliability issue in the mixed-voltage interface.

Several mixed-voltage I/O buffers realized with the low-voltage (thin-oxide) devices have been reported to save the wafer fabrication cost [15]–[19]. Fig. 2 depicts the design concept of the traditional mixed-voltage I/O buffer realized with only low-voltage devices [15]–[19]. As shown in Fig. 2, the stacked nMOS devices, MN0 and MN1, are used to overcome the high-voltage overstress on their gate oxide. Because

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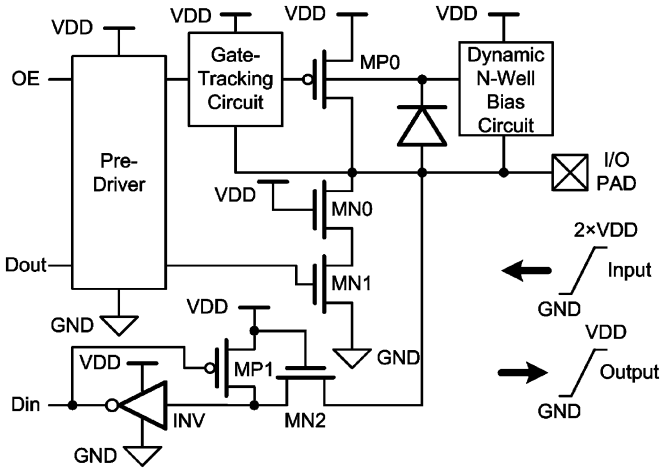

Fig. 2. Mixed-voltage I/O buffer realized with only thin-oxide devices in the mixed-voltage interface.

the gate terminal of the transistor MN0 is connected to V_{DD}, the maximum drain voltage of the transistor MN1 is about $V_{DD} - V_t$, where V_t is the threshold voltage of nMOS. Hence, the gate-drain voltages and the gate-source voltages of the stacked devices, MN0 and MN1, are limited below V_{DD} even if the input signal on the I/O pad is $2 \times V_{DD}$ in the receive mode. The dynamic n-well bias circuit and the gate-tracking circuit in Fig. 2 are designed to prevent the leakage current path through the parasitic drain-to-well pn-junction diode in the pull-up pMOS device and the leakage current path due to the incorrect conduction of the pull-up pMOS device, respectively. In the transmit mode, the dynamic n-well bias circuit has to keep the floating n-well at V_{DD}. So, the threshold voltage of the pull-up pMOS device is not increased due to the body effect. In the transmit mode, the dynamic gate-tracking circuit should pass the output signal from the upper port of the pre-driver to the gate terminal of the pull-up pMOS device. In the receive mode with a $2 \times V_{DD}$ input signal, the dynamic n-well bias circuit will charge the floating n-well to $2 \times V_{DD}$ to prevent the leakage current from the I/O pad to V_{DD} through the parasitic pn-junction diode. When the input signal at the I/O pad is GND, the dynamic n-well bias circuit will keep the floating n-well at V_{DD}. In the receive mode, the gate voltage of the pull-up pMOS device is controlled at V_{DD} or $2 \times V_{DD}$ according to the input signal on the I/O pad in order to prevent the leakage current path from the I/O pad to the power supply (V_{DD}) through the pull-up pMOS. As shown in Fig. 2, the extra transistors, MN2 and MP1, are added in the input buffer. Transistor MN2 is used to limit the voltage level of the input signal reaching to the gate oxide of the inverter INV. Because the gate terminal of transistor MN2 is connected to V_{DD}, the input node of the inverter INV will rise up to $V_{DD} - V_t$ when the input signal at the I/O pad is $2 \times V_{DD}$ in the tri-state input mode. Then, the transistor MP1 is used to pull up the input node of inverter INV to V_{DD} when the output node of the inverter INV is pulled down to GND. Therefore, the gate-oxide reliability problem occurring in the input buffer can be solved.

Realized with the low-voltage devices, the prior mixed-voltage I/O buffers [15]–[19] only can receive $2 \times V_{DD}$ input signals without suffering the gate-oxide overstress. In this paper, the nMOS-blocking technique is proposed to design the mixed-voltage I/O buffers. By using the proposed nMOS-blocking technique, not only the $2 \times V_{DD}$ input tolerant mixed-voltage I/O buffer but also the $3 \times V_{DD}$ and even $4 \times V_{DD}$ input tolerant mixed-voltage I/O buffers [20] can be achieved. The $2 \times V_{DD}$ and $3 \times V_{DD}$ input tolerant mixed-voltage I/O buffers designed with the proposed nMOS-blocking technique have been successfully verified in a 0.25-μm 2.5-V CMOS process to serve the 2.5/5-V mixed-voltage interface and in a 0.13-μm 1-V CMOS process with Cu interconnects to serve the 1/3-V mixed-voltage interface, respectively.

II. NMOS-Blocking Technique

In an nMOS transistor, if its drain voltage V_d is higher than its gate voltage V_g, the source voltage V_s of this nMOS device will be pulled up to $V_g - V_t$, where V_t is the threshold voltage of the nMOS transistor. For example, when the V_g is controlled at V_{DD} and V_d is at $2 \times V_{DD}$, V_s is only pulled up to $V_{DD} - V_t$. Therefore, the feature of nMOS device can be applied to design the mixed-voltage I/O buffer without the gate-oxide reliability issue and the undesired leakage currents described in Fig. 1.

The design concept of the proposed nMOS-blocking technique for mixed-voltage I/O buffer is shown in Fig. 3. The protection devices in Fig. 3 are used to block from the high-voltage input signal on the I/O pad to stress the input buffer and the output buffer of the mixed-voltage I/O circuit. As the I/O buffer is in the transmit mode, the protection devices in Fig. 3 have to pass the signal from node 1 to the I/O pad. As the I/O buffer is in the receive mode, the protection devices not only limit the high-voltage level of the input signal but also pass the signal information from the I/O pad to node 1. The gate voltages of the protection devices must be well controlled in both the transmit mode and the receive mode. As shown in Fig. 3, the mixed-voltage I/O buffer can receive $(n+1) \times V_{DD}$ input signal without the gate-oxide reliability issue by using n protection devices, where n is an integer.

III. $2 \times V_{DD}$ Input Tolerant Mixed-Voltage I/O Buffer

A. Circuit Implementation

Fig. 4 shows the proposed $2 \times V_{DD}$ input tolerant mixed-voltage I/O buffer by using the nMOS-blocking technique. In Fig. 4, V_{DDH} is as high as $2 \times V_{DD}$, which can be generated by an on-chip charge pump circuit with $1 \times V_{DD}$ devices [21] or other high-voltage generators. As shown in Fig. 4, transistor MN1 is used to protect the conventional I/O buffer from the input high-voltage overstress. The pre-driver can generate signals PU and PD to control the output transistors, MP0 and MN0. The dynamic gate-bias circuit in Fig. 4 is used to control the gate voltage of the transistor MN1. Table I lists the operation of the dynamic gate-bias circuit in the proposed $2 \times V_{DD}$ input tolerant mixed-voltage I/O buffer. When this I/O buffer is in the receive mode, the gate terminal (node 2) of transistor MN1 is biased at V_{DD} by the dynamic gate-bias circuit, whereas transistors MP0 and MN0 are both turned off by the pre-driver. At this moment, if an input signal of logic low (GND) is received from the I/O

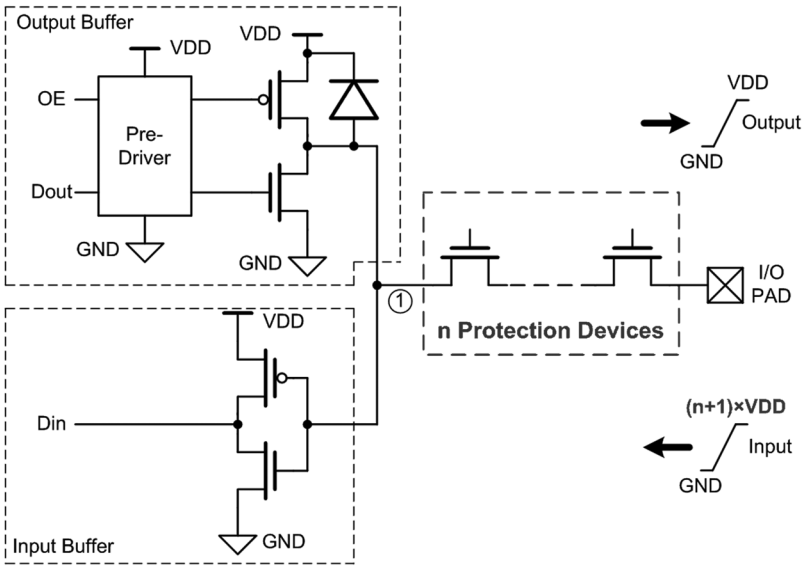

Fig. 3. Proposed design concept of nMOS-blocking technique for mixed-voltage I/O buffer.

TABLE I
OPERATION OF THE DYNAMIC GATE-BIAS CIRCUIT IN THE PROPOSED $2\times V_{DD}$ INPUT TOLERANT MIXED-VOLTAGE I/O BUFFER

Mode	Transmitted Signal	Received Signal	Gate Voltage of MP0 (PU)	Gate Voltage of MN1 (Node 2)
Receive Mode	X	Low (GND)	VDD	VDD
High-Voltage Receive Mode	X	High (2×VDD)	VDD	VDD
Transmit Mode	Low (GND)	X	VDD	VDD
Transmit Mode	High (VDD)	X	GND	VDDH

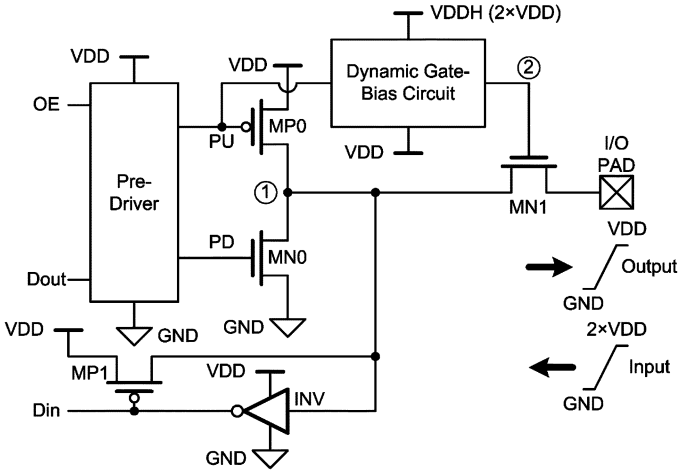

Fig. 4. $2\times V_{DD}$ input tolerant mixed-voltage I/O buffer by using the proposed nMOS-blocking technique.

pad, node 1 is discharged to GND through transistor MN1, and this input signal can be successfully transferred to the node Din of the input buffer. When a logic high ($2\times V_{DD}$) signal is received from the I/O pad, the gate terminal of transistor MN1 is still biased at V_{DD}, so the voltage on node 1 is pulled up to $V_{DD}-V_t$. Because the voltage on node 1 is at $V_{DD}-V_t$, the signal Din is pulled down to GND. A feedback device MP1 is added to restore the voltage level on node 1 to V_{DD}, which avoids the undesired static dc current through the inverter INV in the input buffer. Besides, when the voltage on the I/O pad stays at $2\times V_{DD}$ for a long time, the voltage on node 1 may go up to the voltage determined by the ratio of leakage. The feedback device MP1 is used to solve this issue. In this design, transistors MN1 and MP1 with the inverter INV can convert the $2\times V_{DD}$ input signal to V_{DD} signal successfully. Therefore, transistor MN1 can protect the I/O buffer without suffering high-voltage overstress on the gate oxide.

Fig. 5 depicts the dynamic gate-bias circuit in the proposed $2\times V_{DD}$ input tolerant I/O buffer, where transistors MP2 and MP3 are designed with the cross-coupled structure. If the gate voltage of transistor MP2 (or MP3) is pulled down, this transistor is turned on and pulls up the gate voltage of the other transistor to V_{DDH} to turn it off. For example, if the voltage on node 5 in Fig. 5 is lower than $V_{DDH}-V_t$ and the voltage on node 6 is V_{DDH}, transistor MN2 is turned on to keep the node 5 at V_{DD}. In Fig. 5, capacitors C1 and C2 are used to couple the signals from nodes 3 and 4 to nodes 5 and 6, respectively. The voltages across these capacitors, C1 and C2, are always V_{DD}, because the voltage levels on the top and bottom plates of capacitors C1 and C2 are either V_{DD} and GND or $2\times V_{DD}$ and V_{DD}. With these capacitors, when the voltage level on node 3 is changed from V_{DD} to GND, the voltage on node 5 is pulled down to V_{DD} and then the voltage level on node 6 is pulled up to

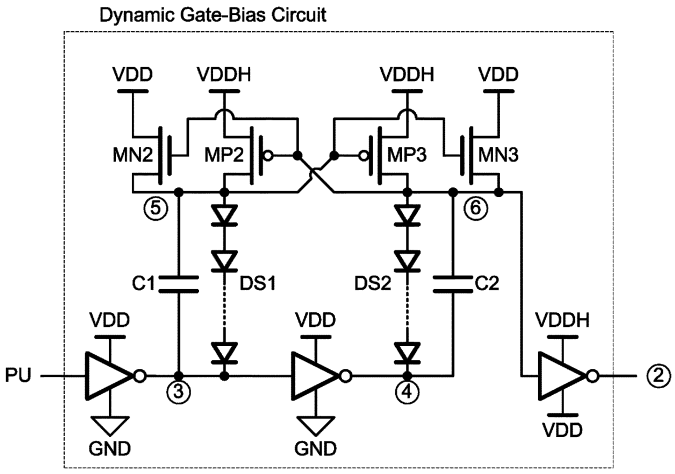

Fig. 5. Dynamic gate-bias circuit in the proposed $2 \times V_{DD}$ input tolerant mixed-voltage I/O buffer.

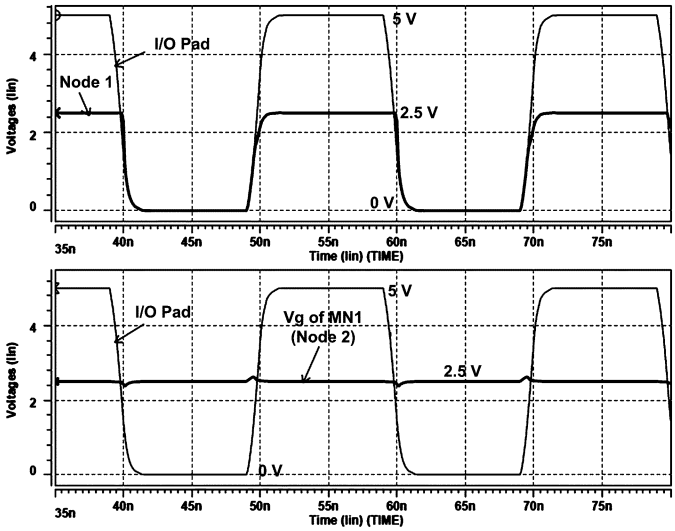

Fig. 6. Simulated waveforms of the proposed $2 \times V_{DD}$ input tolerant mixed-voltage I/O buffer in the receive mode with 5-V input signals.

$2 \times V_{DD}$ by transistor MP3. On the contrary, when the voltage level on node 4 is converted from V_{DD} to GND, that on node 6 is pulled to V_{DD}, and that on node 5 is pulled up to $2 \times V_{DD}$ by transistor MP2.

Initially, the voltages on nodes 3, 4, 5, and 6 in Fig. 5 could be unknown. If the voltages on nodes 5 and 6 are $2 \times V_{DD}$ and V_{DD}, and the voltages on nodes 3 and 4 are GND and V_{DD}, the voltages across capacitors C1 and C2 are $2 \times V_{DD}$ and V_{DD}, respectively, instead of both V_{DD}. In order to overcome this initial problem, the diode strings, DS1 and DS2, are added. The turn-on voltages of the diode strings are designed to a little higher than V_{DD} by using multiple diodes in stacked configuration. In order to prevent the leakage current path to the grounded p-type substrate, the diode-connected MOSFET or polysilicon diode [22] is suggested. With these diode strings, if the voltage on node 3 is at GND and that on node 4 is at V_{DD}, the voltage on node 5 is clamped at the turn-on voltage, which is a little higher than V_{DD}, of the diode string DS1. Therefore, transistor MP3 is turned on to pull up the voltage on node 6 to $2 \times V_{DD}$. Thus, the voltages across capacitors C1 and C2 are both V_{DD}.

In the proposed $2 \times V_{DD}$ input tolerant mixed-voltage I/O buffer, the bulk of the protection device, MN1, can be coupled to GND without the gate-oxide overstress, even if the gate voltage of transistor MN1 may be as high as $2 \times V_{DD}$. The reason is that this protection device, MN1, is always turned on and the voltage across the gate oxide of transistor MN1 is from the gate to the conducting channel, but not from the gate to its bulk. Thus, the gate oxides of all nMOS devices in the dynamic gate-bias circuit are also safe because these nMOS devices are turned on when their gates are pulled up to $2 \times V_{DD}$.

B. Experimental Results

The proposed $2 \times V_{DD}$ input tolerant mixed-voltage I/O buffer has been verified in a 0.25-μm 2.5-V CMOS process to serve 2.5/5-V mixed-voltage interface. Fig. 6 shows the simulated waveforms of the proposed $2 \times V_{DD}$ input tolerant mixed-voltage I/O buffer in the receive mode to receive the input signal of 0-to-5 V. As shown in Fig. 6, the gate voltage

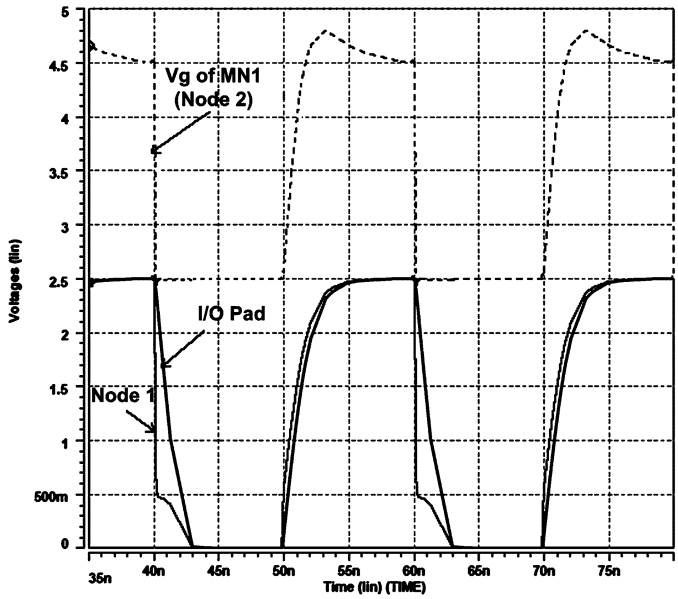

Fig. 7. Simulated waveforms of the proposed $2 \times V_{DD}$ input tolerant mixed-voltage I/O buffer in the transmit mode.

(node 2) of the transistor MN1 is always kept at 2.5 V in the receive mode, and the voltage swing on node 1 is from 0 V to 2.5 V. Fig. 7 shows the simulated waveforms of the proposed $2 \times V_{DD}$ input tolerant mixed-voltage I/O buffer in the transmit mode. When the voltage on node 1 is raised up to 2.5 V, the gate voltage of the transistor MN1 is also raised to $\sim$5 V at the same time to turn on the transistor MN1. Then, the voltage on the I/O pad is pulled up to 2.5 V. When the voltage on node 1 is dropped to 0 V, the gate voltage of the transistor MN1 is kept at 2.5 V to prevent from the high-voltage overstress on the gate oxide of the protection device MN1. The voltage on the I/O pad is therefore dropped to 0 V. With the dynamic gate-bias circuit, the proposed mixed-voltage I/O buffer can successfully transfer signals in full swing to the I/O pad through the protection device MN1.

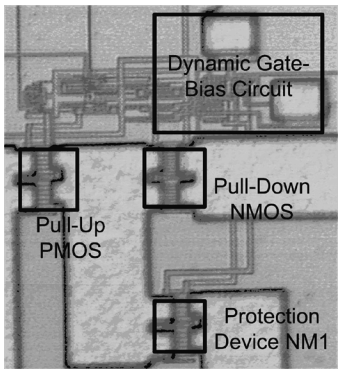

Fig. 8. Chip photograph of the proposed $2 \times V_{DD}$ input tolerant mixed-voltage I/O buffer in a 0.25-μm 2.5-V CMOS process.

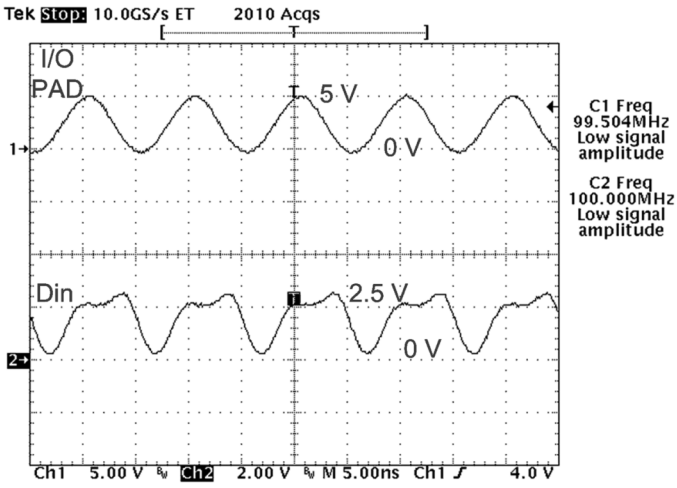

Fig. 9. Measured waveforms on the node Din and I/O pad of the proposed $2 \times V_{DD}$ input tolerant mixed-voltage I/O buffer in the receive mode with 5-V input signals.

Fig. 8 shows the chip photograph of the proposed $2 \times V_{DD}$ input tolerant I/O buffer fabricated in a 0.25-μm 2.5-V CMOS process. Figs. 9 and 10 show the measured voltage waveforms on the node Dout and the I/O pad of the proposed $2 \times V_{DD}$ input tolerant I/O buffer in the receive mode and in the transmit mode, respectively. As shown in Figs. 9 and 10, the proposed $2 \times V_{DD}$ mixed-voltage I/O buffer by using the nMOS-blocking technique can be correctly operated in the 2.5/5-V mixed-voltage interface.

IV. $3 \times V_{DD}$ Input Tolerant Mixed-Voltage I/O Buffer

A. Circuit Implementation

Fig. 11 depicts the proposed $3 \times V_{DD}$ input tolerant mixed-voltage I/O buffer by using the nMOS-blocking technique [20]. V_{DD} is the applied power supply voltage, whereas V_{DDH} ($2 \times V_{DD}$) can be generated by an on-chip charge pump circuit with $1 \times V_{DD}$ devices from V_{DD} [21]. The output voltage of the on-chip charge pump circuit is shared by all mixed-voltage I/O circuits in the same chip. The protection devices, MN1 and MN2, controlled by the dynamic gate-bias circuit are used to avoid the high-voltage overstress on the gate oxide. The detailed operation of the dynamic gate-bias circuit

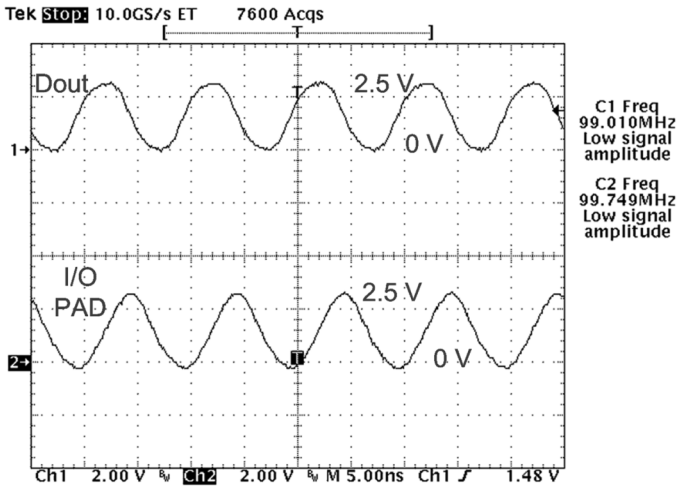

Fig. 10. Measured waveforms on the node Dout and I/O pad of the proposed $2 \times V_{DD}$ input tolerant mixed-voltage I/O buffer in the transmit mode with 2.5-V output signals.

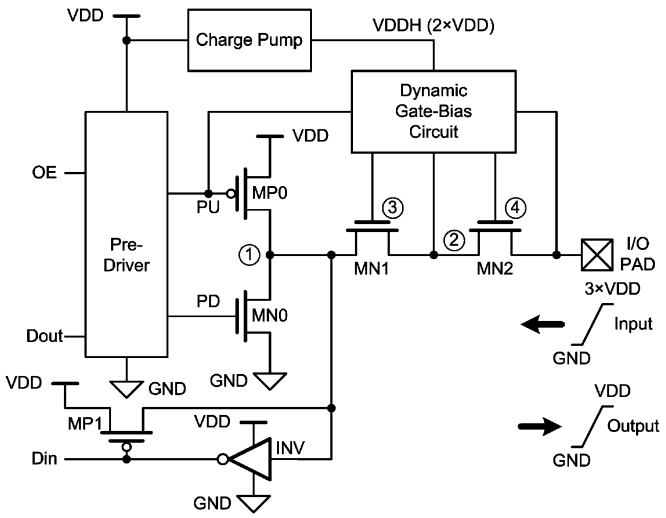

Fig. 11. $3 \times V_{DD}$ input tolerant mixed-voltage I/O buffer by using the proposed nMOS-blocking technique.

is listed in Table II. When this I/O buffer transmits a logic low (GND), the gate voltages of transistors MN1 and MN2 are controlled at V_{DD}, so the logic low can be transmitted from node 1 to the I/O pad. When this I/O buffer transmits a logic high (V_{DD}), the gate voltages of transistors MN1 and MN2 are controlled at V_{DDH}, so the logic high can be transmitted from node 1 to the I/O pad. When this I/O buffer receives a logic low (GND), the gate voltages of transistors MN1 and MN2 are biased at V_{DD}. Thus, the logic low signal can be transmitted to node 1 from the I/O pad. When this I/O buffer receives a logic high ($3 \times V_{DD}$), the gate voltages of transistors MN1 and MN2 are biased at V_{DD} and V_{DDH}, respectively. In the $3 \times V_{DD}$ receive mode, the voltage on node 2 (node 1) is pulled up to $V_{DDH} - V_t$ ($V_{DD} - V_t$), where V_t is the threshold voltage of transistors. Then, the signal Din is pulled down to GND to turn on transistor MP1. Finally, the voltage on node 1 is fully restored to V_{DD}, so the inverter INV has no dc leakage current. In this $3 \times V_{DD}$ input tolerant mixed-voltage I/O buffer, the

TABLE II
OPERATION OF THE DYNAMIC GATE-BIAS CIRCUIT IN THE PROPOSED $3\times V_{DD}$ INPUT TOLERANT MIXED-VOLTAGE I/O BUFFER

Mode	Transmitted Signal	Received Signal	Gate Voltage of MN1 (Node 3)	Gate Voltage of MN2 (Node 4)
Receive Mode	X	Low (GND)	VDD	VDD
High-Voltage Receive Mode	X	High (3×VDD)	VDD	VDDH
Transmit Mode	Low (GND)	X	VDD	VDD
Transmit Mode	High (VDD)	X	VDDH	VDDH

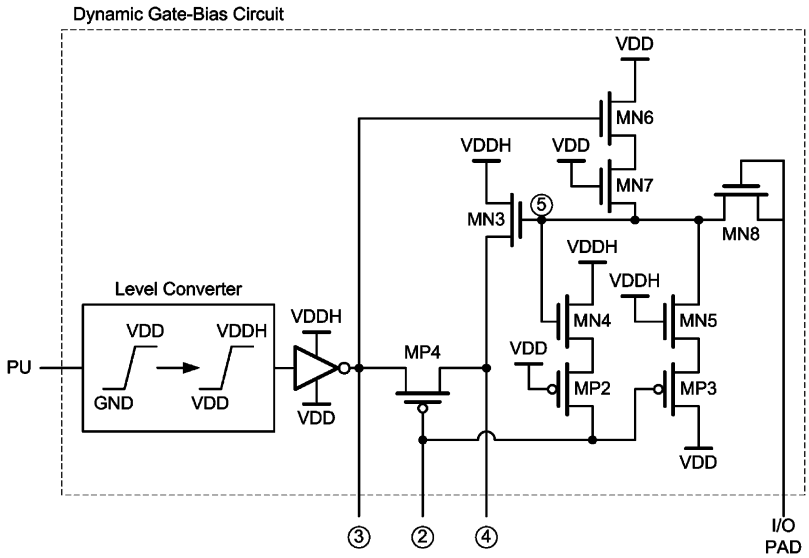

Fig. 12. Dynamic gate-bias circuit in the proposed $3\times V_{DD}$ input tolerant mixed-voltage I/O buffer.

gate-drain, gate-source, and drain-source voltages of every transistor do not exceed V_{DD}. Thus, the proposed mixed-voltage I/O buffer with $1\times V_{DD}$ devices in Fig. 11 can tolerate $3\times V_{DD}$ input signals without the gate-oxide reliability issue.

According to Table II, the dynamic gate-bias circuit in the proposed $3\times V_{DD}$ input tolerant mixed-voltage I/O buffer can be designed. Fig. 12 shows the dynamic gate-bias circuit in the proposed $3\times V_{DD}$ input tolerant mixed-voltage I/O buffer. In both transmit and receive modes, the signal PU has an inverting logic level of node 3. The voltage swing of signal PU is from GND to V_{DD}, but that of node 3 is from V_{DD} to V_{DDH}. Thus, a GND/V_{DD}-to-V_{DD}/V_{DDH} level converter followed by an inverter can be used to generate the signal level of node 3 to control the gate of the transistor MN1. In the transmit mode, node 3 has the same signal level of node 4. Thus, nodes 3 and 4 are connected by the transistor MP4, whose gate is connected to node 2 to avoid the gate-oxide overstress. The voltage on node 5 must be biased at V_{DD} and V_{DDH} alternately in the transmit mode due to the gate-oxide reliability issue of the transistor MN3. When the I/O buffer transmits a logic low, the gate voltages of transistors MN1 and MN2 are kept at V_{DD}, and transistor MP3 is turned on to keep the voltage level on node 5 at V_{DD}. When the I/O buffer transmits a logic high (GND), the gate voltages of transistors MN1 and MN2 are kept at V_{DDH}, and transistor MN6 is turned on to keep the voltage level on node 5 at V_{DD}. The gate-drain and gate-source voltages of transistor MN3 are always lower than V_{DD} in the transmit mode, so there is no gate-oxide overstress issue on transistor MN3.

The gate voltage (node 3) of transistor MN1 is always kept at V_{DD} in the receive mode. The gate voltage (node 4) of transistor MN2 is controlled at V_{DD} or V_{DDH} by the input signal on the I/O pad. When the I/O buffer receives a logic high ($3\times V_{DD}$), the voltage on node 5 is pulled up to the voltage level of $3\times V_{DD}-V_t$ through the diode-connected transistor MN8. At this moment, transistors MN3 and MN4 are turned on to pull the voltages on nodes 4 and 2 both up to V_{DDH}. When the I/O buffer receives a logic low (GND), transistor MP4 is turned on to pull the voltage on node 4 down to V_{DD} because the voltage on node 3 is V_{DD}. At this moment, transistor MP3 is turned on to pull the voltage on node 5 down to V_{DD} to prevent the gate-oxide overstress on transistor MN3. In addition, transistors MP2, MN5, and MN7 can protect transistors MN4, MP3, and MN6 against the gate-oxide overstress.

B. Experimental Results

The proposed $3\times V_{DD}$ input tolerant mixed-voltage I/O buffer has been verified in a 0.13-μm 1-V CMOS process with Cu interconnects to serve 1/3-V mixed-voltage interface. Fig. 13 shows the simulated voltage waveforms of the proposed $3\times V_{DD}$ input tolerant mixed-voltage I/O buffer in the receive mode to receive 3-V input signals. The simulated waveforms

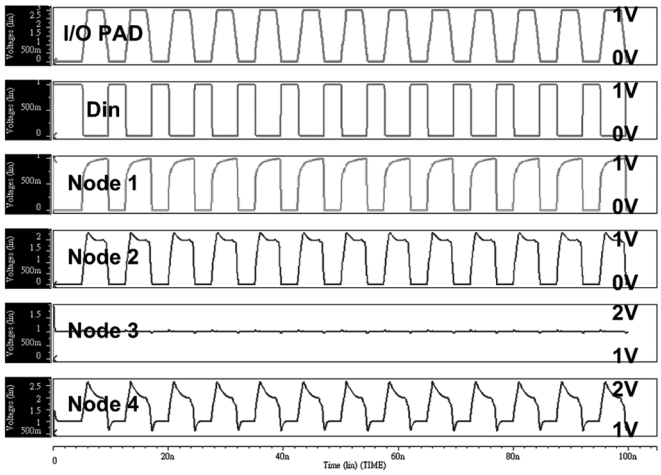

Fig. 13. Simulated waveforms of the proposed $3 \times V_{DD}$ input tolerant mixed-voltage I/O buffer in the receive mode to receive 133-MHz $3 \times V_{DD}$ (3-V) input signals. The waveforms are shown to observe the voltages at the nodes of I/O pad, Din, node 1, node 2, node 3, and node 4 in Fig. 12.

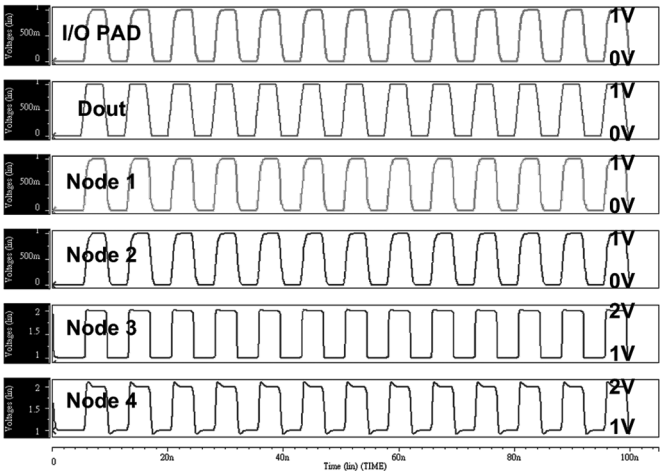

Fig. 14. Simulated waveforms of the proposed $3 \times V_{DD}$ input tolerant mixed-voltage I/O buffer in the transmit mode to drive 133-MHz $3 \times V_{DD}$ (3-V) output signals. The waveforms are shown to observe the voltages at the nodes of I/O pad, Din, node 1, node 2, node 3, and node 4 in Fig. 12.

in Fig. 13 are all consistent to our design expectation. Although the transient peak voltage on node 4 could be larger than 2 V due to the parasitic gate-drain capacitance (C_{gd}) of transistor MN2, the gate-drain and gate-source voltages of transistor MN2 are still kept lower than 1 V. Fig. 14 shows the simulated voltage waveforms of the proposed $3 \times V_{DD}$ input tolerant mixed-voltage I/O buffer in the transmit mode to drive 1-V output signals. The simulated waveforms in Fig. 14 are also consistent to our design expectation. The gate-drain and gate-source voltages of all devices in the proposed $3 \times V_{DD}$ mixed-voltage I/O buffer do not exceed 1 V, which has been confirmed in SPICE simulation.

Fig. 15 shows the layout of the proposed $3 \times V_{DD}$ input tolerant I/O buffer fabricated in a 0.13-μm 1-V CMOS process with Cu interconnects. The active area of the proposed $3 \times V_{DD}$ input tolerant I/O buffer is around 70×150 μm^2. Figs. 16 and 17 show the measured voltage waveforms of the proposed $3 \times V_{DD}$ input tolerant I/O buffer in the receive mode and in the

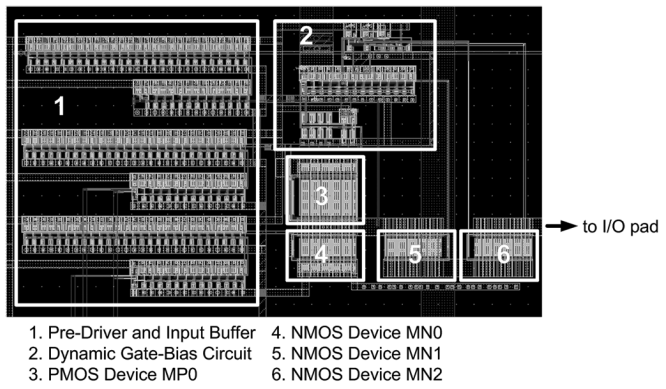

Fig. 15. Layout of the proposed $3 \times V_{DD}$ input tolerant mixed-voltage I/O buffer in a 0.13-μm 1-V CMOS process with Cu interconnects.

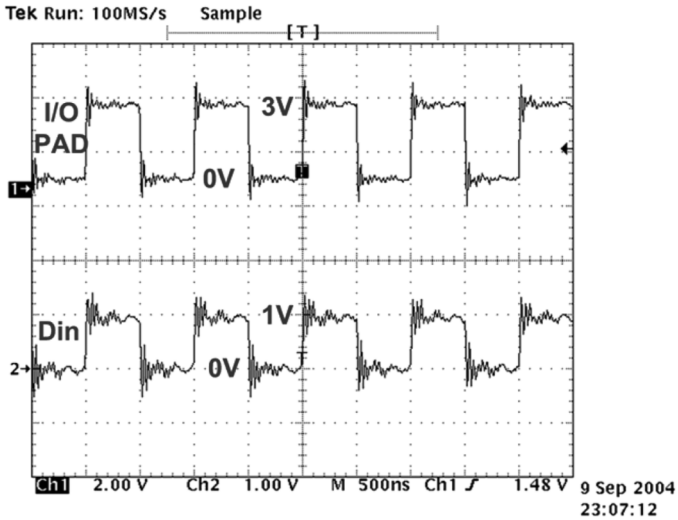

Fig. 16. Measured voltage waveforms of the proposed $3 \times V_{DD}$ input-tolerant mixed-voltage I/O buffer in the receive mode to successfully receive $3 \times V_{DD}$ (3-V) input signals.

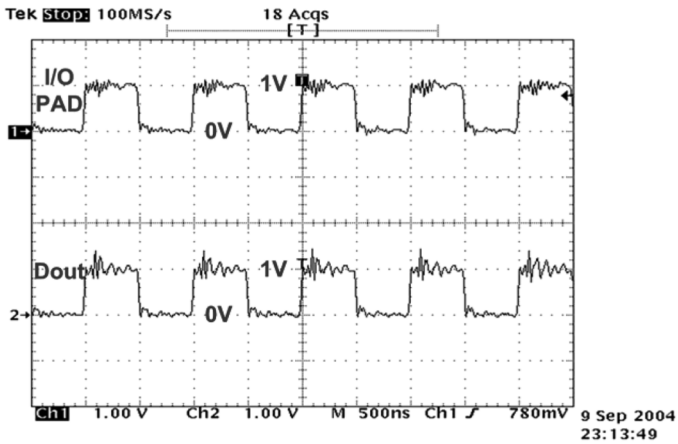

Fig. 17. Measured voltage waveforms of the proposed $3 \times V_{DD}$ input-tolerant mixed-voltage I/O buffer in the transmit mode to drive $1 \times V_{DD}$ (1-V) output signals.

transmit mode, respectively. As shown in Fig. 16, the proposed $3 \times V_{DD}$ input tolerant I/O buffer can successfully receive 3-V input signals in the receive mode. As shown in Fig. 17, the

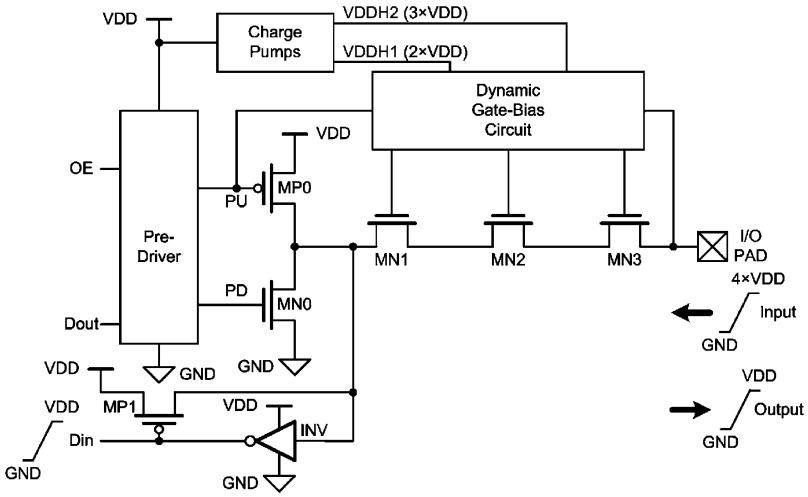

Fig. 18. $4 \times V_{DD}$ input tolerant mixed-voltage I/O buffer by using the proposed nMOS-blocking technique.

proposed $3 \times V_{DD}$ input tolerant I/O buffer can successfully drive 1-V output signals in the transmit mode.

V. Discussion

A. Limitation of the nMOS-Blocking Technique

Ideally, the proposed nMOS-blocking technique can be used to design the $(n+1) \times V_{DD}$ input tolerant mixed-voltage I/O buffer when n protection devices are applied, as shown in Fig. 3. Fig. 18 shows the design example of the $4 \times V_{DD}$ input tolerant mixed-voltage I/O buffer by using the proposed nMOS-blocking technique. Three protection devices, MN1, MN2, and MN3, are applied in Fig. 18, so this mixed-voltage I/O buffer can receive $4 \times V_{DD}$ input signals. Thus, the dynamic gate-bias circuit requires the V_{DDH1} ($2 \times V_{DD}$) and V_{DDH2} ($3 \times V_{DD}$) voltage levels to control the gates of the protection devices, MN1, MN2, and MN3. In Fig. 18, the charge pump circuits realized with $1 \times V_{DD}$ devices can also generate the V_{DDH1} and V_{DDH2} voltage levels.

Actually, the nMOS-blocking technique will be limited by the pn-junction breakdown voltage in the CMOS process. If the input voltage is larger than the pn-junction breakdown voltage, the parasitic pn-junction diode of the protection device which is closed to the I/O pad will break down. For example, the pn-junction breakdown voltage is around 8–9 V in the 0.13-μm 1-V CMOS process. Thus, the $8 \times V_{DD}$ input tolerant mixed-voltage I/O buffer could be designed in the 0.13-μm 1-V CMOS process by using the proposed nMOS-blocking technique.

B. Gate-Oxide Breakdown

Gate-oxide breakdown is a time-dependent issue [23], [24]. The time period during the voltage overstress on the gate oxide is accumulated to induce the oxide breakdown. Hence, the DC stress is more harmful to the gate oxide than the short AC stress (transient stress). Most of the I/O circuits in mixed-voltage applications only focus on the DC stress because the DC stress will damage the gate oxide shortly [15]–[19]. In order to solve the AC stress, the precise resistors and (or) capacitors with special bias circuit are required to detect the transient voltages and then to bias the transistors [25], [26]. However, these resistors and capacitors occupy large silicon area. Besides, these circuits [26] may consume DC current because of using the resistors and capacitors as the bias circuit.

In the mixed-voltage I/O buffers by using the proposed nMOS-blocking technique, the gate-drain and gate-source voltages of devices do not exceed V_{DD} in both receive and transmit modes. Thus, the proposed mixed-voltage I/O buffers do not have the DC gate-oxide reliability issue. Due to the parasitic resistance, inductance, and capacitances, the gate-source and gate-drain voltage may exceed V_{DD} when the input or output signals have transitions. For example, as shown in Fig. 6, the voltage difference between node 2 and I/O pad is a little higher than 2.5 V, when the I/O pad has a low-to-high (0-to-5 V) transition. However, the AC gate-oxide stress is less serious than the DC stress.

C. Hot-Carrier Degradation

The hot-carrier degradation occurs when the drain-source voltage of transistor operated in saturation mode is larger than the normal operating voltage (V_{DD}). The hot-carrier degradation is also a time-dependent issue [9]. In both receive and transmit modes, the drain-source voltages of transistor in the proposed mixed-voltage I/O buffers do not exceed V_{DD}. In the proposed mixed-voltage I/O buffers, the hot-carrier degradation may occurs only during the transition when the proposed mixed-voltage I/O buffers receive high-voltage input signals and then transmit the GND output signals. To reduce this hot-carrier impact, the devices which suffer the hot-carrier issue in the proposed mixed-voltage circuits should be drawn with longer channel width. In [25], the special bias technique can also be used to prevent the hot-carrier degradation.

D. Speed Degradation of the nMOS-Blocking Technique

The proposed nMOS-blocking technique uses the nMOS protection devices to block from high-voltage input signals on the I/O pad. Thus, the mixed-voltage I/O buffer designed with this nMOS-blocking technique can be simply seen as a traditional tri-state I/O buffer cascaded with a resistor (R), as shown in Fig. 19. This resistor represents the equivalent resistance of the

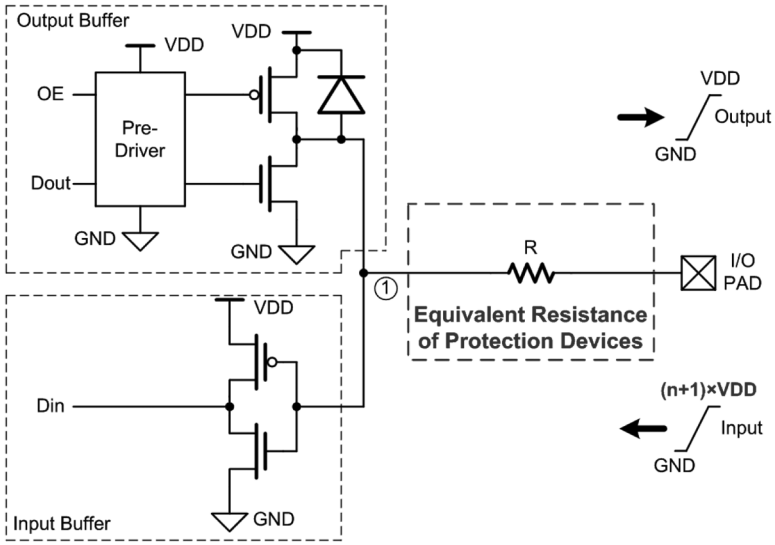

Fig. 19. Equivalent circuit of the mixed-voltage I/O buffer designed with the proposed nMOS-blocking technique.

protection devices. If the equivalent resistance of the protection devices is large, the speed performance will be degraded. Thus, the dimensions of the protection devices must be designed large enough to minimize the equivalent resistance. However, the large dimension device has large drain (source) capacitance, so that the parasitic capacitance on node 1 in Fig. 19 is also somewhat increased to degrade the speed performance. Thus, the dimensions of the protection devices should be optimized according to the given CMOS process.

E. Advantages of the nMOS-Blocking Technique

Generally, the traditional mixed-voltage I/O buffers can only receive $2\times V_{DD}$ input signal without the gate-oxide reliability issue [15]–[19]. However, the proposed nMOS-blocking technique can be extended to design not only the $2\times V_{DD}$ but also $3\times V_{DD}$ and even $4\times V_{DD}$ input tolerant mixed-voltage I/O buffers. Besides, the dynamic n-well bias technique is usually applied in the traditional mixed-voltage I/O buffers [15]–[19], where the voltage on the n-well is not fixed. The latch-up guard rings must be well surrounded when the voltage on the n-well is changed. Because the voltage of the n-well in the proposed mixed-voltage I/O buffers by using the nMOS-blocking technique is fixed, there is no transient latchup problem in the proposed mixed-voltage I/O circuits.

VI. Conclusion

The nMOS-blocking technique has been proposed to design the mixed-voltage I/O buffer in low-voltage CMOS processes. By using the proposed nMOS-blocking technique, the mixed-voltage I/O buffer realized only with $1\times V_{DD}$ devices can receive $2\times V_{DD}$, $3\times V_{DD}$, and even $4\times V_{DD}$ input signals without the gate-oxide reliability issue. The $2\times V_{DD}$ and $3\times V_{DD}$ input tolerant mixed-voltage I/O buffer by using the nMOS-blocking technique have been successfully verified in a 0.25-μm 2.5-V CMOS process to serve 2.5/5-V mixed-voltage interface and in a 0.13-μm 1-V CMOS process with Cu interconnects to serve 1/3-V mixed-voltage interface, respectively. The proposed nMOS-blocking technique can be extended to design the $4\times V_{DD}$, $5\times V_{DD}$, and even $6\times V_{DD}$ input tolerant mixed-voltage I/O buffers. The limitation on the proposed nMOS-blocking technique is the pn-junction breakdown voltage of the given CMOS process.

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