The Impact of Deep Ni Salicidation and NH_3 Plasma Treatment on Nano-SOI FinFETs

Hsin-Chiang You, Po-Yi Kuo, Fu-Hsiang Ko, Tien-Sheng Chao, and Tan-Fu Lei

***Abstract*—In this letter, 50-nm gate-length nano-silicon-on-insulator FinFETs with deep Ni salicidation and NH_3 plasma treatment are fabricated. It is found that device performances, including subthreshold slope (SS) drain-induced barrier lowering (DIBL) and OFF-state leakage current, can be greatly improved by using deep Ni salicidation process compared to no Ni salicidation process. The deep Ni-salicided devices effectively suppress the floating-body effect and parasitic bipolar junction transistor action. In addition, the effect of NH_3 plasma on the deep Ni-salicided devices is discussed. Experimental results reveal that the devices under a new state-of-the-art NH_3 plasma process can achieve better performance such as an SS of 66 mV/dec and a DIBL of 0.03 V.**

***Index Terms*—Deep Ni salicidation, drain-induced barrier lowering (DIBL), floating-body effect, NH_3 plasma, subthreshold slope (SS).**

I. Introduction

RECENTLY, the industries focus on the issue of scaling planar CMOS. However, scaling planar CMOS to short gate length will face many problems, including electrostatics, excessive leakages, and mobility degradation. Nonplanar CMOS MOSFETs exhibit potential advantages in packaging density, carrier transport, and device scalability [1]. Silicon-on-insulator (SOI) FinFET technology has a couple of advantages, such as the reduction of parasitic capacitances, the feasibility of diffusion resistors and capacitors free of junction effects, and the better device isolation leading to absence of latch up, substrate coupling, and good gate control ability. However, the floating-body effect is a main issue of the SOI MOSFET devices. This effect will cause the drain current "kink," abnormal subthreshold slope (SS), and low breakdown voltage [2], [3]. The metal salicidation has been studied as an approach to suppressing the issue of floating-body effect and drain-induced barrier lowering (DIBL) [4], [5] and reducing the parasitic source/drain (S/D) resistances in the thin-film SOI devices.

Plasma treatment has long been used in the thin-film transistor (TFT) devices. The suitable plasma treatment can improve the electrical characteristics of the TFT devices due to the repair of the device's defects. However, to the best of our knowledge, plasma treatment has yet to be proposed for the nano-SOI FinFET fabrication. In this letter, we describe the fabrication of 50-nm gate-length nano-SOI FinFETs prepared through the deep Ni salicidation and NH_3 plasma treatment. This is the first time to apply NH_3 plasma treatment on thin-film SOI devices. The NH_3 plasma treatment is expected to repair the process-induced defects for the thin-film SOI devices.

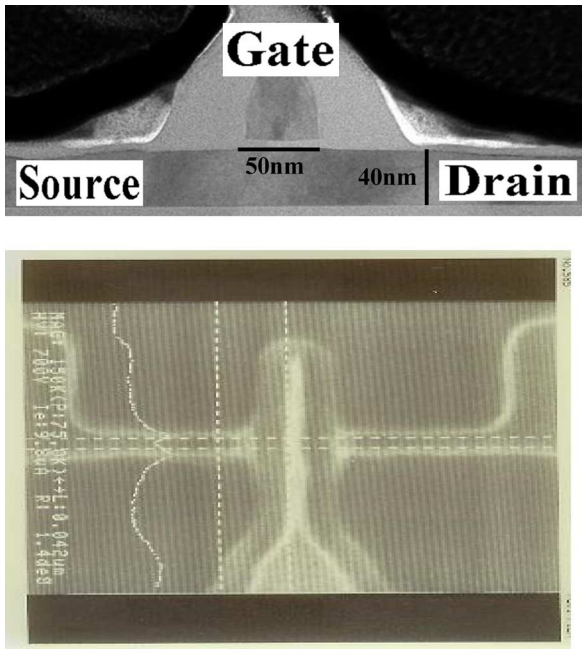

Fig. 1. TEM and top view SEM for the nano-SOI FinFETs. The gate length is 50 nm, and the Si channel thickness is 40 nm. (Color version available online at http://ieeexplore.ieee.org.)

II. Experiment

The schematic device structure for the transmission electron microscopy (TEM) and the top view scanning electron micrograph (SEM) of the nano-SOI FinFETs are shown in Fig. 1. The channel length, thickness, and fin width of nano-SOI FinFETs is about 50, 40, and 42 nm, respectively. The channel width of the device is estimated to be about 122 nm (fin width $+ 2 \times$ fin height $= 42$ nm $+ 2 \times 40$ nm).

The schematic diagram of nano-SOI FinFETs is illustrated in Fig. 2. The nano-SOI FinFETs were fabricated by the following process steps: First, the active region was patterned, and a 4-nm thermal gate oxide layer was grown by a furnace. Subsequently, a 100-nm *in situ* n^+ phosphorus-doped amorphous silicon (a-Si) gate layer was deposited by low-pressure chemical vapor deposition (LPCVD). After gate patterning, the remaining

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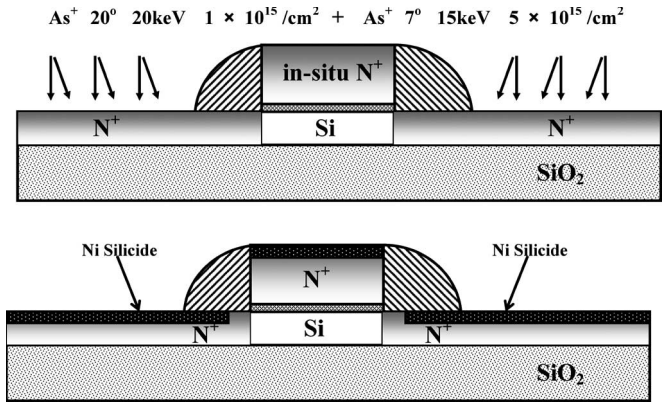

Fig. 2. Device structures for the nano-SOI FinFETs. The gate length is 50 nm, and the Si channel thickness is 40 nm.

oxide on S/D regions was removed by diluted hydrofluoric acid (HF), and then, a 150-nm tetraethoxysilane (TEOS) oxide sidewall spacer was formed by deposition and etching. A self-aligned implantation was used to perform the n^+ S/D extension with the As^+ dosage of 1×10^{15} cm^{-2}, energy of 20 keV, and tilt of 20°. Similarly, a self-aligned implantation was subsequently used to perform the n^+ S/D with the As^+ dosage of 5×10^{15} cm^{-2}, energy of 15 keV, and tilt of 7°. Dopants were activated by rapid thermal annealing (RTA) at 950 °C for 15 s. Prior to sputtering deposition of 10-nm Ni film, a dilute HF dip step was used to clean the sample. Then, Ni salicidation was carried out by one-step RTA at 450 °C for 60 s in the N_2 atmosphere. Unreacted Ni was removed by the mixture of H_2SO_4 and H_2O_2 solutions. After contact and metallization processes, NH_3 plasma procedures were implemented, as well as the subsequent sintering at 400 °C for 30 min. Conventional devices without Ni salicidation and NH_3 plasma were also fabricated to serve as control ones.

III. Results and Discussion

The transistor characteristics of the control SOI devices (no Ni salicidation) with width/length $(W/L) = 122$ nm/50 nm (SOI FinFETs) and $W/L = 180$ nm/50 nm (SOI MOSFETs) are displayed in Fig. 3. Fig. 3(a) indicates an SS of 379 mV/dec and a DIBL of 0.397 V for SOI FinFETs, whereas Fig. 3(b) suggests an SS of 267 mV/dec and a DIBL of 0.24 V for SOI MOSFETs. The poor device performance for the SOI MOSFETs is attributed to the issue of very short gate length (50 nm). In addition, the subthreshold swing is relatively large due to the short-channel effect and the poor gate controlling ability. On the contrary, the SOI FinFETs exhibit good gate controlling ability and improved subthreshold swing [6]. We think that these dopants were activated by RTA at 950 °C for 15 s, but, the defects of S/D are not fully eliminated. The presence of S/D defects will cause the high leakage currents for the devices.

The characteristic of the deep Ni-salicided SOI FinFETs with $W/L = 122$ nm/50 nm is illustrated in Fig. 4. This figure indicates that the deep Ni-salicided SOI FinFETs have smaller SS (i.e., 112 mV/dec) and less DIBL (i.e., 0.11 V) in

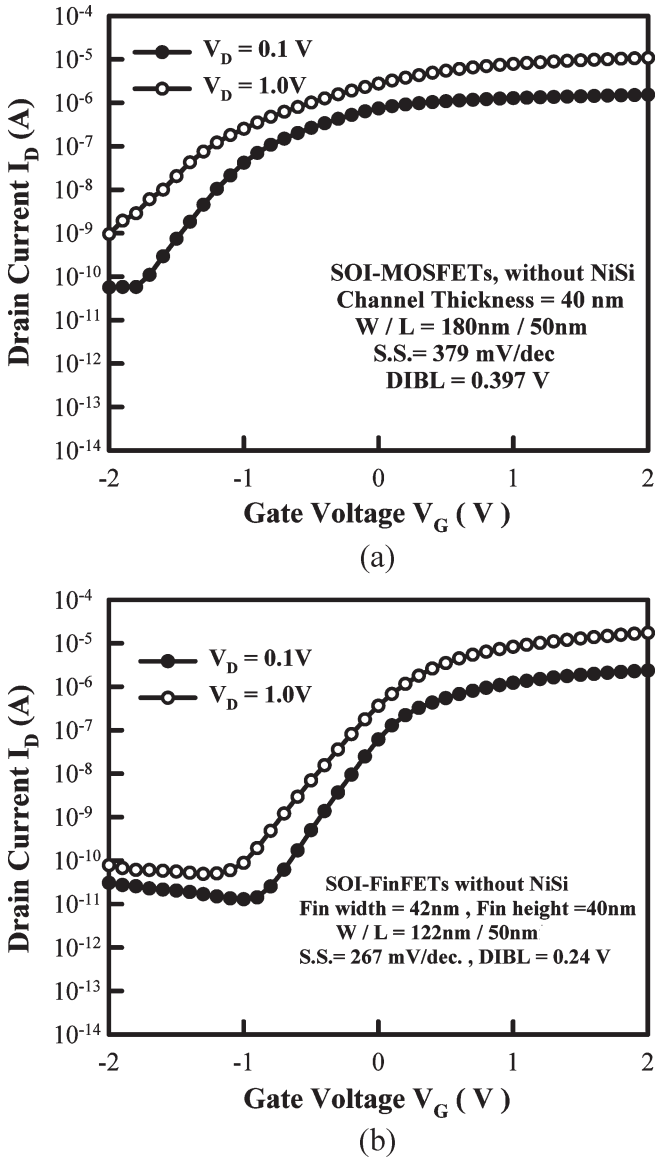

Fig. 3. Transistor characteristic for the control SOI devices (no Ni salicidation) with $W/L = 122$ nm/50 nm (SOI FinFETs) and $W/L = 180$ nm/50 nm (SOI MOSFETs).

comparison with no Ni-salicided SOI devices. Fig. 4 suggests the improvement of OFF-state leakage currents observed in deep Ni-salicided SOI FinFETs. The DIBL in the same device is defined by the $V_{\rm TH}$ shift between two drain voltages. The $V_{\rm TH}$ shift is caused by the DIBL effect. The reduced $V_{\rm TH}$ shift strongly supports that the bipolar junction transistor (BJT) effect was significantly suppressed in the deep Ni-salicided SOI FinFETs. Similar suppression of the floating-body effect was reported for deep silicidation of partially depleted SOI devices, where the thick silicide layer worked as a sink for holes [4], [5]. We demonstrate that Ni salicidation is highly effective in suppressing floating-body effects. Besides, the Ni salicidation can reduce parasitic S/D resistances in the nano-SOI FinFETs. We think that the improved SS is due to the reduced parasitic S/D resistances in the nano-SOI FinFETs.

Fig. 5 displays the transistor characteristic of the deep Ni-salicided SOI FinFETs after state-of-the-art NH_3 plasma

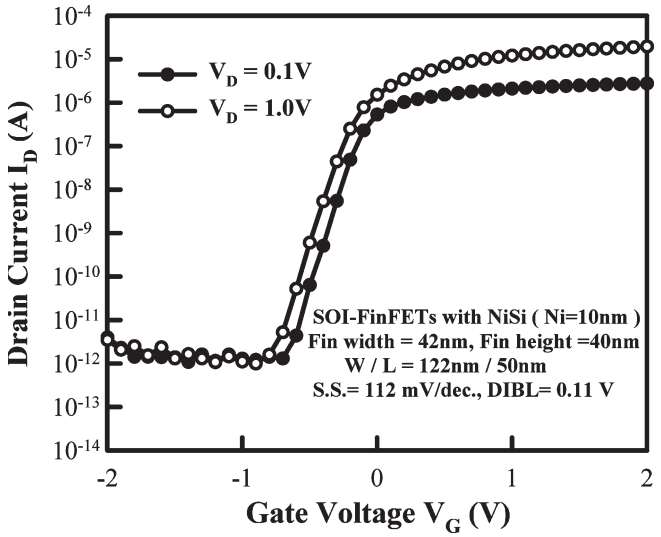

Fig. 4. Transistor characteristic for the deep Ni-salicided SOI FinFETs with $W/L = 122$ nm/50 nm and without plasma treatment.

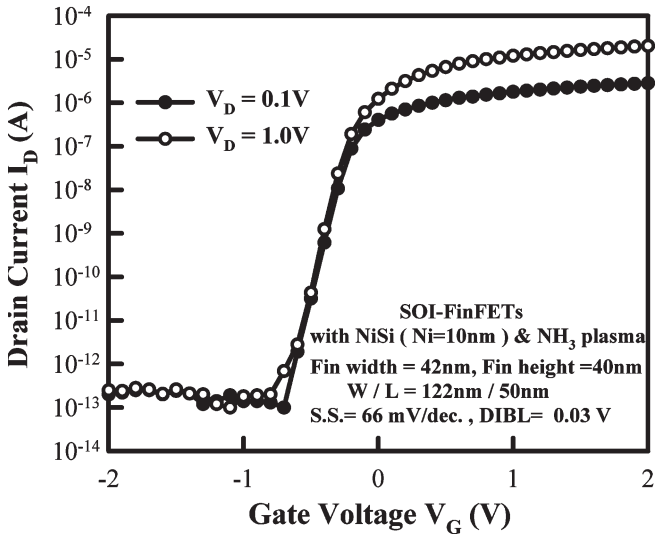

Fig. 5. Transistor characteristic for the deep Ni-salicided SOI FinFETs after state-of-the-art NH_3 plasma treatment with $W/L = 122$ nm/50 nm.

treatment with $W/L = 122$ nm/50 nm. The SS and DIBL of deep Ni-salicided SOI FinFETs after NH_3 plasma treatment are 66 mV/dec and 0.03 V, respectively. We note, after suitable NH_3 plasma treatment, that the improvement of OFF-state leakage current is also observed for the deep Ni-salicided SOI FinFETs. The SS, DIBL, and OFF-state leakage current for the deep Ni-salicided SOI FinFETs with NH_3 plasma treatment are better than the deep Ni-salicided SOI FinFETs without NH_3 plasma treatment. The NH_3 plasma treatment exhibits high defect passivation ability for deep Ni-salicided SOI FinFETs. We believe that this improvement is due to the generation of H atoms in NH_3 plasma, which can passivate the process-induced defects for thin-film SOI devices [7], [8]. We can see from Fig. 5 that the defects of S/D junction (leakage currents) and Si/SiO_2 interface (SS) can be passivated by NH_3 plasma. However, the DIBL also can be improved by the NH_3 plasma because the true device will be affected by the defects from S/D junction, channel, and Si/SiO_2 interface. In this letter, we think that the improvement of DIBL is due to the passivation of deep Ni salicidation process-induced defects from the S/D junction.

IV. Conclusion

In this letter, we have fabricated 50-nm gate-length nano-SOI FinFETs with deep Ni salicidation and NH_3 plasma treatment. From the measured transistor characteristics, the SOI FinFETs are performed better than the long width device. We also discuss the effect of Ni salicidation and state-of-the-art NH_3 plasma treatment on the nano-SOI FinFETs. The deep Ni-salicided SOI FinFETs after NH_3 plasma treatment can achieve high performances such as an of SS $= 66$ mV/dec and a DIBL $= 0.03$ V. Floating-body effect and process-induced defects can be improved by deep Ni salicidation and NH_3 plasma treatment for the nano-SOI FinFETs. We believe that these key technologies are suitable and compatible for future nano-device manufacturing.

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