Load Current Adaptive Control of a Monolithic CMOS DC/DC Converter for Dynamic Power Management

Wei-Chi Su and Ying-Yu Tzou, *Member, IEEE*

Power Electronics Systems & Chips Lab.,
Advance Power Electronics Center,
Department of Electrical and Control Engineering,
National Chiao Tung University, Taiwan.

***Abstract* - This paper presents the design of a monolithic current-mode CMOS DC/DC converter with integrated power switches and an on-chip passive adaptive controller with the sensed average inductor current. The sensed switched current, combined with the integration of inductor voltage, and a voltage-controlled floating resistor, can be used for the adaptive control of a CMOS DC/DC converter. The nonlinear carrier control can adjust carrier according to input voltage to reduce the input disturbance. The proposed control scheme has been design and simulation verified based on the TSMC 0.35μm technology. The designed CMOS DC/DC switching regulator is based on a rated output current of 500mA with an adjustable output voltage from 1.0V to 1.8V. Simulation results shows the proposed adaptive control scheme can achieve a fast dynamic power on transient response as well as a robust voltage regulation against large loading current variation.**

***Index Terms* - CMOS DC/DC converters, synchronous buck regulator, load current adaptive control, nonlinear carrier, fast dynamic response, dynamic power management.**

I. Introduction

Applications of system-on-a-chip (SOC) can be broadly classified according to their high-performance (HP) or low-power (LP) characteristics. Advanced microprocessors and high-end graphic processors are examples of high performance applications, while portable wireless applications such as PDAs, digital cameras, and bluetooth devices are examples of low-power SOCs. In either application, the power supplying to the SOC systems needs to satisfy the dynamic power management, fast dynamic response, and low power consumption [1]-[3].

To accommodate the diverse power requirements of a portable device, we need to design dedicated dc-dc converters for target point-of-load (POL) applications. CMOS based synchronous buck regulators are widely employed in portable information appliances. Low power consumption with low standby power, high power density with integrated magnetic components, high efficiency with large input voltage range, fast power on response time, robust voltage regulation without external components, and voltage scaling capability, etc., are important design issues for integrated dc-dc converters [4]-[6]. In order to achieve robust control performance, current-mode control schemes are usually employed with the control loops. Among various realization schemes, the peak current mode (PCM) control with negative slope compensation is probably the most frequently adopted scheme in realization of PWM control ICs [7]. The PCM control with negative slope compensation can eliminate subharmonic oscillations within the inner current loop when operating duties are high [8]. The sensing scheme for the monolithic CMOS DC/DC needs to be realized with high bandwidth as well as low power consumption. An on-chip current sensing scheme without using a series connected resistor is proposed in [9], however, this scheme need sophisticated design of circuit parameters to match the high temperature sensitivity of on-chip CMOS buffer circuits.

This work was supported by the National Science Council, Taipei, Taiwan, R.O.C. Project no. NSC 94-2213-E-009-146

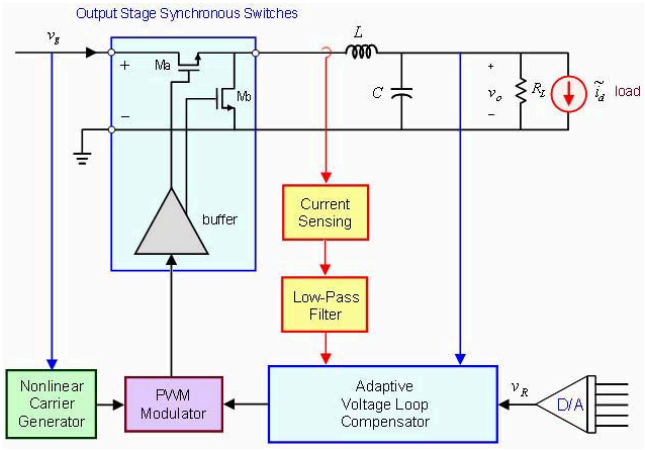


Fig. 1. Proposed analog adaptive voltage loop control scheme.

To simplify the design of control loops of a CMOS DC/DC converter, various voltage-mode control schemes, such as second-order slope compensation [10], observer-based sensorless current mode control [11], end-point prediction [12], adaptive parameter scheduling [13], and digital control [14], have been developed to provide robust performance as well as simple circuit realization. However, these control schemes still can not meet the requirement of low-cost design with robust performance. In this paper, a simple load-current adaptive gain control scheme with a feedforward nonlinear carrier control has been proposed to achieve simple and robust control of a monolithic DC/DC converter without current mode control.

A monolithic current-mode CMOS DC/DC converter with integrated power switches and a novel on-chip adaptive controller is presented in this paper. The proposed analog adaptive voltage loop control scheme is shown in Fig. 1. With the sensed switch current, combined with the

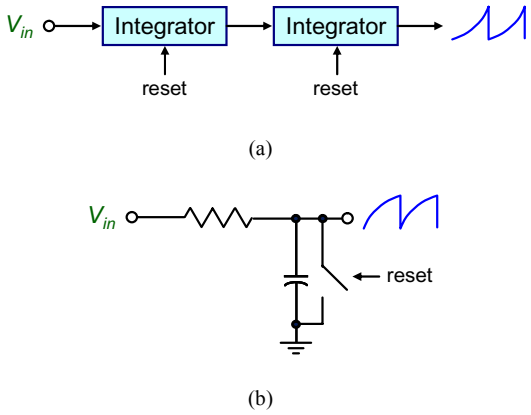


Fig. 2. The ways to generate nonlinear carrier.

integration of inductor voltage, and a voltage-controlled floating resistor, an analog adaptive control scheme is proposed for the regulation of a CMOS DC/DC converter. The inductor current is sensed by using an on-chip sensing circuit in measuring the current of the complementary switches, however, because this measured current is used for the tuning of the control gain for the voltage mode controller, it can be much slower compared with the current mode sensing circuit and furthermore, the requirement on its accuracy much less stringent. Therefore, simple current sensing scheme can be employed in design of the on-chip current sensing circuit.

The designed CMOS DC/DC converter has been verified by using a system-level simulation software tool PSIM and also by a device-level simulation tool HSPICE based on the TMSC 0.35μm technology. Simulation results shows the proposed adaptive control scheme can achieve a fast dynamic power on transient response as well as a robust voltage regulation against large load current variations.

II. Analog Adaptive Controller

A. Feedforward Nonlinear Carrier Control

In general, a fixed frequency tooth carrier is used in pulse-width generator to generate driving signal for power stage because of it is easy to design and realize. But if the input voltage of converter suffers from disturbance in circuit or noise, the output voltage of converter will blend the disturbance component and become changeable. If the voltage loop compensator of converter doesn't design well, the input disturbance may cause the converter unstable.

The feedforward nonlinear carrier can reduce the influence of input disturbance on output voltage of converter. As shown in Fig. 2, it generates the carrier according to the input voltage. If the input voltage has any change, the amplitude of carrier will adjust itself to decrease the change of output voltage.

Fig. 3 is the simulation results of compared with fixed frequency tooth carrier and nonlinear carrier. A 1000Hz sine wave with 2V peak-to-peak voltage is added on input voltage as a disturbance. Without any voltage loop compensation, use fixed frequency tooth carrier can't adjust

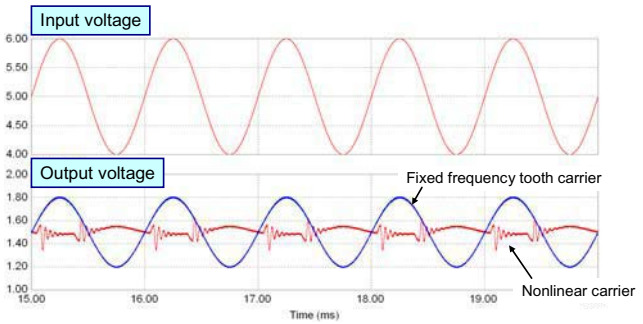


Fig. 3. Simulation results of compared with fixed frequency tooth carrier and nonlinear carrier when input voltage is variable.

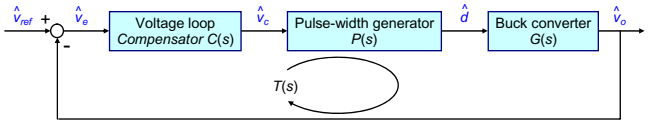


Fig. 4. Block diagram of voltage control loop

itself and hence occurs a variation which equals to 0.6V on output voltage, but the variation can be reduced to 0.25V if nonlinear carrier is used.

If the way descripted in Fig. 2(a) is used, the output of voltage loop compensator will be in low level and may cause the transistors in compensator to leave saturation region. Therefore, the way to generate nonlinear carrier is as Fig. 2(b) in this paper.

B. Adaptive Voltage Loop Compensator

In the design of a loop compensator for a high bandwidth switching regulator we need take careful considerations in determination of gain crossover frequency and compensation of the resonant peak inherent in the output LC filter. The resonant peak of a switching regulator becomes more spiky at light load and more flat as load becomes heavy. Conventional approach is employing current-mode control to ensure robust response under large lard load disturbances. However, this approach needs complicated control circuit and still requires proper phase compensation to ensure a guaranteed phase margin for large load variations. Voltage-mode control with matched load compensation emerges as a competitive solution for dedicated applications due to its simplicity and fast dynamic response. However, this approach still requires a careful design of the voltage loop compensator. Fig. 4 shows the block diagram of voltage-mode control loop of a switching regulator. In order to ease the applications of switching regulators for more versatile applications without the need of loop compensator design, we need to develop an adaptive controller to accommodate various loading conditions and to eliminate the compensation circuit to simplify the circuit implementation. This papers proposes a simple analog circuit oriented adaptive control scheme by tuning the control loop gain with a nonlinear function of the measured average inductor current.

A proportional-integral (PI) phase-lead compensator with adjustable gain is adopted in the realization of the voltage-mode controller. Fig. 5 shows the schematic of the

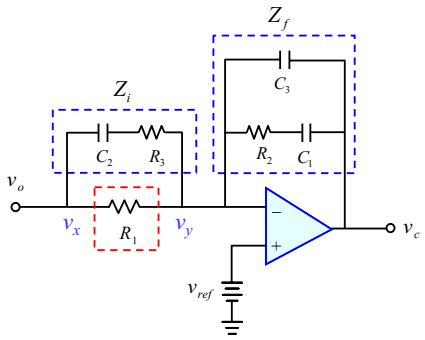
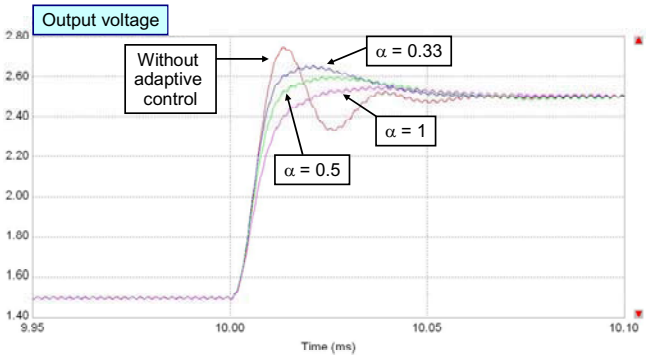
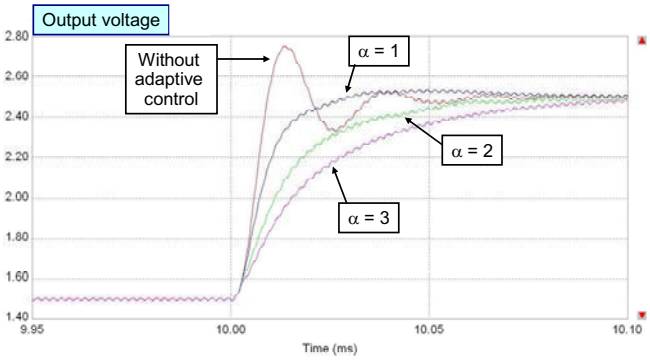


Fig. 5. Schematic of the voltage loop compensator.



(a) α less or equal to 1.



(b) α large or equal to 1.

Fig. 6. Simulation result of adaptive control with a step change of reference voltage.

voltage-loop error amplifier with its compensator circuit and its transfer function is

$$C(s) = K_p \cdot \frac{(s+z_1)(s+z_2)}{s(s+p_1)(s+p_2)} \tag{1}$$

where

$$p_1 = \frac{1}{R_3 C_2} \quad p_2 = \frac{R_2 C_1 C_3}{C_1 + C_3}$$

$$z_1 = \frac{1}{R_2 C_1} \quad z_2 = \frac{1}{R_1 C_2 + R_3 C_2} \quad K_p = \frac{R_1 + R_3}{R_1 R_3 C_3} .$$

By using a voltage-controlled floating resistor [15], the control gain is proportionally adjusted according to the loading condition. The proposed control scheme can achieve a robust fast dynamic response and provides a

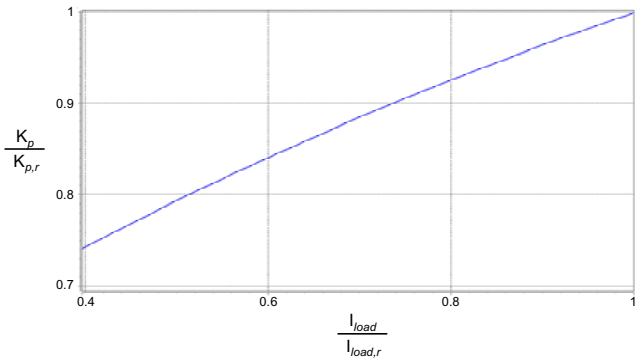


Fig. 7. The relationship between loading condition and adaptive control gain.

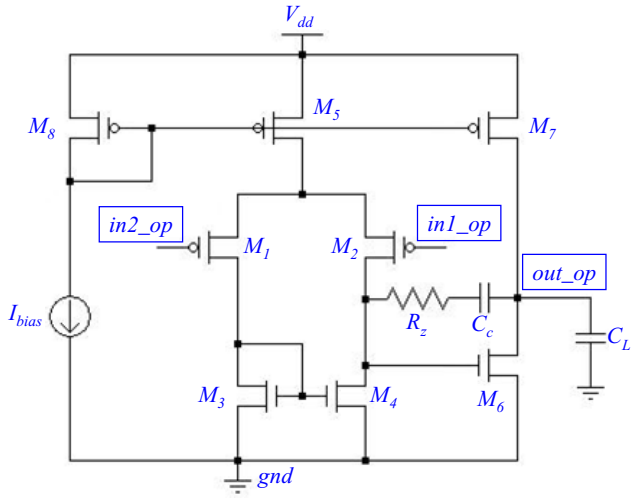


Fig. 8. Schematic of voltage error amplifier.

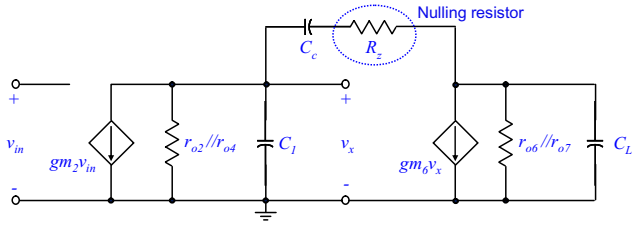


Fig. 9. Small signal model of voltage error amplifier.

simple realization of the CMOS DC/DC synchronous buck converter without any external compensation components.

The loading condition can be determined by the inductance current. The transfer function of voltage loop compensator can be rewritten as

$$C(s) = \frac{K_p}{\alpha \cdot i_L} \cdot \frac{(s+z_1)(s+z_2)}{s(s+p_1)(s+p_2)} \tag{2}$$

where α is a factor repersents the amount that inductance current influences the gain of compensator.

Fig. 6 shows the simulation results of adaptive control with a step change of reference voltage. The reference voltage switches from 1.5V to 2.5V at t = 10ms. In Fig. 6(a), the simulation condition is α less or equal to 1. The response waveform will approach the waveform without adaptive control. It causes the voltage control loop unstable

if is smaller. In Fig. 6(b), the simulation condition is α large or equal to 1. The rise time and settling time will be extend if α is large. In other words, when α becomes large, the gain of compensator decreases and hence the bandwidth of compensator becomes narrow.

The relationship between loading condition and adaptive control gain in this paper is shown in Fig. 7, where $I_{load,r}$ is the rated output current and $K_{p,r}$ is the compensator gain in full loading. According to loading condition, the adaptive control gain will adjust to corresponding value.

III. Circuit Implementation

In this section, the circuit implementation of the load-current adaptive gain control scheme with a feedforward nonlinear carrier control is addressed and the design is based on the structure shown in Fig. 1. Design details of each sub-circuit are presented as follows.

A. Voltage Loop Compensator

Fig. 8 shows the schematic of voltage error amplifier. Compared with other topologies of operational amplifier (OPA) such as telescopic or folded-cascode, two-stage OPA has advantages of high gain and large output swing. Fig. 9 shows its small signal model and its gain, poles and zero are

$$A_v = g_{m2}(r_{o2} // r_{o4})g_{m6}(r_{o6} // r_{o7})$$
$$p_1 = \frac{-g_{m2}}{A_v C_c},\quad p_2 = \frac{-g_{m6}C_c}{C_1C_c + C_cC_L + C_1C_L} \tag{3}$$
$$z_1 = \frac{1}{C_c(\frac{1}{g_{m6}} - R_z)}$$

Note that the nulling resistor R_z should larger than $1/g_{m6}$ to generate a negative zero and p_1 is the dominant pole.

In order to reduce the input offset voltage, V_{ds3} should equal to V_{ds4}. This condition occurs when

$$\frac{(W/L)_3}{(W/L)_6} = \frac{(W/L)_4}{(W/L)_6} = \frac{1}{2}\frac{(W/L)_5}{(W/L)_7}. \tag{4}$$

All MOS are designed to operate in saturation region. Decide the bias current is 2μA and the dominant pole locates 100Hz, the W/L ratio of each MOS can be calculated:

$$(W/L)_1 = (W/L)_2 = (W/L)_3 = (W/L)_4 = (W/L)_6 = \frac{6}{2}$$
$$(W/L)_5 = (W/L)_7 = (W/L)_8 = \frac{12}{2}$$

The Bode plot of designed loop gain $C(s)P(s)G(s)$ is shown in Fig. 10. The designed compensator provides 50° phase margin and the bandwidth of voltage loop is 80kHz.

B. On-Chip Current-Sensing Circuit

Fig. 11 shows the schematic of on-chip current-sensing circuit. During the converter ON-state, M_1 and M_{s1} turn on, the V_{ds} of M_1 and M_2 are almost the same because the OPA

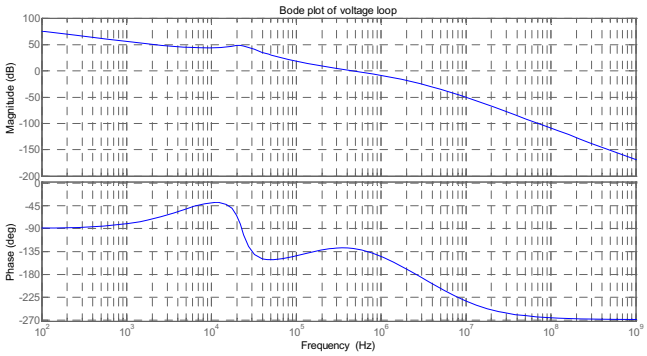


Fig. 10. Bode plot of loop gain

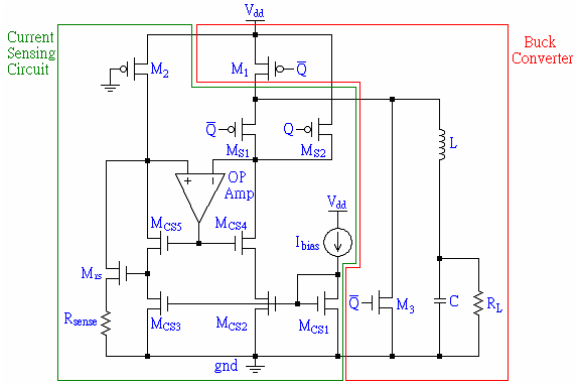


Fig. 11. Schematic of on-chip current-sensing circuit.

in this circuit is used as a voltage mirror. Therefore, $I_{D1} : I_{D2}$ will equal to $(W/L)_1 : (W/L)_2$ and the inductance current is sensed. The drain current of M_2 through R_{sense} to generate a sensing voltage V_{sense} used to control the voltage controlled floating resistor in voltage loop compensator. During the converter OFF-state, M_1 and M_{s1} turn off and M_{s2} turn on. The voltage at the negative input node of OPA is closed to V_{dd}. The drain current of M_1 is zero and M_2 is the same.

Assume all MOS operate in saturation region, the calculated results of the W/L ratio of each MOS are listed below:

$$(\frac{W}{L})_{MS1} = (\frac{W}{L})_{MS2} = 3.5\ ,\ (\frac{W}{L})_{Mrs} = 26$$
$$(\frac{W}{L})_{MCS1} = (\frac{W}{L})_{MCS2} = (\frac{W}{L})_{MCS3} = (\frac{W}{L})_{MCS4} = (\frac{W}{L})_{MCS5} = 0.2$$

C. Low-Pass Filter

Because the on-chip current sensing circuit mentioned before only senses the switch current during ON-state, a low-pass filter should be used to get the average inductance current. The cutoff frequency should much lower than switching frequency of converter, but improperly low cutoff frequency will cause the adaptive control gain adjust insensitively. In this paper, the cutoff frequency is decided at a tenth of switching frequency of converter.

D. Voltage-Controlled Floating Resistor

Fig. 12 shows the schematic of voltage controlled

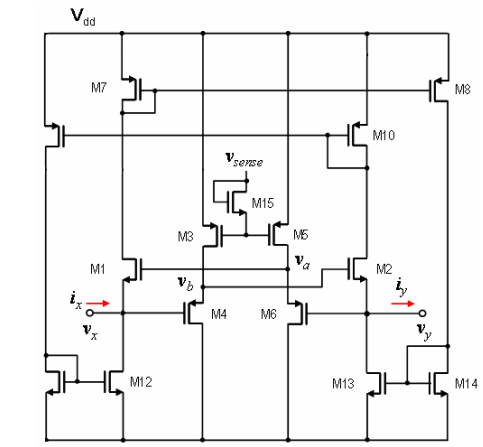


Fig. 12. Schematic of voltage controlled floating resistor.

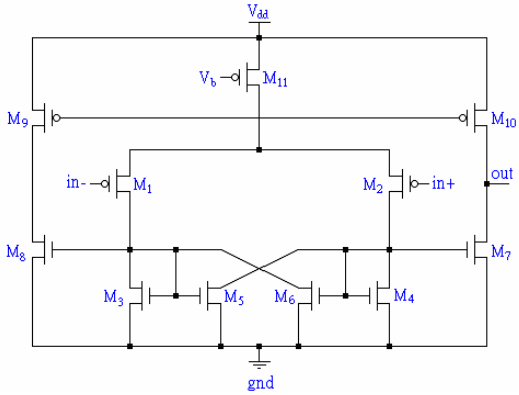


Fig. 13. Schematic of hysteresis comparator.

floating resistor. The gate of M_4 and M_6 are the two terminals of the resistor. Because of $I_x = I_y$:

$$I_x = I_y = I_{D2} - I_{D1}$$
$$= \frac{K_n}{2}(V_a + V_b - V_x - V_y - 2V_{th,n})(V_b - V_a + V_x - V_y) \quad (5)$$

where $K_n = \mu_n C_{ox}(W/L)_{1,2}$. The drain current of the matched transistors M_3 and M_4 are equal:

$$\frac{K_p}{2}(V_{g3} - V_{dd} - V_{th,p}) = \frac{K_p}{2}(V_{g3} - V_{dd} - V_{th,p})$$
$$\Rightarrow V_b = V_x - V_{g3} + V_{dd} \quad (6)$$

where $K_p = \mu_p C_{ox}(W/L)_{3,4}$. Similarly, from the matched transistors M_5 and M_6, V_a can be express as

$$V_a = V_y - V_{g3} + V_{dd}\,. \quad (7)$$

V_{g3} can be express as

$$V_{g3} = V_{sense} - V_{th,n}\,. \quad (8)$$

From (5), (6), (7) and (8), I_x and I_y can be rewritten as

$$Ix = Iy = 2K_n(V_{dd} - V_{sense})(V_x - V_y)$$
$$\Rightarrow \frac{V_x - V_y}{I_x} = \frac{1}{2K_n(V_{dd} - V_{sense})} = resistor\ value\,. \quad (9)$$

Obviously, the resistor value is controlled by V_{sense}.

E. Comparator in PWM Modulator

The comparator, shown in Fig. 13, is implemented by a source-coupled differential pair with positive feedback. The gate-to source voltages of M_1 and M_2 can be calculated from their respective drain currents and are given by

$$v_{GS1} = V_{th,n} + \sqrt{\frac{i_{D1}}{k_p'(W/L)_{M1}}}\ ,\ v_{GS2} = V_{th,n} + \sqrt{\frac{i_{D2}}{k_p'(W/L)_{M2}}} \quad (10)$$

where $k_p' = 0.5\mu_p C_{ox}$. The hysteresis V_H can be calculated as

$$V_H = 2V_{trig} = 2(v_{GS2} - v_{GS1})$$
$$= 2\cdot\left(\sqrt{\frac{i_{D2}}{k_p'(W/L)_{M2}}} - \sqrt{\frac{i_{D1}}{k_p'(W/L)_{M1}}}\right) \quad (11)$$
$$= 2\cdot\sqrt{\frac{i_{D11}}{k_p'(W/L)_{M1}}}\,\frac{\sqrt{\beta}-1}{\sqrt{1+\beta}}$$

where

$$\beta = \frac{(W/L)_3}{(W/L)_5} = \frac{(W/L)_4}{(W/L)_6}\,.$$

Note that the comparator has hysteresis characteristic only when β is larger than 1.

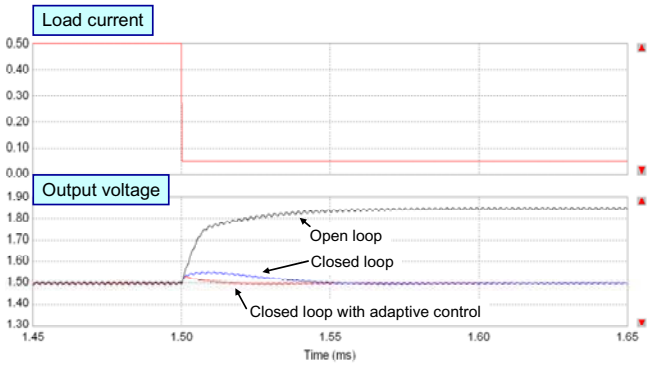
IV. Simulation Results

The designed CMOS DC/DC converter is simulated by using a system-level simulation software tool PSIM and synthesized by a device-level simulation tool HSPICE based on the TMSC 0.35μm technology. The input voltage of converter and the supply voltage of control circuit are DC 5V, the operated frequency of converter is 500kHz. The component values are shown in Table I.

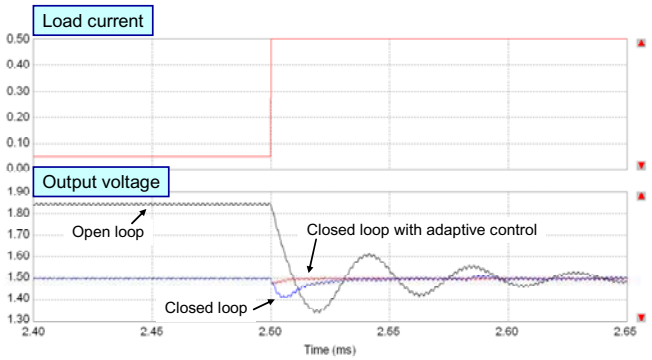
TABLE I
COMPONENT VALUES OF THE SIMULATION SETUP

Buck converter	L	10μH
	C	4.7μF
	R_L	3Ω
Nonlinear carrier generator	R_{int}	16.6kΩ
	C_{int}	88.9pF
Compensator	R_z (in OPA)	16kΩ
	C_c (in OPA)	3pF
	R_2	30kΩ
	R_3	135Ω
	C_1	1nF
	C_2	886pF
	C_3	1pF
Low-pass filter	R_{fil}	1.59kΩ
	C_{fil}	2nF

Fig. 14 shows the simulation results for a large step load change. Converter is operated in discontinuous mode when load current is 50mA. In closed loop simulation with adaptive control, the output voltage variation is 30mV and the settling time is 10μs. It's better than the closed loop simulation without adaptive control.



(a) Switches to light loading.



(b) Switches to heavy loading.

Fig. 14. Simulation results for a step load change.

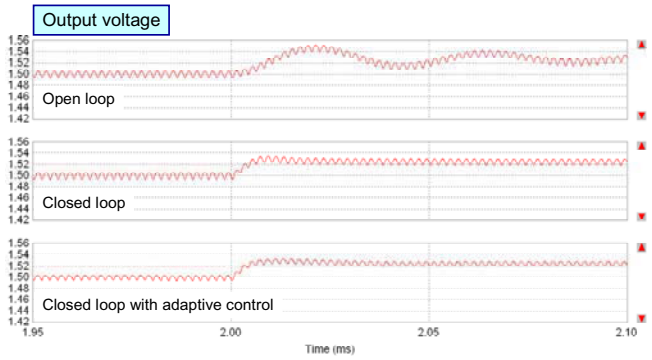


Fig. 15. Simulation results for a step change of reference voltage.

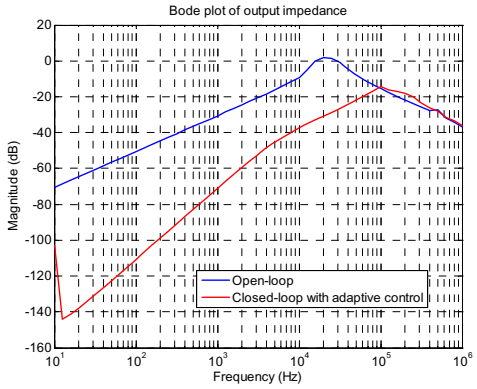


Fig. 16. Frequency response of output impedance.

Fig. 15 shows the simulation results for a step change of reference voltage from 1.5V to 1.525V. The load current

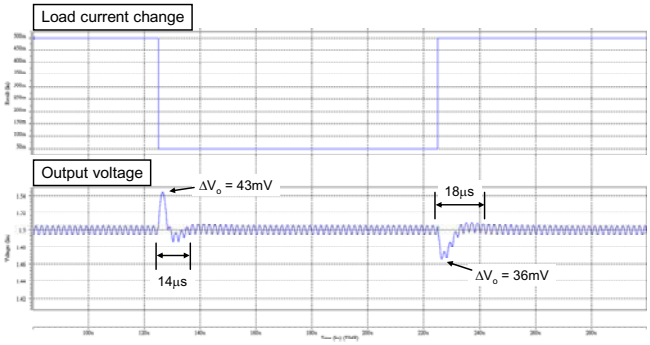


Fig. 17. Simulation results for a large load current change.

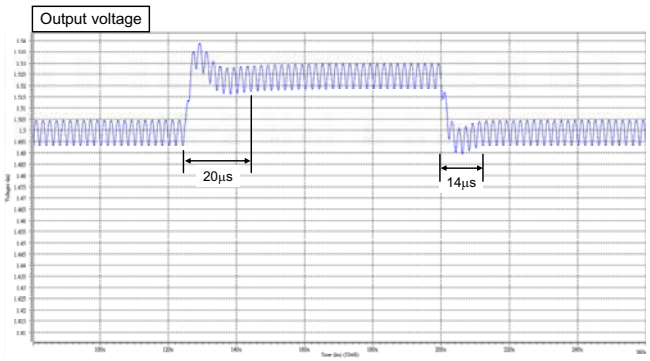


Fig. 18. Simulation results for a step change of reference voltage.

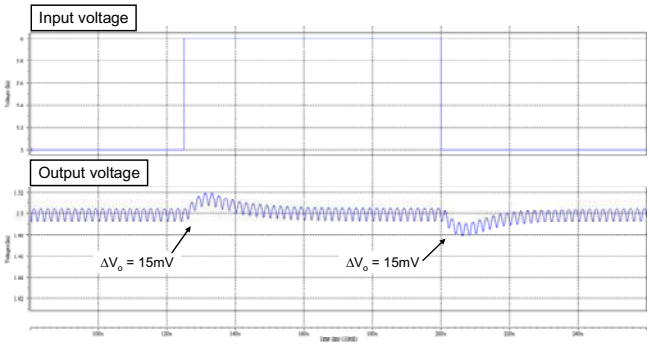


Fig. 19. Simulation results for a step change of input voltage.

only has little change and hence the gain of compensator in adaptive control has little adjustment. Therefore, the transient response of closed loop simulation is similar to closed loop simulation with adaptive control.

Fig. 16 shows the frequency response of output impedance. The resonant frequency is 23kHz. The output impedance is reduced in magnitude after closed loop with adaptive control. After the crossover frequency of the voltage loop, the loop gain is small and hence the frequency response of output impedance is almost the same as open loop control.

Fig. 17, Fig. 18, and Fig. 19 are simulated by HSPICE. Fig. 17 shows the simulation results for a large step load change and Fig. 18 shows the simulation results for a step reference voltage change which are corresponding to the simulation results in Fig. 14 and Fig. 15. Fig. 19 shows the simulation results for a step change of input voltage from 5V to 6V. The variation of average output voltage in transient response is 1%. It means the input disturbance can be reduced by using a feedforward nonlinear carrier control.

V. CONCLUSION

This paper has presented the design of a monolithic current-mode DC/DC converter by using feedforward nonlinear carrier PWM modulation scheme with passive adaptive control to accommodate large load current disturbances as well as input voltage variations. The nonlinear carrier generated by the integration of input voltage can reduce the input-to-output voltage disturbance effect compared with the conventional PWM technique. The passive adaptive controller provided a simple self-adjust of gain based on the averaged inductor current to stabilize the control loop to accommodate different loading conditions. Simulation results show the designed adaptive monolithic dc-dc switching regulator can maintain fast and well damped dynamic response for large changes of input voltage and load current. This research reveals feasibility of implementation of adaptive switching dc-dc regulators for wide applications without loop compensator design by using analog technology.

REFERENCES

[1] Z. Ren, B. H. Krogh, and R. Marculescu, "Hierarchical adaptive dynamic power management," *IEEE Transactions on Computers*, vol. 54, no. 4, pp. 409-420, April 2005.

[2] A. Lidow, D. Kinzer, G. Sheridan, and D. Tam, "The semiconductor roadmap for power management in the new millennium," *Proceedings of the IEEE*, vol. 89, no. 6, pp. 803-812, June 2001.

[3] G. Patounakis, Y. W. Li, and K. L. Shepard, "A fully integrated on-chip DC-DC conversion and power management system," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 3, pp. 443-451, March 2004.

[4] Surya Musunuri, Patrick L. Chapman, Jun Zou, and Chang Liu, "Design issues for monolithic DC–DC converters," *IEEE Trans. on Power Electronics*, vol. 20, no. 3, pp. 639-649, May 2005.

[5] A. P. Dancy and A. P. Chandrakasan, "Ultra low power control circuits for PWM converters," *IEEE PESC Conf. Rec.*, pp. 21-27, 1997.

[6] B. Sahu and G. A. Rincon-Mora, "A low voltage, dynamic, noninverting, synchronous buck-boost converter for portable applications," *IEEE Transactions on Power Electronics*, vol. 19, no. 2, pp. 443-452, March 2004.

[7] R. Mammano, "Switching power supply topology: voltage mode vs. current mode," in Unitrode Design Note DN-62. Dallas, TX: Texas Instruments Incorporated, 1994.

[8] Wing-Hung Ki, "Analysis of subharmonic oscillation of fixed-frequency current-programming switch mode power converters," *IEEE Trans. on Citrcuits and Systems - I: Fundamental and Applications*, vol. 45, no. 1, pp. 104-108, Jan. 1998.

[9] Cheung Fai Lee and Philip K. T. Mok, "A monolithic current-mode CMOS DC–DC converter with on-chip current-sensing technique," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 1, pp. 3-14, Jan. 2004.

[10] H. Sakurai and Y. Sugimoto, "Analysis and design of a current-mode PWM buck converter adopting the output-voltage independent second-order slope compensation scheme," *IEICE Trans. on Fundamentals*, vol. E88–A, no. 2, pp. 490-47, Feb. 2005.

[11] J. T. Mossoba and P.T. Krein, "Design and control of sensorless current mode dc-dc converters," *IEEE APEC Conf.* Rec., 2003.

[12] Man Siu, Philip K. T. Mok, Ka Nang Leung, Yat-Hei Lam, and Wing-Hung Ki, "A voltage-mode PWM buck regulator with end-point prediction," *IEEE Trans. on Circuits and Systems—II: Express Briefs*, vol. 53, no. 4, pp. 294-298, April 2006.

[13] A. J. Forsyth, I. K. Ellis, and M. Moller, "Adaptive control of a high-frequency DC-DC converter by parameter scheduling," *IEE Proceedings - Electric Power Applications*, vol. 146, no. 4, pp. 447-454, July 1999.

[14] B. Patella, A. Prodic, A. Zirger, and D. Maksimovic "High-frequency digital controller IC for DC-DC converters," *IEEE APEC Conf. Rec.*, pp. 374 –380,2002.

[15] Hassan O. Elwan, Soliman A. Mahmoud, and Ahmed M. Soliman, "CMOS voltage controlled floating resistor," *Int. J. Electronics*, vol. 81, no. 5, pp. 571-576, 1996.