Demonstration of Gigabit WDMA Networks Using Parallelly Processed Subcarrier Hopping Pilot-Tone (P^3) Signaling Technique

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***Abstract*— An extremely short header transmission and processing time in a gigabit wavelength-division-multiple-access (WDMA) network has been experimentally demonstrated. This was achieved by using parallelly processed subcarrier hopping pilot-tones in combination with an array of detectors and RF switches. The results showed that, without considering the time consumed in an arbitration circuit, the total processing time of the hopping pilot-tone headers was as short as 40 ns which is independent of the number of network nodes and data transmission rate.**

I. INTRODUCTION

IN A high-speed packet-switched WDMA network, wavelength channel reconfiguration time, signaling transmission time, and signaling processing time may severely limit the throughput performance of the network. Wavelength reconfiguration time can be shortened by, e.g., using the combination of a wavelength-demultiplexer, a photodetector array, and electronic selector fabrics at the receiving site, and fixed wavelength transmitters at the transmitting sites [1]. To reduce the signaling transmission and processing time, a signaling technique of using subcarrier-multiplexed (SCM) headers was proposed to reduce the long delay in serially processing multiple users' headers, and to effectively separate the high-speed data payload (e.g., >Gb/s) from the low-speed control header (e.g., <100 Mb/s) [2]. However, a long processing delay may still be incurred in using an SCM header because of the multiple bytes in the header that must be serially processed by a computer CPU or a logical circuit. To alleviate this processing load, an SCM pilot-tone signaling technique was used in a ring network [3]. In this letter, we extend the pilot-tone-based SCM signaling technique by using parallelly processed hopping pilot-tones [4], or the hopping "P^3" signaling technique. The feasibility of using hopping P^3 signaling technique with an array of detectors and RF switches to obtain an extremely short header transmission and processing time was experimentally demonstrated.

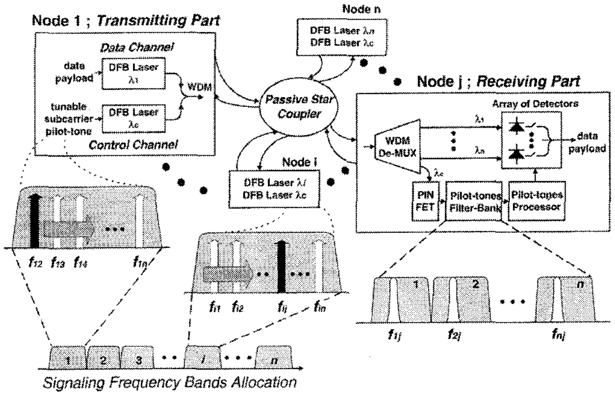

Fig. 1. General network configuration with illustrations of signaling frequency bands allocation and a node filter bank.

II. NETWORK OPERATION PRINCIPLE

The operation principle of our proposed signaling scheme can be illustrated in a general network configuration as shown in Fig. 1. All nodes are assumed to be synchronized by a system clock. The transmitting part in a node i consists of a DFB laser with a unique wavelength λ_i to transport data payload, and a DFB laser with a wavelength λ_c (common to all nodes) to carry a tunable pilot tone. The tunable pilot tone is supposed to hop among frequencies f_{ij} ($j = 1, 2, \cdots, n,\ j \neq i$; i and j represent the transmitting and receiving nodes, respectively) at a rate controlled by the system clock. The control signaling slot of the pilot-tone is scheduled to transmit one slot ahead of its corresponding data (the tell-and-go protocol [5]). The receiving part in each node consists of a WDM demultiplexer, an array of detectors for data payload, an optical receiver for SCM hopping pilot-tones, and an ASK pilot-tone processor which functions as follows: the pilot tones from all other $N-1$ nodes are spatially separated by the filter bank simultaneously; an envelope detector and a reshaping circuit convert these pilot-tones into parallel pulses, e.g., $010010\cdots01$, where 1 and 0 represent the presence or absence of the corresponding call-setup pilot tones, respectively. Arbitration and switch driving circuits are then used to turn on one of the detector-array RF switches at the time when the data payload arrives.

III. EXPERIMENT

Our experimental setup is shown in Fig. 2. Each of the three transmitting nodes (1, 2, and 3) had a 1.55 μm, 1 Gb/s DFB

Manuscript received December 18, 1995; revised March 25, 1996. This work was supported by National Science Council, R.O.C., under Contract NSC84-2215-E009-011.

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Publisher Item Identifier S 1041-1135(96)05106-3.

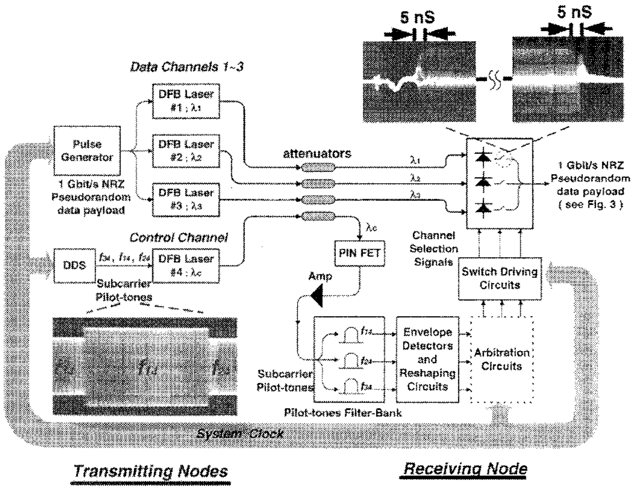

Fig. 2. Experimental setup.

laser transmitter at wavelengths λ_i (i = 1, 2, 3). Node 4 is the receiving node and had three optical receivers. Each of the receiver was followed by an RF switch with a bandwidth of 1 GHz. A fourth DFB laser was used to deliver three consecutive frequencies (f_{34} = 300 MHz, f_{14} = 100 MHz, f_{24} = 250 MHz) which were generated by a direct digital synthesizer (DDS). The three frequencies represent the pilot-tones transmitted from nodes 1–3 at three consecutive time slots, respectively. Each time slot was assumed to be 500 ns which is equivalent to the total time required for 53 bytes of 1 Gb/s ATM data, plus its associated guard and preamble bits. This 500 ns time slot will be shortened as data rate increases. For example, the time slot becomes 250 ns for a data rate of 2.5 Gb/s [6]. Note that the DDS can hop from one frequency to the other within 20 ns. In node 4, three filters centered at f_{14}, f_{24}, and f_{34} with a bandwidth of 5 MHz and a delay of ~5 ns were used to spatially separate the three pilot-tones. The separated pilot-tones then parallelly went through an envelope detector and a pulse-shaping circuit with a ~30 ns delay. The arbitration circuit was temporarily neglected in our experiment. Finally, the selected pulse was used to turn on one of the three RF switches. As shown in Fig. 2, the synchronized system clock was connected to the pulse generator, the DDS, and the switch driving circuits. The turn-on and turn-off time of the RF switch were both about 5 ns, as can be seen in Fig. 2. Without considering the arbitration circuit, the total processing time of the pilot-tone headers was about 40 ($= 5 + 30 + 5$) ns, and this time is independent of the number of nodes. Note that 40 ns is equivalent to the time required to process less than 4 bits in a conventional 80 Mb/s control channel [6]. This extremely short header processing time leaves sufficient room for future data rate upgrade, i.e., when the data rate is increased to 2.5 Gb/s (time slot ≅250 ns) or 5 Gb/s (time slot ≅125 ns).

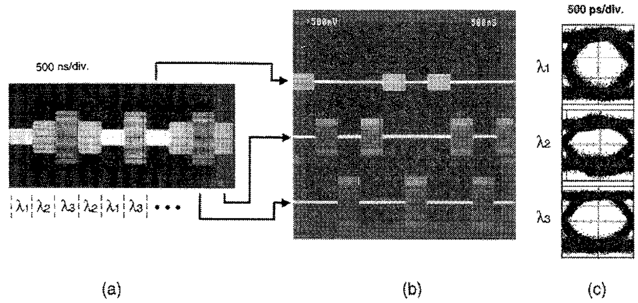

Fig. 3. (a) Consecutively received packets at node 4, (b) packets from λ_1, λ_2, and λ_3, respectively, and (c) 1 Gb/s eye diagrams.

The received packets at node 4 are shown in Fig. 3(a). The slotted packets (each with a 500 ns duration) were sequentially received from $\lambda_1, \lambda_2, \lambda_3, \lambda_2, \lambda_1, \lambda_3 \cdots$ in accordance with the tuning of f_{i4} (i = 1, 2, 3). For illustration purpose, the amplitudes of the packets from the three nodes were purposely made unequal so that they can be easily distinguished. The packets and the associated eye diagrams from each of the three nodes are displayed in Fig. 3(b) and (c), respectively.

IV. CONCLUSION

In conclusion, we have experimentally demonstrated the feasibility of using subcarrier-based P^3 (parallelly processed hopping pilot-tones) signaling technique, in combination with an array of detectors and RF switches, to obtain an extremely short header transmission and processing time in a four-node gigabit WDMA network.

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