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Self-assembled $In_{0.22}Ga_{0.78}As$ quantum dots grown on metamorphic $GaAs/Ge/Si_xGe_{1-x}/Si$ substrate

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Self-assembled $In_{0.22}Ga_{0.78}As$ quantum dots (QDs) grown on Si substrate with Ge/SiGe as buffer layer grown by metal organic vapor phase epitaxy were investigated. Transmission electron microscopy and atomic force microscopy images were used to observe the size and space distribution of the $In_{0.22}Ga_{0.78}As$ QDs grown on the GaAs/Ge/GeSi/Si layer structure. The influence of the growth temperature on the QDs size and density distribution was investigated. For QDs grown at 450 °C, the density of the $In_{0.22}Ga_{0.78}As$ dots was estimated to be 1×10^{11} cm^{-2} and the $In_{0.22}Ga_{0.78}As$ QDs thickness was 5 ML (monolayer) thick. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2337770]

I. INTRODUCTION

III-V compound semiconductor devices have been widely used for high-speed electronics and optoelectonics applications. Recent progress of the epitaxial growth technique has allowed the realization of III-V based semiconductor nanostructures such as quantum wires and quantum dots (QDs). Using Stranski-Krastanov (SK) growth mode with InGaAs QDs (0.9–1.7 μm wavelength response) are expected electronic and optical properties for the optical communications and near-infrared imaging application[1–3] such as near-infrared spectrography, laser beam profiling, and semiconductor inspection. However, most of the quantum dots structures were grown on GaAs substrate, which is easy to grow and less dislocations. Si substrate has superior mechanical properties, higher thermal conductivity, and lower cost than GaAs. As a result, quantum dots grown on Si substrate provide great potential in fabrication cost down or integration of III-V based and Si based devices. However, there is a large lattice constant difference between Si and GaAs. This crystallographic problem indicates that there is a need for a well-designed buffer layer growth technology to accommodate the large lattice mismatch. One of the approaches is via graded SiGe buffer layer.[4] This method has already been extensively studied; however, a very thick buffer layer is required to get a high-quality GaAs layer on Si. In our former studies, a SiGe strained buffer structure for the growth of high-quality GaAs layers on Si (100) substrate is proposed.[5] The total buffer thickness is only 2.6 μm, which is very thin compared to that grown by molecular beam epitaxy (MBE) system using graded SiGe buffer layer which is 10 μm in thickness.[4] In this paper, we demonstrate the feasibility of using SiGe strained buffer technology for the growth of III-V based structures on Si substrate. The effect of the growth temperature on the InGaAs quantum dot size distribution was investigated. It was found that a thin GaAs layer inserted between the Ge buffer and the GaAs layer can improve the QD size uniformity and distribution. Atomic foro microscopy (AFM) measurement on these QDs showed that if the QDs were grown at 450 °C with 30 s gas interruption time, the dot density of about 1×10^{11} cm^{-2} can be achieved successfully.

II. EXPERIMENTAL PROCEDURES

The growth of the SiGe/Ge buffer layers on Si was carried out using an ultra-high vacuum chemical vapor deposition (UHVCVD) system using Si_2H_6 and GeH_4 as the depositing sources with a base pressure of less than 2×10^{-8} torr by the furnace. First, a 4 in. Si wafer with 6° off (100) toward ⟨110⟩ direction was cleaned using 10% HF dipping followed by high-temperature baking at 800 °C in the growth chamber for 5 min. Then, a 0.8 μm $Si_{0.1}Ge_{0.9}$, a 0.8 μm $Si_{0.05}Ge_{0.95}$, and a 1.0 μm Ge layer were grown at 400 °C in sequence. Between successive layers, growth was interrupted for an *in situ* 15 min 750 °C annealing. After Ge layers were grown on the Si substrate, the sample was changed to another metal organic vapor phase epitaxy (MOVPE) system to grow GaAs and $In_{0.22}Ga_{0.78}As$ QDs. The $In_{0.22}Ga_{0.78}As$ QDs/GaAs layer were grown on the Ge/SiGe/Si heterostructure by MOVPE method at 40 torr reactor pressure at different growth temperatures and 30 s interruption time for the AsH_3 gas. InGaAs QD layers were grown at 450, 480, and 520 °C.[6] The triethyl gallium (TEGa) and trimethyl indium (TMIn) were used as the III

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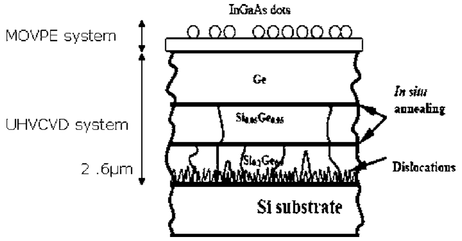

FIG. 1. Schematic diagram of InGaAs QDs on Si substrate.

source, and the arsine (AsH_3) was used as the V source. V/III ratio was kept at 60 for the GaAs layer and 10 for the $In_{0.22}Ga_{0.78}As$ QDs layer. TEM was used to observe the thickness of the epitaxial layers and the dislocation distribution. The transmission electron microscopy (TEM) samples were prepared using the standard "sandwich" technique followed by ion milling. Structural analyses of the epitaxial layers were performed on the cross-section using high-resolution transmission electron microscope (HRTEM). This study was carried out on a Phillips-200 electron microscope operating at 200 kV with an interpretable resolution of 0.16 nm. Figure 1 shows the schematic of the structure of the $In_{0.22}Ga_{0.78}As$ QDs/GaAs/Ge/Si. The surface morphology and the size of the quantum dots were analyzed by AFM in the contact mode.

III. RESULTS AND DISCUSSIONS

A. Ge layers grown by UHVCVD system

Figure 2 shows the cross-section TEM image of the Ge buffer layers grown on the Si substrate. The total thickness of the epitaxial structure is only approximately 2.6 μm. The method mainly involves (1) growth of two Si_xGe_{1-x} layers consisting of a 0.8 μm $Si_{0.1}Ge_{0.9}$ layer, a 0.8 μm $Si_{0.05}Ge_{0.95}$ layer, and (2) *in situ* 15 min 750 °C annealing performed on each individual layer. There were a large number of dislocations located near the $Si_{0.1}Ge_{0.9}/Si$ interface and at the lower part of the $Si_{0.1}Ge_{0.9}$ layer due to the large Ge composition difference in the Ge two layers. The upward propagated dislocations were bent sideward and terminated very effectively by the $Si_{0.05}Ge_{0.95}/Si_{0.1}Ge_{0.9}$ and $Ge/Si_{0.05}Ge_{0.95}$ interfaces due to compressive stress induced in the interfaces. Almost no threading dislocation can propagate into the top Ge layer. The details of the growth of the Ge/SiGe buffer layers can be found in Ref. 5

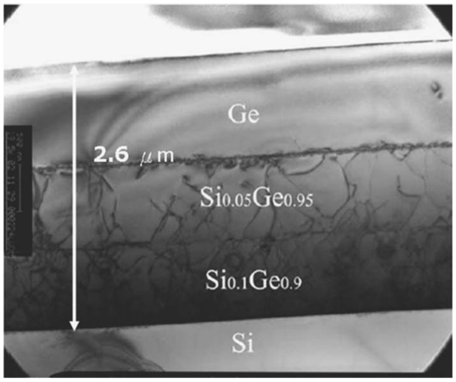

FIG. 2. Cross-sectional TEM image of the epitaxial structure.

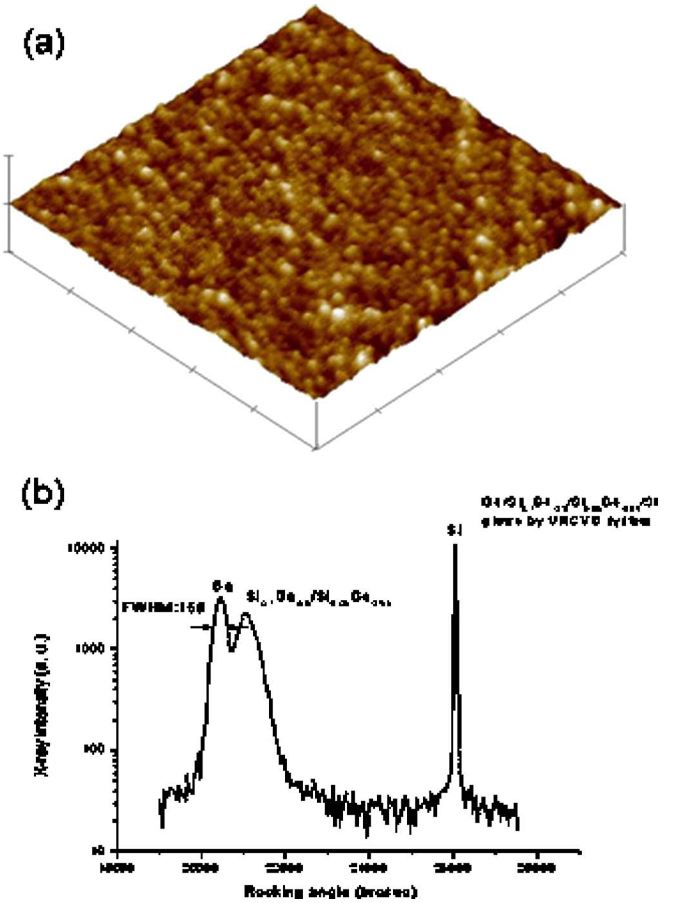

FIG. 3. (Color online) (a) AFM image of the surface of the Ge layer. (b) The quality of Ge layer of FWHM of x-ray rocking curves.

Figure 3(a) shows the surface roughness of the Ge layer grown on Si wafer with 6° off (100) toward ⟨110⟩ direction. The root mean square (rms) of the Ge layer was 1.3 Å and the roughness average (R_a) was 1.04 Å. The smooth surface is useful for the growth of the III-V material on the top of the Ge layer. The top Ge layer growth exhibits a low threading dislocation density and very smooth surface. It is shown that this proposed growth technique is very practical for the growth of high-quality Ge layers on Si substrates. Figure 3(b) shows the rocking curve of the stacked Ge and SiGe epilayers. The value of full width at half maximum (FWHM) for the top Ge layer was 150 arc sec.

B. APB-free GaAs growth on Si

GaAs layers were grown on Si substrate with $Ge/Si_{0.05}Ge_{0.95}/Si_{0.1}Ge_{0.9}$ layer as buffer by low-pressure-MOVPE system have low mismatch ($<0.12\%$) and low thermal expansion difference ($<2\%$) GaAs and Ge. Although the low lattice mismatch of the GaAs/Ge system suggests that it should be nearly dislocation-free considerable problems still exist related to the epitaxy between polar (GaAs) and nonpolar (Ge) semiconductors resulting in the formation of antiphase domains. The most common method for avoiding the antiphase domains (APDs) at the GaAs/Ge interface is by the use of tilted substrates with sufficient ther-

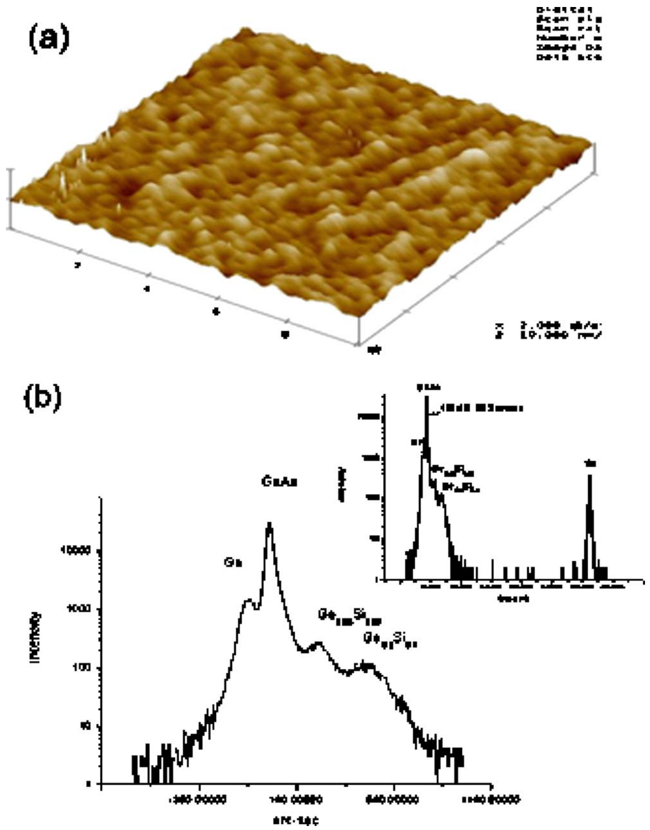

FIG. 4. (Color online) AFM scans $(10\times 10\ \mu\text{m}^2)$ of the typical GaAs grown on the composite structure with Ge/SiGe/Si substrate with 6° off degree toward [110]. (b) The quality of GaAs layer of FWHM of x-ray rocking curves.

mal annealing. The suppression of APDs can be achieved by using Ge wafer with 6° off (100) toward ⟨110⟩ direction. For the substrates with a larger miscut angle (6°), in which the terraces between the steps are very narrow, the steps are so close to each other that no nucleus can be formed on the terraces. As the growth proceeds, the initial nuclei coalesce so that a single domain of GaAs is achieved.[7] This diminishes the chance for two-dimensional nucleation on the terraces. Therefore, only GaAs nuclei at the steps will be formed. Consequently, all the layers have the same sublattice orientation. In this study, the sample was grown on Ge/SiGe/Si substrate with 6° off (100) toward ⟨110⟩ direction. No antiphase bourndary (APB) was observed on the surface. The AFM data of the surface roughness were shown in Fig. 4(a). The rms of the GaAs layer grown was 7.35 Å and the R_a was 5.81 Å. Double crystal x-ray measurement of the sample shows five peaks in the diffraction spectra, with GaAs peak (30.2 arc sec), pure Ge peak, $\mathrm{Si_{0.1}Ge_{0.9}}$ peak, $\mathrm{Si_{0.05}Ge_{0.95}}$ peak, and Si substrate peak, as shown in Fig. 4(b). The narrower FWHM of the GaAs peak indicates that high-quality GaAs layer was grown on Si.

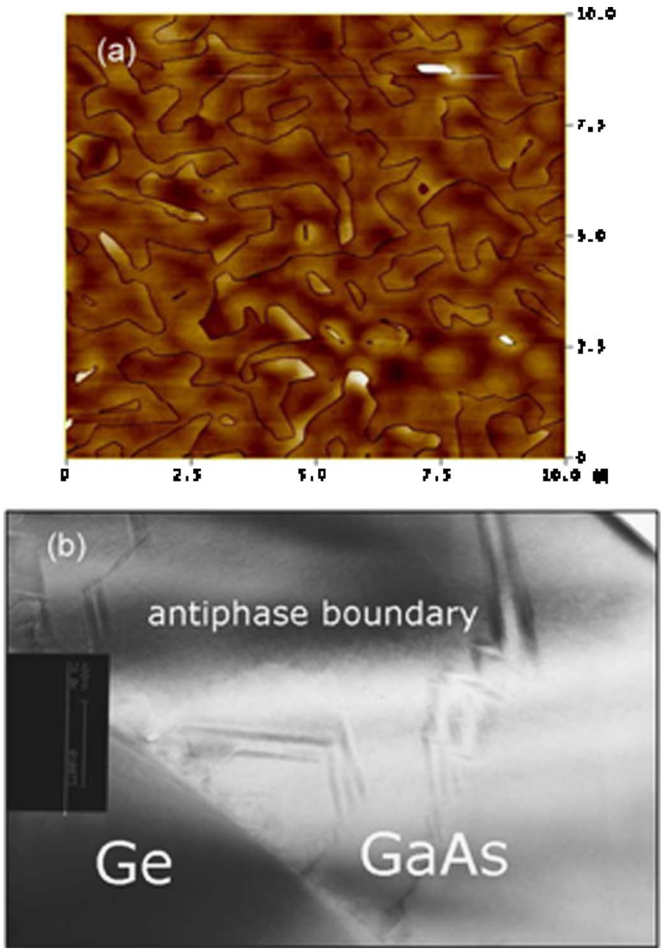

FIG. 5. (Color online) (a) AFM scans $(10\times 10\ \mu\text{m}^2)$ of the typical GaAs grown on the composite structure with Ge/SiGe/Si substrate with 6° off degree toward ⟨110⟩. (b) The TEM micrograph of GaA layer grown on Si substrate with 6° off degree toward ⟨110⟩ shows that APBs cross the GaAs layer.

For the substrate with a small miscut angle, nuclei form at the steps and terraces with the latter having crystal orientation 90° rotated. Figure 5(a). shows the two possible growth orientations of the GaAs layer on the 0° off sample. The two domains differ from each other in a reversal Ga and As atoms in the sublattices resulting in a rotation of 90° with respect to the substrate.[8] AFM measurement shows many square lines on the surface. The depth of APBs was 13 nm and R_a value was 8 nm [Fig. 5(a)] for the GaAs grown on 0° off Si substrate. APBs provide deep levels in the forbidden gap and act as nonradiative recombination surface. In our study, the twins and the lattice defects finally disappeared when the GaAs/Ge/SiGe epilayers were grown on Si substrate with 6° off (100) toward ⟨110⟩ direction. The reason for this resides in the structure and the density of the steps, not the (110) terrace. The occurrence of the self-annihilation processes of APBs is very important for the growth of the device quality GaAs/Ge/SiGe/Si epitaxial layers.

C. InGaAs QDs layer grown by MOVPE system

Figure 6. shows the top layer of the $\mathrm{In_{0.22}Ga_{0.78}As}$ QDs/GaAs/Ge/SiGe/Si structure. These QDs were grown at 480 °C after a 30 s growth interruption time without $\mathrm{AsH_3}$. During the growth interruption, arsenic surface is unstable to result in indium segregation increases and instead appears as an unbounded indium-floating layer. The thickness of the GaAs layer was 40 nm. The $\mathrm{In_{0.22}Ga_{0.78}As}$ QDs [~5 ML (monolayer)] were grown on the top of the GaAs layer, which corresponds to the critical layer thickness for the InGaAs QDs formation on the GaAs layers.[9] For the

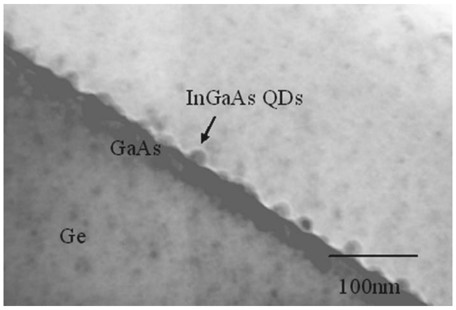

FIG. 6. Bright-field cross-section TEM image of the $In_{0.22}Ga_{0.78}As$ QDs formed on GaAs/Ge/SiGe/Si.

GaAs/InGaAs material system, typically, the growth appears in Sranski-Krastanov mode, the driving force for the QD formation is the 2% lattice mismatch of InGaAs/GaAs. The stress on a crystal surface can provide a natural driving force for nanostructure formation and three-dimensional island formation in the lattice mismatched growth on the planar low index substrates. For GaAs/InGaAs material system with small interface energy but large lattice mismatch, initial growth is layer by layer, when thicker layer was grown, it has large strain energy and can lower its total energy by forming isolated thick islands.[10] InGaAs QDs were grown on different off-orientation Si substrates for compasion. Figure 7(a) shows that InGaAs QDs were grown on the 6° off angle substrate; there was no APB on the surface and the distribution of the InGaAs QDs is uniform. Figure 7(b) shows that InGaAs QDs were grown on the substrate with 0° off (100) toward ⟨110⟩ direction. The InGaAs QDs accumulated along the APBs, which support enough energy for the formation of the InGaAs QDs resulting in nonuniform quantum dots distribution on the surface.

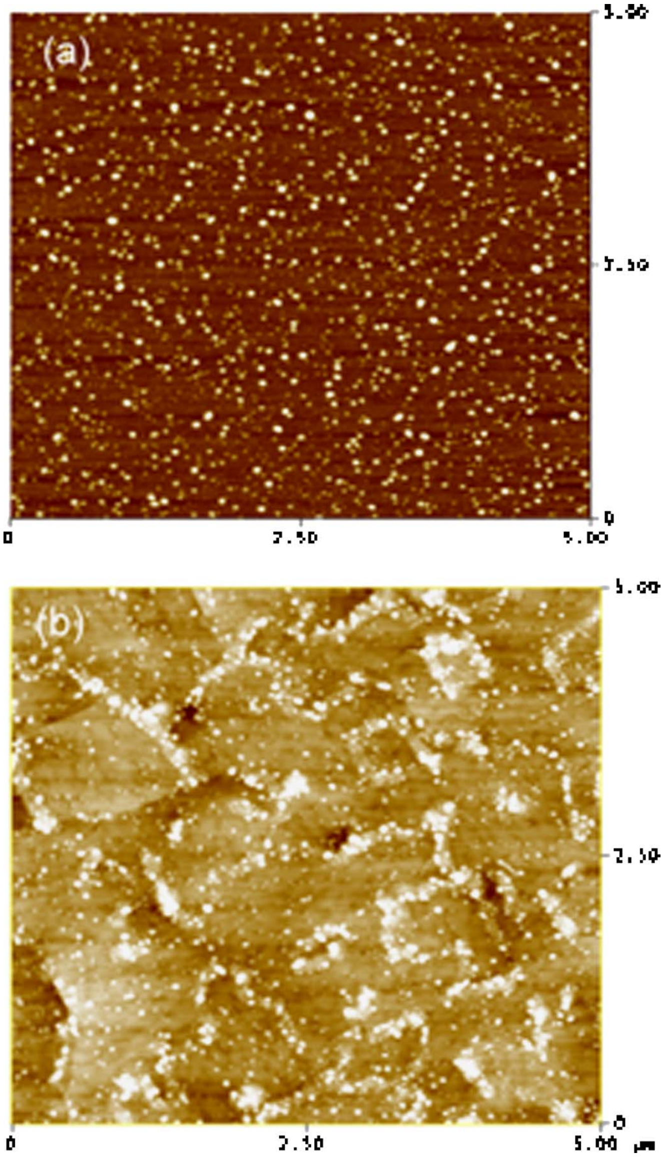

FIG. 7. (Color online) Distribution of InGaAs QDs grown on misorientated Si substrate. (a) 6° off degree toward ⟨110⟩ (b) 0° off degree toward ⟨110⟩.

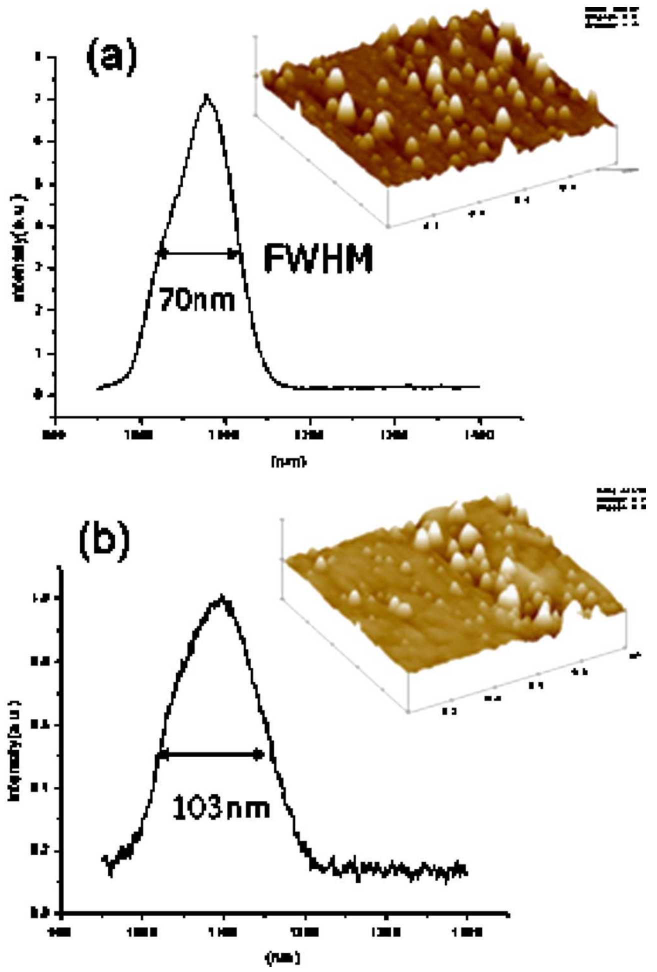

FIG. 8. (Color online) PL measurement of the InGaAs QDs grown on misorientated Si substrate. (a) 6° off degree toward ⟨110⟩ and (b) 0° off degree toward ⟨110⟩.

While InGaAs QDs grown at 0° substrate give a weak asymmetric PL emission profile, the InGaAs QDs grown at 6° off substrate show narrow and high intensity peaks. Figure 8(a) shows the photoluminescence (PL) emission of the InGaAs QDs grown on the substrate with 6° off (100) toward ⟨110⟩ direction; the FWHM of the PL emission is 77 nm in this case. Figure 8(b) shows the PL emission of the InGaAs QDs grown on substrate 0° off (100); the FWHM of the PL emission is 103 nm. The nonuniform InGaAs QDs result in the larger FWHM of the PL emission.

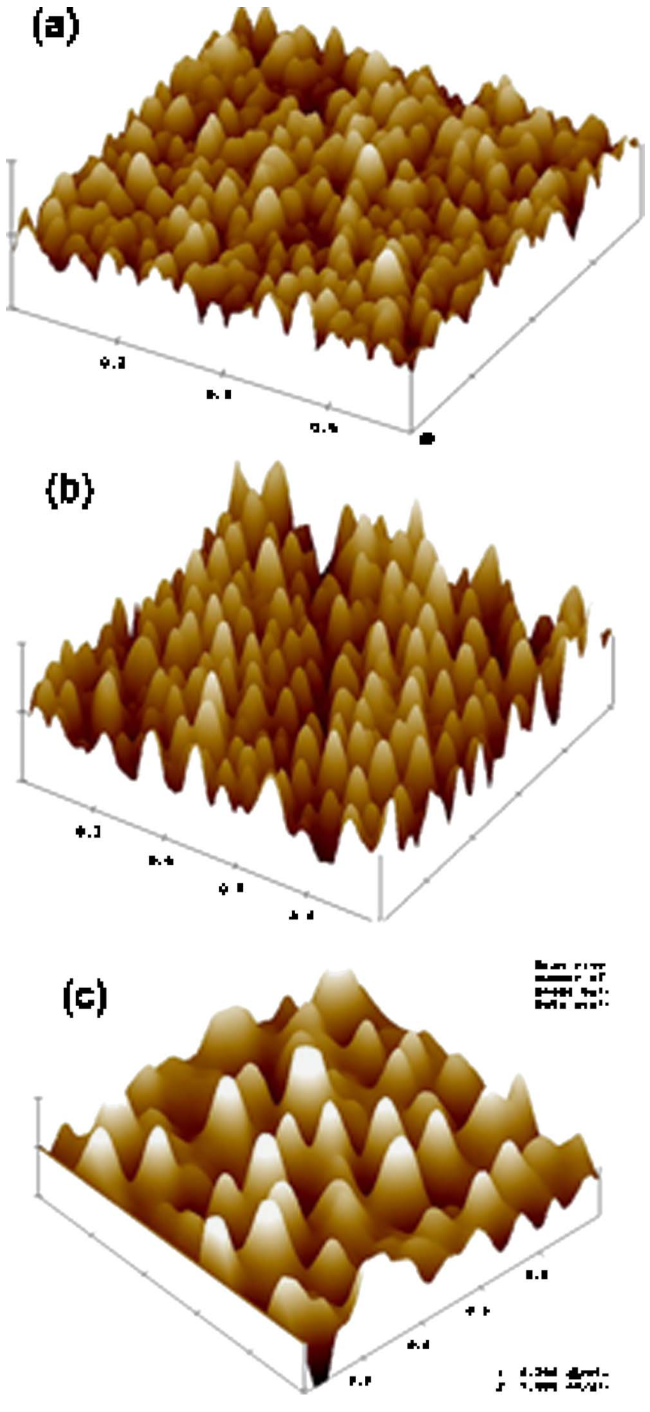

FIG. 9. (Color online) AFM images of self-assembled InGaAs QDs grown at different temperatures. (a) 450 °C (b) 480 °C, and (c) 520 °C.

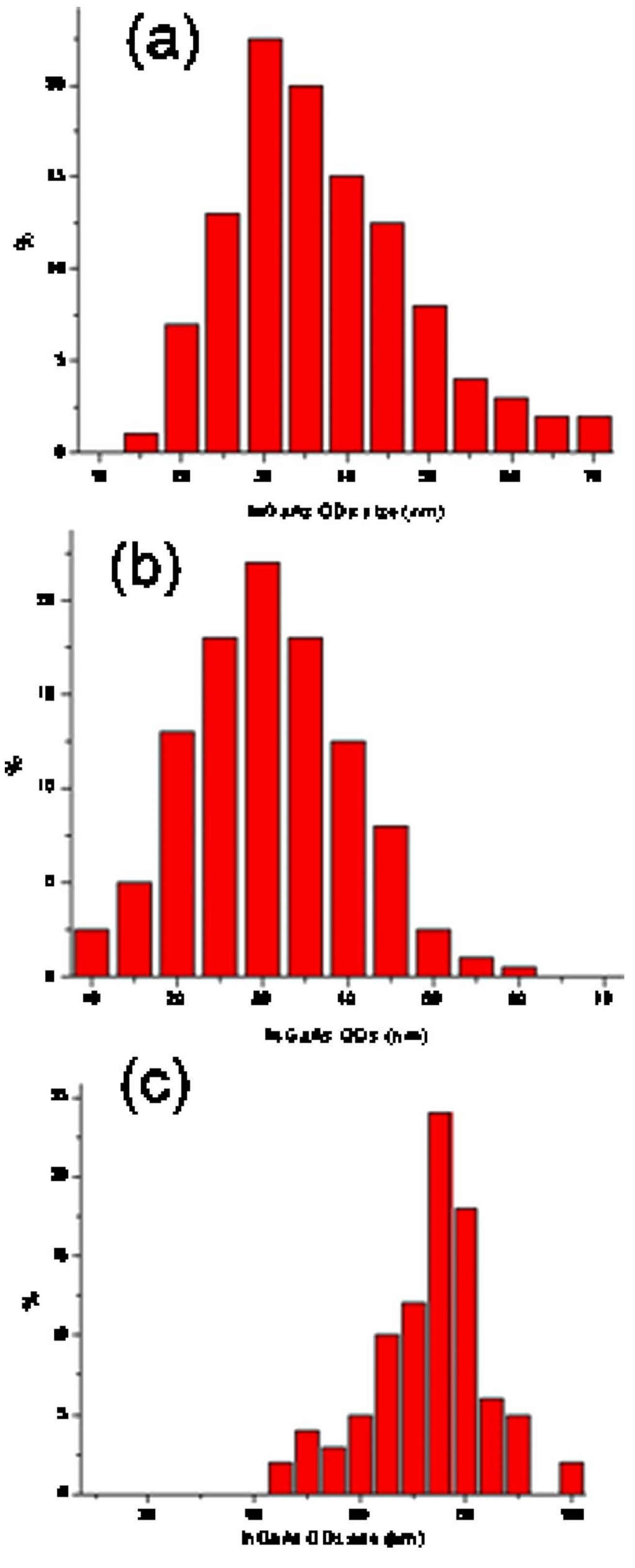

FIG. 10. (Color online) Average size distribution of the $In_{0.22}Ga_{0.78}As$ QDs grown at different temperatures. (a) 450 °C (b) 480 °C and (c) 520 °C.

AFM image of the $In_{0.22}Ga_{0.78}As$ QDs grown on the composite structure with silicon substrate is shown in Fig. 9(a). The growth conditions of these quantum dots are the growth temperature of 450 °C and the TMIn, TEGa, and AsH_3 flows of 3, 3, and 90 μmol/s, respectively, at the mean growth rate of the $In_{0.22}Ga_{0.78}As$ QDs at 0.2 ML/s. The $In_{0.22}Ga_{0.78}As$ QDs in the sample were 5 ML $In_{0.22}Ga_{0.78}As$ QDs/GaAs/Ge/Si and the density of $In_{0.22}Ga_{0.78}As$ QDs was about 1×10^{11} cm^{-2}. The small and vague features of QDs observed at low temperature are explained by poor surface diffusion kinetics. At low growth temperature, atoms can only diffuse short distance before they are incorporated. Therefore, island formation is kinetically delayed of frozen out[11–13]. Reduced mass transport may limit the amount of indium participating in the gallium-indium exchange and reduce the effect of arsenic on the surface. At high growth temperatures, the dot formation is kinetically enhanced because atoms can diffuse longer distance before low-density and large dot formation. AFM image in Fig. 9(c). reflects the feature with QD array density decreasing and the size of each dot increasing shows that $In_{0.22}Ga_{0.78}As$ QDs were formed on the sample with 5 ML $In_{0.22}Ga_{0.78}As$ on Si substrate with the growth temperature of 520 °C, the $In_{0.22}Ga_{0.78}As$ QD thickness of 5 ML, and the density of about 4.5×10^{9} cm^{-2}. The indium segregation is different with temperature. At the lower temperature, the arsenic surface became more stable and adatom diffusion length was reduced to lower mass transport properties. The higher temperature increases diffusion length of the surface species which may improve the segregation of indium to increase the InGaAs QD size and distribution.

Figures 10(a) and 10(b) show the size distribution of the $In_{0.22}Ga_{0.78}As$ QDs on the Si substrate at different temperatures. In Fig. 10(a) the QDs were grown at 480 °C, the grown QDs have an average lateral dot size of around 31 and 7 nm in heights. Figure 10(b). shows the size distribution of the $In_{0.22}Ga_{0.78}As$ QDs/GaAs/Ge/Si substrate grown at 480 °C. The $In_{0.22}Ga_{0.78}As$ QDs grown at 480 °C have an average lateral dot size around 36 nm. Figure 10(c) shows the size distribution of the $In_{0.22}Ga_{0.78}As$ QDs/GaAs/Ge/Si substrate when grown at 520 °C; the $In_{0.22}Ga_{0.78}As$ QDs grown at 520 °C have an average lateral dot size around 75 nm.

IV. CONCLUSIONS

The twins and APBs disappeared at Si substrate with 6° off (100) towards ⟨110⟩ orientation. $In_{0.22}Ga_{0.78}As$ QDs were deposited successfully on Si substrate with Ge buffer layer. From the PL measurement, it shows strong PL intensity with narrow linewidth when InGaAs QDs were formed on Si substrate with 6° off (100) towards ⟨110⟩ orientation. The density of $In_{0.22}Ga_{0.78}As$ dots was estimated to be 1×10^{11} cm^{-2} for the sample with 5 ML thick $In_{0.22}Ga_{0.78}As$ grown at 450 °C, 5×10^{10} cm^{-2} for the sample with 5 ML thick $In_{0.22}Ga_{0.78}As$ grown at 480 °C and 4.5×10^{9} cm^{-2} for the sample with 5 ML thick $In_{0.22}Ga_{0.78}As$ grown at 520 °C. The corresponding average distribution sizes of $In_{0.22}Ga_{0.78}As$ QDs were 31, 36, and 75 nm, respectively. These results indicate that Ge/SiGe/Si strained buffer is a promising method for the fabrication of InGaAs QDs on Si substrate.

ACKNOWLEDGMENTS

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