Physics and Characterization of Various Hot-Carrier Degradation Modes in LDMOS by Using a Three-Region Charge-Pumping Technique

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***Abstract*—Degradation of lateral diffused MOS transistors in various hot-carrier stress modes is investigated. A novel three-region charge-pumping technique is proposed to characterize interface trap (N_{it}) and bulk oxide charge Q_{ox} creation in the channel and in the drift regions separately. The growth rates of N_{it} and Q_{ox} are extracted from the proposed method. A two-dimensional numerical device simulation is performed to gain insight into device degradation characteristics in different stress conditions. This paper shows that a maximum I_g stress causes the largest drain current and subthreshold slope degradation because of both N_{it} generation in the channel and Q_{ox} creation in the bird's beak region. The impact of oxide trap property and location on device electrical characteristics is analyzed from measurement and simulation.**

***Index Terms*—Hot-carrier degradation, lateral diffused MOS (LDMOS), three-region charge pumping (CP).**

I. Introduction

IN RECENT years, multifunction power integrated chips are strongly demanded for the market of portable devices, automotive applications, and display drivers [1]. The integrated bipolar, CMOS, and DMOS (BCD) process has been developed to realize complex single power ICs [2], [3]. Among the candidates of high-voltage devices, lateral diffused MOS (LDMOS) transistors are attractive because they can be easily integrated with standard low-voltage CMOS process [1]–[4]. The LDMOS has been widely used in today's high-voltage and high-current output circuits [4], from a standard 12-V automotive battery [5] to 100-V plasma display panel drivers [6].

One of the major reliability issues in an LDMOS is hot-carrier injection and trapping in the oxide [7]. Various hot-carrier stress modes have been reported. Different stress conditions result in oxide damage of different types (N_{it} and Q_{ox}) and locations (channel or drift region). Moens *et al.* reported that maximum I_B stress results in the worst hot-carrier degradation for a gate oxide thickness from 7 nm [7] to 17 nm [8]. Their studies showed that gate oxide damage occurs in the channel and in the accumulation regions. The device characteristics degradation is attributed to interface trap generation [7], [8]. Hefyene *et al.* [9] and Chen *et al.* [10] claimed that maximum I_g stress has more serious degradation, and again, interface trap generation is the cause of degradation [9], [10]. Since LDMOS degradation is closely dependent on trap type and location, the profiling of trap spatial distribution

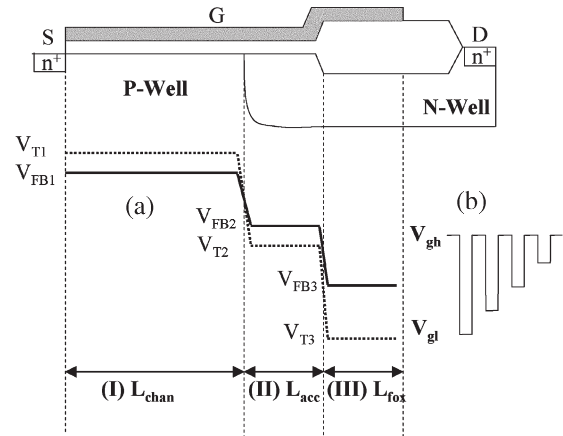

Fig. 1. (a) Cross section of an n-LDMOS and flatband (solid line) and threshold (dash line) voltage distributions. The device is divided into three parts, i.e., 1) L_{chan} (channel region), 2) L_{acc} (accumulation region), and 3) L_{fox} (field oxide region). (b) Illustration of a CP measurement waveform. $V_{\mathrm{gh}} = 12$ V is fixed, and V_{gl} varies from +3.6 to −40 V.

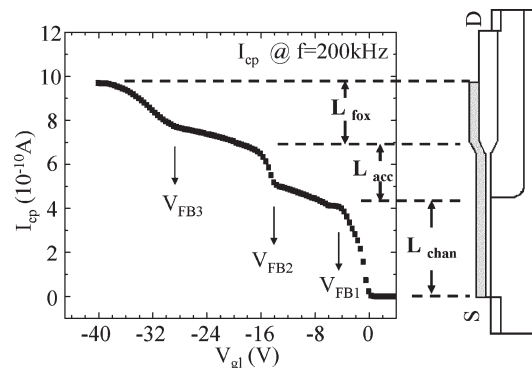

Fig. 2. Typical CP current in an n-LDMOS. The three stages of the CP current correspond to the three regions of the device. The flatband voltage of each region is indicated in the figure. The frequency in CP measurement is fixed at 200 kHz.

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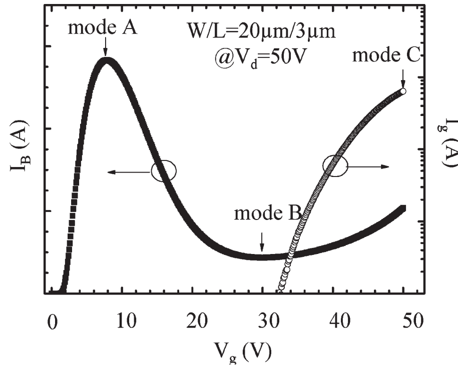

Fig. 3. Substrate current and gate current versus gate voltage in an LDMOS. Three different stress modes are shown in the figure, i.e., 1) mode A (maximum I_b), 2) mode B ($V_g \sim (1/2)V_d$), and 3) mode C (maximum I_g).

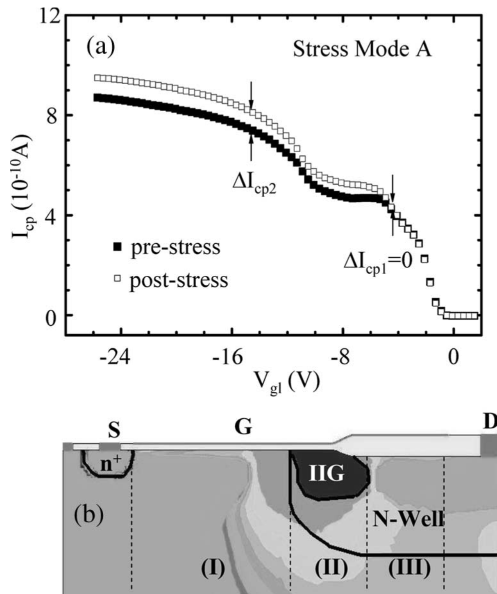

Fig. 4. (a) CP current versus $V_{\rm gl}$ before and after 1400-s mode A stress. (b) 2-D device simulation of IIG distribution in stress mode A.

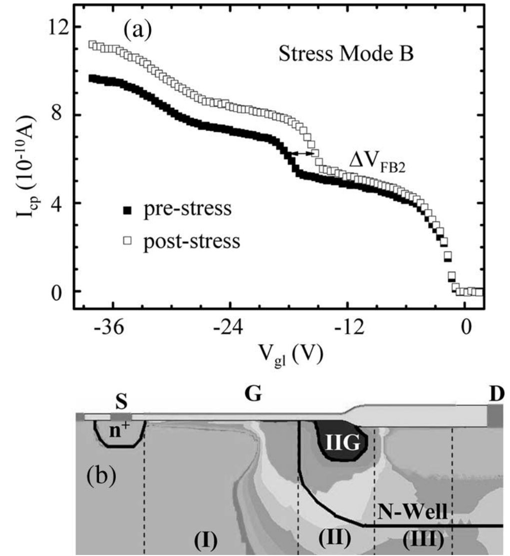

Fig. 5. (a) CP current versus $V_{\rm gl}$ before and after 1400-s mode B stress. The shift of the flatband voltage in stage 2 implies the generation of negative oxide charge in the accumulation region. (b) 2-D device simulation of IIG in stress mode B.

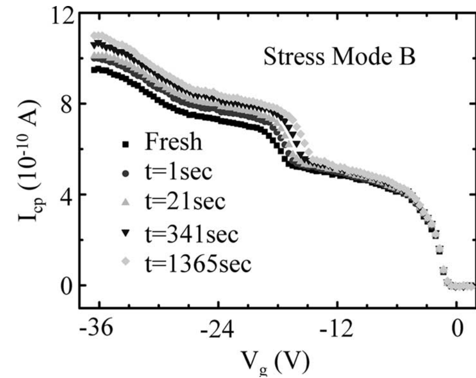

Fig. 6. CP results in stress mode B for different stress times.

and trap behavior is important to the understanding of the impact of various hot-carrier stress modes.

In this paper, we demonstrate a novel three-region charge-pumping (CP) technique to probe hot-carrier stress-induced oxide damage in an LDMOS [11]. Each region of the CP current corresponds to a different part of the device. By comparing the prestress and poststress CP currents in each region, we are able to identify the locations of oxide damage in the device and corresponding trap properties. A two-dimensional (2-D) device simulation is performed to identify an impact ionization generation (IIG) region in the device. The dependence of device degradation characteristic on trap position is also simulated.

II. Three-Region CP Measurement

The n-LDMOS used in this work was processed in a 0.18-μm CMOS technology with a gate oxide thickness of 100 nm and a field oxide thickness of 500 nm. The operation voltages are $V_g = 40$ V and $V_d = 40$ V. Fig. 1(a) shows the device cross section. The device is divided into three regions. Region (I) is the channel region. Regions (II) and (III) are the accumulation region and the field oxide region, respectively. The length of each region is denoted by $L_{\rm chan}(= 3\ \mu{\rm m})$, $L_{\rm acc}$, and $L_{\rm fox}$, respectively. The gate width is 20 μm, and the threshold voltage is 1.5 V. The device flatband voltage ($V_{\rm FB}$, solid line) and threshold voltage (V_T, dash line) distributions of the three regions are illustrated in Fig. 1(a). In the drift region, the flatband voltage is higher than the threshold voltage because of the n-type substrate.

The gate voltage waveform in CP measurement is illustrated in Fig. 1(b) with a fixed $V_{\rm gh} = 12$ V and a variable $V_{\rm gl}$. For the 100-nm-thick gate oxide, we can switch $V_{\rm gl}$ from $+3.6$ to -40 V without a significant gate oxide tunneling current. In this $V_{\rm gl}$ range, all the three regions of the device can be probed. The measurement frequency is 200 kHz. Typical CP measurement result is shown in Fig. 2. The CP current ($I_{\rm cp}$) exhibits three stages, which correspond to the three regions of an n-LDMOS. It should be noticed that each stage has its corresponding threshold and flatband voltages. By measuring the change of $I_{\rm cp}$ and $V_{\rm FB}$ after stress in each stage, we are able to separate $N_{\rm it}$ and $Q_{\rm ox}$ in each region of the

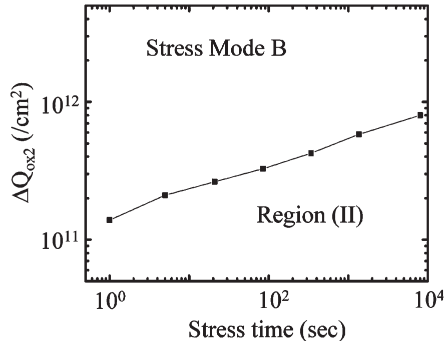

Fig. 7. Region (II) oxide-trapped charge growth rate in stress mode B.

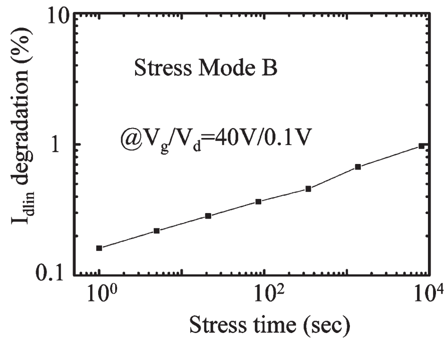

Fig. 8. Linear drain current degradation (I_{dlin}) rate measured at $V_g/V_d =$ 40 V/0.1 V in stress mode B.

device [11], e.g., $\Delta N_{\mathrm{it}}(\text{channel}) = \Delta I_{\mathrm{cp}}(\text{stage 1})/qfWL_{\mathrm{chan}}$, $\Delta Q_{\mathrm{ox}}(\text{acc}) = \Delta V_{\mathrm{FB}}$ (stage 2) $\cdot C/q$, and so on.

Three hot-carrier stress modes, i.e.: 1) mode A (maximum I_b); 2) mode B ($V_g \sim (1/2)V_d$); and 3) mode C (maximum I_g), are investigated. The I_g–V_g and I_b–V_g of an n-LDMOS are shown in Fig. 3. The maximum I_b (mode A) stress is applied at $V_g/V_d = 8$ V/50 V, whereas the maximum I_g (mode C) stress is applied at $V_g/V_d = 50$ V/50 V. The bias conditions of the three stress modes are also indicated in Fig. 3. For each stress mode, the three-region CP method is performed to investigate trap type (N_{it} or Q_{ox}) and growth characteristics. Subthreshold slope and linear drain current (I_{dlin}) are measured to monitor device degradation.

III. Results and Discussion

A. Maximum I_b Stress Mode

Fig. 4(a) shows the I_{cp} in a fresh device and after 1400-s maximum I_b stress. The poststress I_{cp} in the first stage is nearly the same as the prestress one, indicating that region (I) oxide is not damaged by the stress. The poststress I_{cp} in stage 2, however, exhibits an upward shift, while the flatband voltage remains the same (no rightward shift in the I_{cp}). This feature suggests N_{it} generation in region (II) but no Q_{ox} creation. Numerical device simulation also shows the maximum IIG rate in region (II) [Fig. 4(b)]. Although interface trap generation is observed from the I_{cp}, the subthreshold swing of the device is not degraded because the generated N_{it} is distributed in region (II) rather than in the channel region. In addition, I_{dlin} degradation is not observed either.

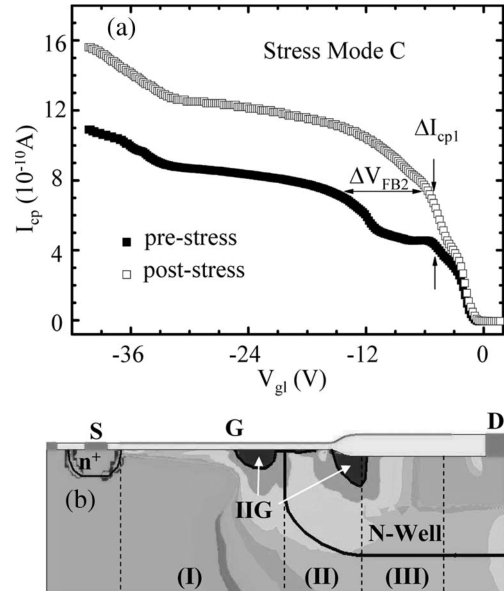

Fig. 9. (a) CP current before and after 1000-s mode C stress. Upward shift in first-stage I_{cp} indicates interface trap generation in the channel, and rightward shift in second-stage I_{cp} implies oxide charge creation in the accumulation region. (b) 2-D device simulation of IIG distribution in stress mode C. Two IIG regions are found: One is in the channel region, and the other is in the accumulation region.

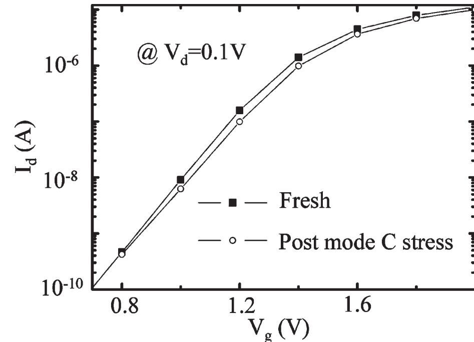

Fig. 10. Subthreshold characteristics before and after mode C stress. The swing degradation is attributed to interface trap generation in the channel region.

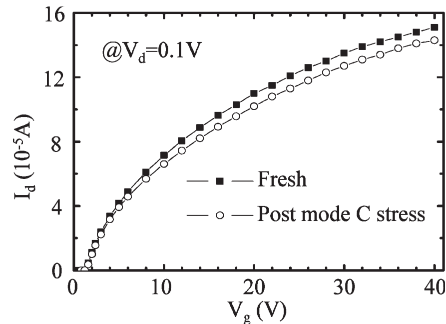

Fig. 11. The linear drain current versus V_g before and after mode C stress.

B. $V_g \sim$ (1/2) V_d Stress Mode

The I_{cp} results before and after mode B stress (at $V_g/V_d =$ 30 V/50 V) are shown in Fig. 5(a). N_{it} generation in stress mode B is relatively small and can be realized due to a smaller

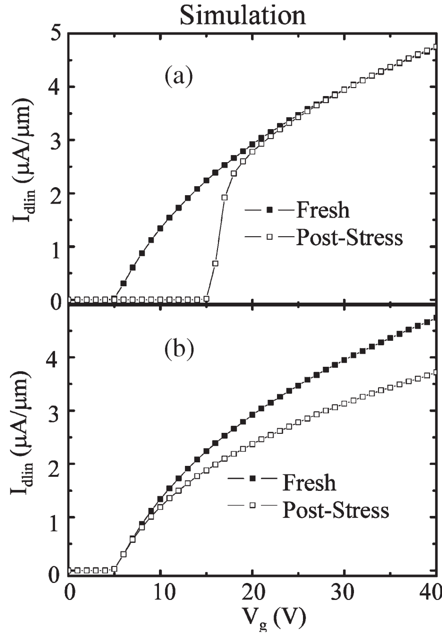

Fig. 12. Simulated drain current versus gate voltage without and with oxide charges. (a) Oxide charge is placed in the channel. (b) Oxide charge is placed in the bird's beak region.

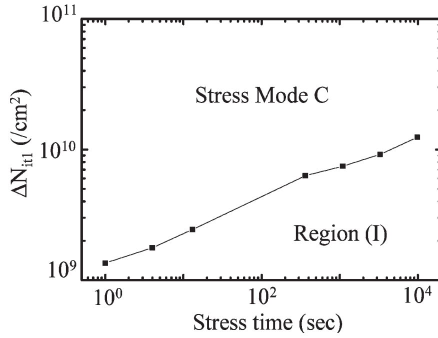

Fig. 13. Region (I) interface trap growth rate in stress mode C.

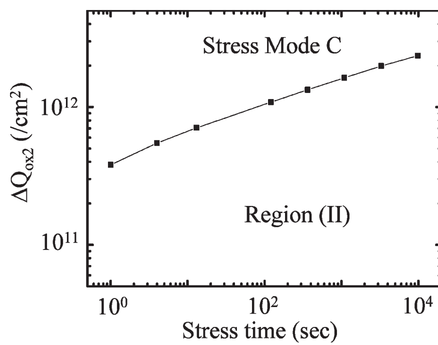

Fig. 14. Region (II) oxide charge growth rate in stress mode C.

substrate current [and a smaller IIG region in Fig. 5(b)], as compared to stress mode A. Unlike stress mode A, a distinct flatband voltage shift in region (II) is noticed, which is manifested by a rightward shift of the $I_{\rm cp}$ in stage 2. An arrow is drawn in Fig. 5(a) to indicate the flatband voltage shift ($\Delta V_{\rm FB2}$). The rightward shift of the slope is caused by negative $Q_{\rm ox}$ creation in region (II). Fig. 6 shows the evolution of the $I_{\rm cp}$ with

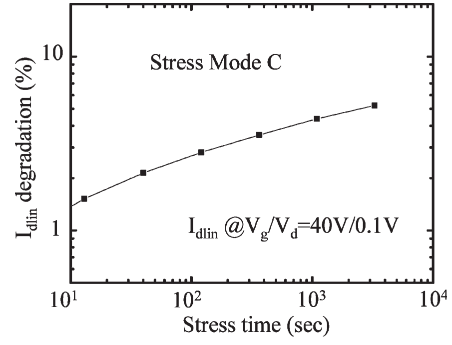

Fig. 15. $I_{\rm dlin}$ degradation versus stress time in stress mode C. The degradation is mainly caused by negative oxide creation in the drift region.

TABLE I
SUMMARY OF MAJOR OXIDE AND DEVICE PERFORMANCE DEGRADATIONS IN VARIOUS STRESS MODES

mode	A	B	C	
Trap Location	Region (II)	Region (II)	Region (II)	Region (I)
Trap Property	N_{it}	Q_{ox}	Q_{ox}	N_{it}
Device Degradation	N/A	I_{dlin}	I_{dlin}	$I_{subthreshold}$

stress time. As stress time increases, the flatband voltage of the region (II) continuously shifts to the right. The $Q_{\rm ox2}$ generation rate (Fig. 7) can be extracted from the $\Delta V_{\rm FB2}$ versus stress time by using the equation in Section II. Because of negative $Q_{\rm ox}$ creation, the resistance beneath the bird's beak increases. At a large V_g, region (I) resistance is relatively small, and the resistance in the bird's beak region occupies a larger part of the total resistance. Thus, $I_{\rm dlin}$ degradation is observable at a higher measurement $V_g = 40$ V (Fig. 8). Numerical simulation for the dependence of $I_{\rm dlin}$ degradation on trap location will be given later.

C. Maximum I_g Stress Mode

Fig. 9(a) shows the $I_{\rm cp}$ result before and after maximum I_g stress for 1000 s. Two different stress-induced oxide degradation mechanisms are noticed: One is $N_{\rm it}$ generation in region (I), and the other is negative $Q_{\rm ox}$ creation in region (II). These two trap creation processes are reflected by an upward shift of the first-stage $I_{\rm cp}$ denoted by $\Delta I_{\rm cp1}$ and by a rightward shift of the second-stage $I_{\rm cp}$ [$\Delta V_{\rm FB2}$ in Fig. 9(a)]. In contrast to stress mode A, a 2-D device simulation reveals that the IIG region in maximum I_g stress splits into two parts [Fig. 9(b)]: One is in the channel [region (I)], and the other is underneath the bird's beak. The $N_{\rm it}$ generation in region (I) results in a significant subthreshold swing degradation (Fig. 10) in stress mode C. In addition, $Q_{\rm ox2}$ creation accounts for a serious $I_{\rm dlin}$ degradation (Fig. 11) in mode C. Fig. 11 shows that the $I_{\rm dlin}$ degradation is more apparent at a larger V_g. To explain the V_g dependence, a 2-D device simulation is performed. We calculate the $I_{\rm dlin}$ versus V_g by placing the same amount of fixed oxide charge ($Q_{\rm ox}/q = 10^{19}/{\rm cm}^3$) in the channel [Fig. 12(a)] and in the bird's beak region [Fig. 12(b)]. Fig. 12(a) shows a larger $I_{\rm dlin}$ degradation at a low V_g, whereas Fig. 12(b) shows a

larger I_{dlin} degradation at a high V_g. The trend in Fig. 12(b) agrees with our measured result (Fig. 11), and thus, we can conclude that the created Q_{ox} is in region (II).

The N_{it1} and Q_{ox2} growth rates in stress mode C are shown in Figs. 13 and 14, respectively. The growth rate obeys a power-law time dependence, and the power factor is around 0.25, which is in agreement with [12]. Comparing to modes A and B, the larger Q_{ox2} growth rate in mode C is attributed to a larger stress gate current (or a higher stress gate voltage). The I_{dlin} degradation rate is shown in Fig. 15. Stress mode C has the worst I_{dlin} degradation. Due to oxide charge creation in region (II), region (II) resistance increases, and the current flow in region (II) is pushed deeper. Consequently, the electron mobility exhibits a saturated effect, and thus, I_{dlin} degradation has a tendency to saturate in Fig. 15. This mobility saturation model is also described in [13] and [14] for MOSFET and in [8] for LDMOS structure. The LDMOS degradation behavior and trap properties in the three stress modes are summarized in Table I.

IV. Conclusion

A novel three-region CP technique has been developed to characterize hot-carrier stress-induced oxide degradation in each region of an n-LDMOS. The trap location and property in various stress modes are identified, and their impact on device characteristics has been analyzed. A correlation between device degradation and CP and device simulation results has been established. Our study reveals that the device subthreshold swing degradation is mainly affected by interface traps in the channel region, whereas the linear drain current degradation is dictated by oxide-trapped charge in the drift region. Our study also shows that maximum I_g stress results in the worst hot-carrier degradation in an LDMOS, which is attributed to both N_{it} generation in the channel region and Q_{ox} generation in the bird's beak region.

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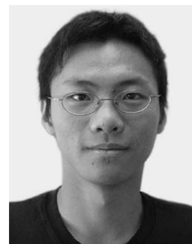

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