Overview and Design of Mixed-Voltage I/O Buffers With Low-Voltage Thin-Oxide CMOS Transistors

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Abstract—Overview on the prior designs of the mixed-voltage I/O buffers is provided in this work. A new 2.5/5-V mixed-voltage I/O buffer realized with only thin gate-oxide devices is proposed. The new proposed mixed-voltage I/O buffer with simpler dynamic n-well bias circuit and gate-tracking circuit can prevent the undesired leakage current paths and the gate-oxide reliability problem, which occur in the conventional CMOS I/O buffer. The new mixed-voltage I/O buffer has been fabricated and verified in a 0.25-μm CMOS process to serve 2.5/5-V I/O interface. Besides, another 2.5/5-V mixed-voltage I/O buffer without the subthreshold leakage problem for high-speed applications is also presented in this work. The speed, power consumption, area, and noise among these mixed-voltage I/O buffers are also compared and discussed. The new proposed mixed-voltage I/O buffers can be easily scaled toward 0.18-μm (or below) CMOS processes to serve other mixed-voltage I/O interfaces, such as 1.8/3.3-V interface.

Index Terms—Gate-oxide reliability, gate-tracking circuit, interface, mixed-voltage I/O buffer.

I. INTRODUCTION

THE device dimension of transistor has been scaled toward the nanometer region and the power-supply voltage of chips in the nanoscale CMOS technology has been also decreased [1]. Obviously, the shrunk device dimension makes the chip area smaller to save silicon cost. The lower power-supply voltage (VDD) results in lower power consumption. Therefore, chip design quickly migrates to the lower voltage level with the advancement of the nanoscale CMOS technology. However, some peripheral components or other integrated circuits (ICs) in an electronic system are still operated at the higher voltage levels, such as 3.3 or 5 V [2]–[4]. In other words, an electronic system could have chips operated at different voltage levels. In order to interface these chips with different voltage levels, the conventional I/O buffer is unsuitable anymore. Several problems arise in the I/O interface between these ICs, such as the gate-oxide reliability [5]–[7], the hot-carrier degradation [8], and the undesirable leakage current paths [9], [10].

The conventional tri-state I/O buffer with 2.5-V gate-oxide devices in a 0.25-μm CMOS process is shown in Fig. 1, where the power-supply voltage (VDD) is 2.5 V. However, the input
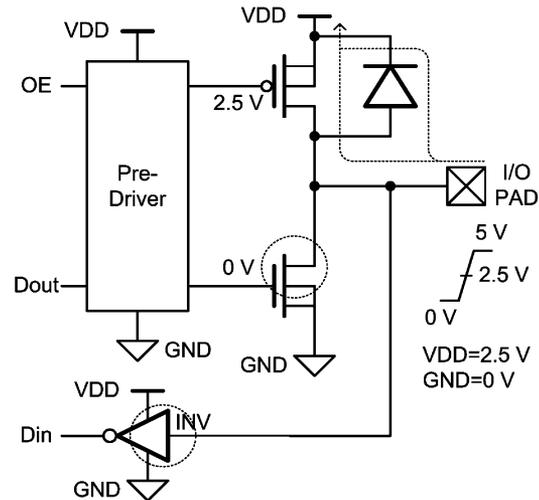
Fig. 1. Conventional tri-state I/O buffer in a 0.25-μm CMOS process that will suffer the circuit leakage and gate-oxide reliability issue in the mixed-voltage I/O interface.

signal at the I/O pad in the mixed-voltage I/O interface may rise up to 5 V in the tri-state input (receive) mode. In the receive mode, the gate voltages of the pull-up pMOS device and the pull-down nMOS device of the I/O buffer are traditionally controlled at 2.5 V and 0 V to turn off the pull-up pMOS device and the pull-down nMOS device by the pre-driver circuit, respectively. When the input signal at the I/O pad rises up to 5 V in the tri-state input mode, the parasitic drain-to-well pn-junction diode in the pull-up pMOS device will be forward biased. Therefore, an undesired leakage current path flows from the I/O pad to the power-supply voltage (VDD) through the parasitic pn-junction diode. Besides, because the gate voltage of the pull-up pMOS device is 2.5 V and the input signal at I/O pad is 5 V, the pull-up pMOS device will be turned on in such tri-state input mode to conduct another undesired leakage current path from the I/O pad to the power-supply voltage (VDD). Such undesired leakage currents cause not only more power consumption in the electronic system but also malfunction in the whole system.

Moreover, because the gate–drain voltage of the pull-down nMOS device and the gate–source voltage of the input buffer in Fig. 1 with 5-V input signal are larger than their voltage levels in the normal operation, such high voltage across the thin gate oxide of the pull-down nMOS device and the input buffer results in the gate-oxide reliability issue [5]–[7]. Besides, the pull-down nMOS device and the input buffer with a 5-V input signal may suffer serious hot-carrier degradation if their drain–source voltages are too large [8].

Fig. 2. Mixed-voltage I/O buffer with dual-oxide option and an external n-well bias.

Fig. 3. Basic design concept for mixed-voltage I/O buffer realized with only thin-oxide devices.

Fig. 2 shows the mixed-voltage I/O buffer with dual-oxide (thick-oxide and thin-oxide) devices and an external n-well bias voltage. For such mixed-voltage interface applications, the dual-oxide process provided by foundry is used to avoid the gate-oxide reliability problem [11]–[13]. Since the thick oxide can sustain higher gate voltage, the devices which have the gate-oxide reliability problem can be replaced by the thick-oxide devices to prevent the high-voltage overstress on the thin gate oxide. Therefore, the core circuits are designed with thin-oxide devices to decrease the chip area and power consumption, but the I/O circuits are designed with thick-oxide devices to avoid the gate-oxide reliability issue. In order to avoid leakage current path from the I/O pad to the power supply (VDD) through the parasitic drain-to-well pn-junction diode in the pull-up pMOS device, the body terminal of the pull-up pMOS must be connected to an extra pad that provides a higher external voltage (VDDH) to bias the body of the pull-up pMOS device. In addition, a gate-tracking circuit is needed to avoid the leakage current path induced by the incorrect conduction of the pull-up pMOS device.

Although the traditional mixed-voltage I/O buffer with dual-oxide devices and an external n-well bias can be used to solve the aforementioned problems, there are still some limitations in this I/O buffer. Using an external bias voltage needs an extra pad and another power supply (VDDH), the silicon area and the cost of the whole system are increased. The threshold voltage of the thick-oxide devices is so high that their driving capacities are decreased when their gates are controlled by the pre-driver circuit with low-voltage devices. In addition, because the body terminal of the pull-up pMOS device is connected to a higher voltage (VDDH), the threshold voltage of the pull-up pMOS device is also increased due to the body effect. Because the driving capacity is decreased, the larger device dimension is needed for the pull-up pMOS device to support the desired driving specifications. In turn, it increases the silicon area for such I/O buffer. Therefore, the mixed-voltage I/O buffer with dual-oxide devices and an external n-we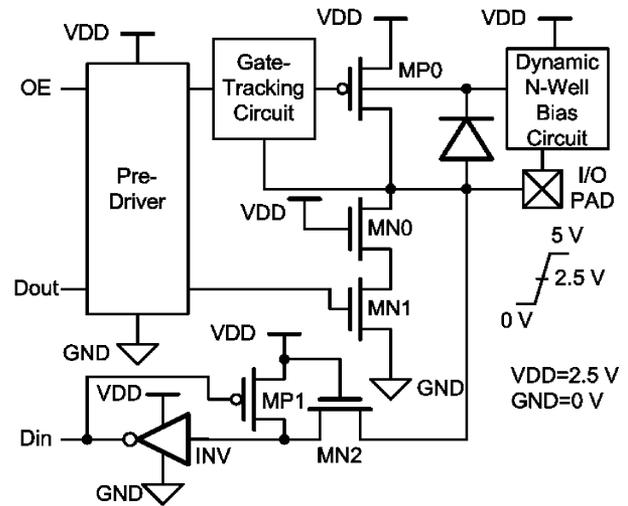ll bias is unsuitable for the low-cost commercial ICs. Considering these limitations, several mixed-voltage I/O buffers have been reported in [14]–[18], which are overviewed in this paper.

In this work, two new proposed mixed-voltage I/O buffers with the dynamic n-well bias circuit and gate-tracking circuit are realized with the thin-oxide devices. This new proposed mixed-voltage I/O buffer 1 has been successfully verified without the gate-oxide reliability problem in a 0.25-μm 2.5-V CMOS process [19]. In addition, the new proposed 2.5/5-V mixed-voltage I/O buffer without the gate-oxide reliability problem and excessive leakage problem for high-speed applications is also presented in this paper.

II. OVERVIEW ON THE PRIOR DESIGNS OF MIXED-VOLTAGE I/O BUFFERS

A. Design Concept

Fig. 3 shows the mixed-voltage I/O buffer realized with thin-oxide devices, a dynamic n-well bias circuit, and a gate-tracking circuit [10], [14]–[18]. The stacked nMOS devices, MN0 and MN1, are used to avoid the high-voltage overstress on their gate oxide. In a 0.25-μm CMOS process, the power-supply voltage (VDD) is 2.5 V and the threshold voltage of the devices is about 0.6 V. Because the gate terminal of transistor MN0 is connected to 2.5 V (VDD), the drain voltage of transistor MN1 is about 1.9 V $(2.5 - 0.6 = 1.9)$ when the input signal at the I/O pad is 5 V in the tri-state input mode. Hence, the gate–drain voltages and the gate–source voltages of the stacked nMOS devices, MN0 and MN1, are limited below 2.5 V even if the input signal at the I/O pad is 5 V. Therefore, the stacked nMOS devices, MN0 and MN1, can solve the gate-oxide reliability problem.

The gate-tracking circuit shown in Fig. 3 is used to prevent the leakage current path due to the incorrect conduction of the pull-up pMOS device when the input signal is higher than VDD. In the transmit mode, the gate-tracking circuit must transfer the signal from the pre-driver circuit to the gate terminal of the pull-up pMOS device exactly. In the tri-state input mode (receive mode) with 5-V input signal, the gate-tracking circuit will

charge the gate terminal of the pull-up pMOS device to 5 V to turn off the pull-up pMOS device completely, and to avoid the leakage current from the I/O pad to the power supply (VDD). On the contrary, the gate-tracking circuit will keep the gate terminal of the pull-up pMOS device at 2.5 V to turn off the pull-up pMOS device completely, and to prevent the overstress on the gate oxide of the pull-up pMOS device, when the input signal at the I/O pad is 0 V in the tri-state input mode.

The dynamic n-well bias circuit shown in Fig. 3 is designed to prevent the leakage current path due to the parasitic drain-to-well pn-junction diode in the pull-up pMOS device. In the transmit mode, the dynamic n-well bias circuit must keep the floating n-well bias at 2.5 V. So, the threshold voltage of the pull-up pMOS device isn't increased by the body effect. In the tri-state input mode with a 5-V input signal, the dynamic n-well bias circuit will charge the floating n-well to 5 V to prevent the leakage current from the I/O pad to the power supply (VDD) through the parasitic pn-junction diode. When the input signal at the I/O pad is 0 V, the dynamic n-well bias circuit will bias the floating n-well at 2.5 V.

Because the floating n-well is clamped to 2.5 V or 5 V through the parasitic diodes by some dynamic n-well bias circuits [14], [15], [17], the voltage on the floating n-well will be a little lower than 2.5 V or 5 V. The lower floating n-well voltage results in the lower threshold voltage of the pull-up pMOS transistor. Thus, the subthreshold leakage current becomes large when the pull-up pMOS transistor is in off state. If the given process has serious subthreshold leakage issue, such as the 0.13-μm or below processes, the dynamic n-well bias circuit must clamp the floating n-well directly to the desired voltage level by the MOS transistor to decrease the subthreshold leakage.

As shown in Fig. 3, the extra transistors, MN2 and MP1, are added in the input buffer. Transistor MN2 is used to limit the voltage level of input signal reaching to the gate oxide of inverter INV. Because the gate terminal of transistor MN2 is connected to the power-supply voltage (VDD), the input terminal of inverter INV will rise up to 1.9 V $(2.5 - 0.6 = 1.9)$ when the input signal at the I/O pad is 5 V in the tri-state input mode. Then, transistor MP1 is used to pull up the input node of inverter INV to 2.5 V when the output node of inverter INV is pulled down to 0 V. Therefore, the gate-oxide reliability problem of the input buffer can be solved.

B. Prior Designs of Mixed-Voltage I/O Buffers

Fig. 4 re-draws the mixed-voltage I/O buffer with stacked pull-up pMOS devices [14]. Signal OE is the output-enable control signal. In the transmit mode, transistor MN1 is turned on and transistor MP2 is turned off, so that this I/O buffer drives the I/O pad according to the output signal Dout. In the tri-state input mode, transistor MN1 is turned off and transistor MP2 is turned on by the control signal OE at logic zero. If the input signal at the I/O pad is 5 V, the gate voltage of transistor MP1 and the floating n-well are pulled up to 5 V through transistor MP2 and the parasitic drain-to-well pn-junction diode in transistor MP0 to prevent the undesired leakage current paths from I/O pad to power-supply voltage (VDD), respectively. Although this I/O buffer is simple, transistors MN0, MN1, and MP2 have the gate-oxide reliability problem in the tri-state input mode when
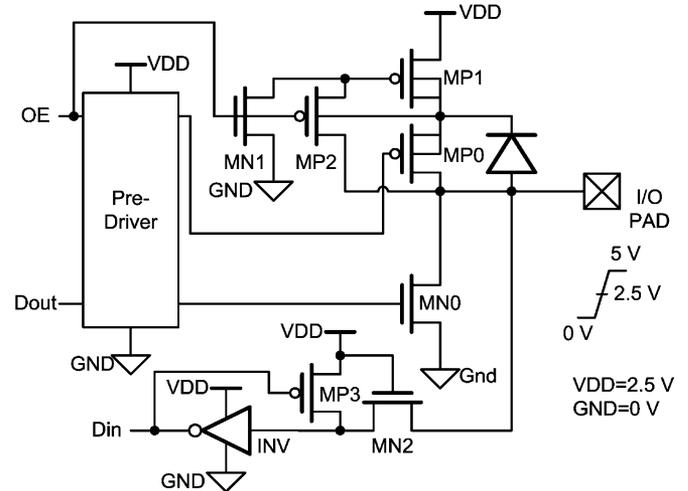
Fig. 4. Mixed-voltage I/O buffer with stacked pull-up pMOS devices [14].
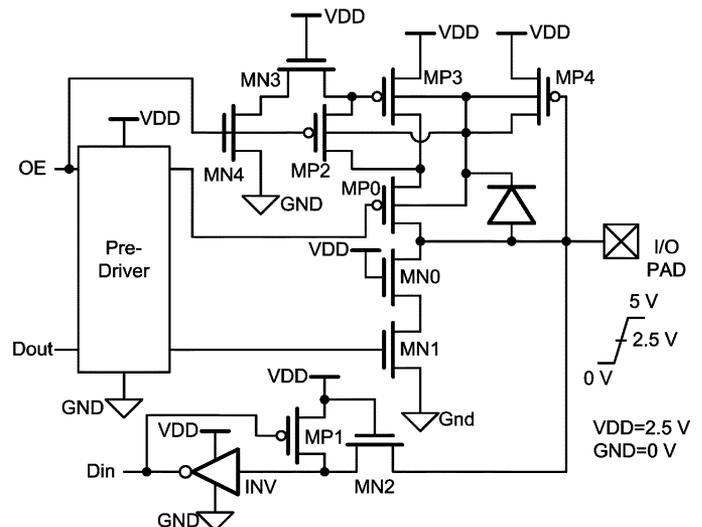
Fig. 5. Mixed-voltage I/O buffer with stacked pull-up pMOS devices and stacked pull-down nMOS devices [15].

the input signal has a 5-V voltage level. Besides, because the stacked pMOS devices with the floating n-well to prevent the leakage current is applied to this I/O buffer, the pMOS devices in stacked configuration occupy more silicon area.

Fig. 5 re-draws another mixed-voltage I/O buffer with stacked pull-up pMOS devices and stacked pull-down nMOS devices [15]. This I/O buffer uses transistors MP2, MN3, and MN4 as the gate-tracking circuit and transistors MP0, MP3, and MP4 as the dynamic n-well bias circuit. In the tri-state input mode with the control signal OE at GND, transistor MN4 is turned off and transistor MP2 is turned on. If the input signal at the I/O pad is 5 V, the gate voltage of transistor MP3 is biased at 5 V through transistors MP0 and MP2 to avoid the undesired leakage current path due to the incorrect conduction of transistor MP3. The floating n-well is biased at ~5 V through the parasitic drain-to-well pn-junction diode of transistor MP0. In the transmit mode with the OE control signal at VDD, transistor MN4 is turned on so that transistor MP3 is turned on, and transistor MP2 is kept off. Hence, this I/O buffer drives the

Fig. 6. Mixed-voltage I/O buffer with a depletion pMOS device MP2 [16].

Fig. 7. Mixed-voltage I/O buffer realized with only thin-oxide devices [17].

I/O pad according to the output signal Dout. When the signal at the I/O pad is 0 V, the floating n-well is biased at 2.5 V through transistor MP4. When the input signal at the I/O pad is 2.5 V, the floating n-well is biased at ∼2.5 V through the parasitic source-to-well pn-junction diodes of transistors MP3 and MP4. However, transistor MP2 has the gate-oxide reliability problem when the input signal at the I/O pad is 5 V in the tri-state mode. Besides, because the I/O buffer uses two pMOS devices, MP0 and MP3, in stacked configuration to drive the I/O pad, the stacked devices occupy more silicon area.

The mixed-voltage I/O buffer with a depletion pMOS device is re-drawn in Fig. 6 [16]. The depletion pMOS device MP2 in the I/O buffer is used as the gate-tracking circuit. In the tri-state mode, if the input signal at I/O pad is 5 V, the gate voltage of transistor MP0 is biased at 5 V through the depletion pMOS device MP2 to avoid the undesired leakage current path through the transistor MP0. This I/O buffer uses an extra pad that is connected to 5-V power supply (VDDH) to avoid the undesired leakage current path through the parasitic drain-to-well pn-junction diode. However, using the depletion device increases mask layer and process modification. Thus, the fabrication cost of such I/O buffer design will be increased. In addition, using the extra n-well bias (VDDH) not only degrades the driving capacity of output device MP0 due to the body effect, but also increases the system cost.

Fig. 7 re-draws the mixed-voltage I/O buffer realized with only thin-oxide devices reported in [17]. In Fig. 7, the gate-tracking circuit and the dynamic n-well bias circuit are formed by transistors MP1, MP2, MP3, MP4, MN2, MN3, MN4, and MN5. In the transmit mode with signal OE at logic "1", transistor MN4 is turned on to keep transistors MP3 and MP4 on. Thus, this I/O buffer drives the I/O pad according to signal Dout. Besides, because transistor MP3 is turned on, the floating n-well is biased at 2.5 V by transistor MP3 in the transmit mode. In the tri-state input mode with signal OE at logic "0", transistor MN4 is kept off. If the input signal at the I/O pad is 5 V, the gate voltages of transistors MP0 and MP4 are biased at 5 V through transistor MP1 and MP2 to avoid the undesired

Fig. 8. Mixed-voltage I/O buffer realized with only thin-oxide devices [18].

leakage paths through the transistors MP0 and MP4. Besides, the floating n-well is also biased at ∼5 V to avoid the undesired leakage path through the parasitic drain-to-well pn-junction diode of transistor MP0 when the voltage at the I/O pad is 5 V in tri-state input mode. When the input signal at the I/O pad is 0 V in the tri-state input mode, transistor MN3 is turned on to keep transistor MP3 on. So, the floating n-well is biased at 2.5 V.

Another mixed-voltage I/O buffer realized with only thin-oxide devices is re-drawn in Fig. 8, [18]. The gate-tracking circuit in Fig. 8 is composed of transistors MN3, MN4, MP2, MP3, and MP4. The dynamic n-well bias circuit in Fig. 8 is formed by transistors MN5, MP5, MP6, and MP7. Besides, the body terminals of all pMOS transistors in the gate-tracking circuit and the dynamic n-well bias circuit are connected to the floating n-well. Such I/O circuit shown in Fig. 8 can overcome the gate-oxide
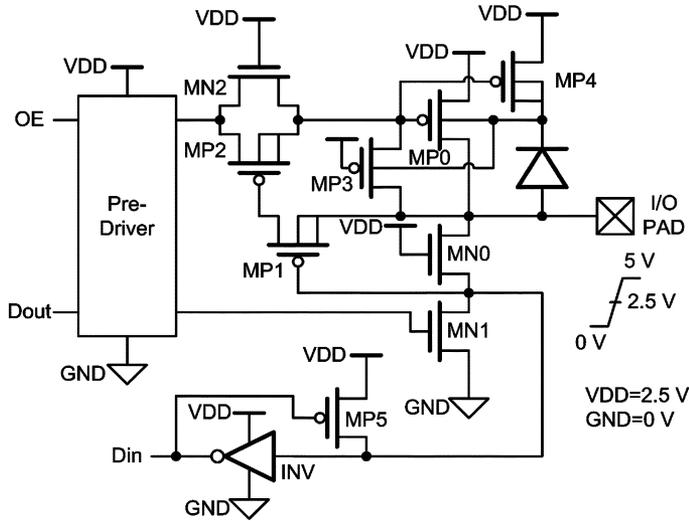
Fig. 9.   New proposed mixed-voltage I/O buffer 1 with only thin-oxide devices.

reliability problem and avoid the undesired leakage paths. However, too many devices are used to realize the desired functions of the gate-tracking circuit and the dynamic n-well bias circuit. More devices used in the mixed-voltage I/O buffer often cause more complex metal routing connection in the I/O cells.

III. NEW MIXED-VOLTAGE I/O BUFFERS

A. New Mixed-Voltage I/O Buffer 1

Fig. 9 shows the new proposed mixed-voltage I/O buffer with the new dynamic n-well bias circuit and gate-tracking circuit. The new proposed I/O buffer is realized with only the thin gate-oxide devices, and occupies smaller silicon area than the prior designs of mixed-voltage I/O buffers. When the tri-state control signal OE is at 2.5 V (logic "1"), the I/O buffer is operated in the transmit mode. The signal at the I/O pad rises or falls according to signal Dout, which is controlled by the internal circuits of IC. The lower output port of the pre-driver circuit is directly connected to the gate terminal of the pull-down nMOS device, MN1. The upper output port of the pre-driver circuit is connected to the gate terminal of the pull-up pMOS device, MP0, through the gate-tracking circuit. If the voltage level at the upper port is 0 V, the signal can be fully transmitted to the gate terminal of the pull-up pMOS device MP0 through transistor MN2, and the signal at the I/O pad is pulled up to 2.5 V. Besides, transistor MP4 is also turned on to bias the floating n-well at 2.5 V. When the voltage level at the upper port is 2.5 V, the gate terminal of transistor MP0 is charged to $\text{VDD} - |\text{Vtp}|$ through transistor MN2 first. Consequently, the voltage at the I/O pad and the gate voltage of transistor MP1 are discharged to 0 V through transistors MN0 and MN1. Transistor MP1 is turned on until the gate terminal of transistor MP2 is discharged to $|\text{Vtp}|$. At this moment, transistor MP2 is turned on to continually pull the gate voltage of transistor MP0 up to 2.5 V. The pull-up pMOS device MP0 can be completely kept off. The floating n-well is also biased at ~2.5 V through the parasitic pn-junction diodes of transistors MP0 and MP4 at this moment.

When the proposed I/O buffer is operated in the tri-state input (receive) mode, the upper and lower output ports of the pre-

driver circuit are kept at 2.5 V and 0 V, respectively, to turn off transistors MP0 and MN1. Signal Din rises or falls according to the signal at the I/O pad in the tri-state input mode. In order to prevent the undesired leakage current from the I/O pad to the power supply (VDD) through the pull-up pMOS device MP0, transistor MP3 is used to track the signal at the I/O pad and to control the gate voltage of transistor MP0. When the voltage level at the I/O pad exceeds $\text{VDD} + |\text{Vtp}|$, such as 5 V, transistor MP3 is turned on to charge the gate terminal of transistor MP0 up to 5 V. Transistor MP0 is completely turned off to prevent the leakage current through its channel. Transistor MP4 is also turned off and the floating n-well is biased at 5 V through the parasitic pn-junction diode. Thus, there is no leakage current path from the I/O pad to the power supply (VDD). Besides, transistor MP1 is also turned on to keep transistor MP2 off in order to prevent another leakage path from the gate terminal of transistor MP0 to the upper port of the pre-driver, when the signal at the I/O pad is 5 V.

Transistors MN0 and MP5 with inverter INV are used to transfer the input signal from the I/O pad to the internal node Din in the tri-state input mode. Transistor MN0 is used to limit the voltage level of input signal reaching to the gate oxide of inverter INV. Because the gate terminal of transistor MN0 is connected to the power-supply voltage (2.5 V), the input voltage of inverter INV is limited to 1.9 V $(2.5 - 0.6 = 1.9)$ when the voltage level at the I/O pad is 5 V. Then, transistor MP5 will pull the input node of inverter INV up to 2.5 V when the output node of inverter INV is pulled down to 0 V. The signal at the I/O pad can be successfully transferred to the internal input node Din. This I/O buffer can be correctly operated with neither gate-oxide reliability problem nor any circuit leakage issue in the tri-state input mode.

A 0.25-μm 2.5-V CMOS device model is used to verify the design of the new proposed mixed-voltage I/O buffer by HSPICE simulation. Fig. 10(a) and (b) shows the simulated waveforms of the new proposed mixed-voltage I/O buffer with a 20-pF output load at the pad and 50-MHz I/O signal in the transmit mode and in the tri-state input mode, respectively. As shown in Fig. 10(a), the new proposed mixed-voltage I/O buffer can successfully drives the I/O pad according to signal Dout in the transmit mode. As shown in Fig. 10(b), the new proposed mixed-voltage I/O buffer can successfully transfer the signal at the I/O pad to the signal Din when it receives the 5-V signals in the tri-state input mode. This simulation also verifies that the gate–drain voltages (Vgd) and gate–source voltages (Vgs) of all devices in the new proposed mixed-voltage I/O buffer do not exceed 2.5 V. Fig. 10(b) only shows the gate–drain voltage (Vgd) of the pull-up pMOS device MP0. With the new gate-tracking circuit, the Vgd of the pull-up pMOS device MP0 is always controlled within the normal operation voltage (VDD). Thus, the gate-tracking circuit can solve the gate-oxide reliability problem in the new proposed mixed-voltage I/O buffer.

Fig. 11 shows the die photograph of the new proposed mixed-voltage I/O buffer fabricated in a 0.25-μm 2.5-V 1P5M CMOS process. The measured waveforms of the new proposed mixed-voltage I/O buffer with 1-MHz I/O signal in the transmit mode, the tri-state input mode with 2.5-V input, and
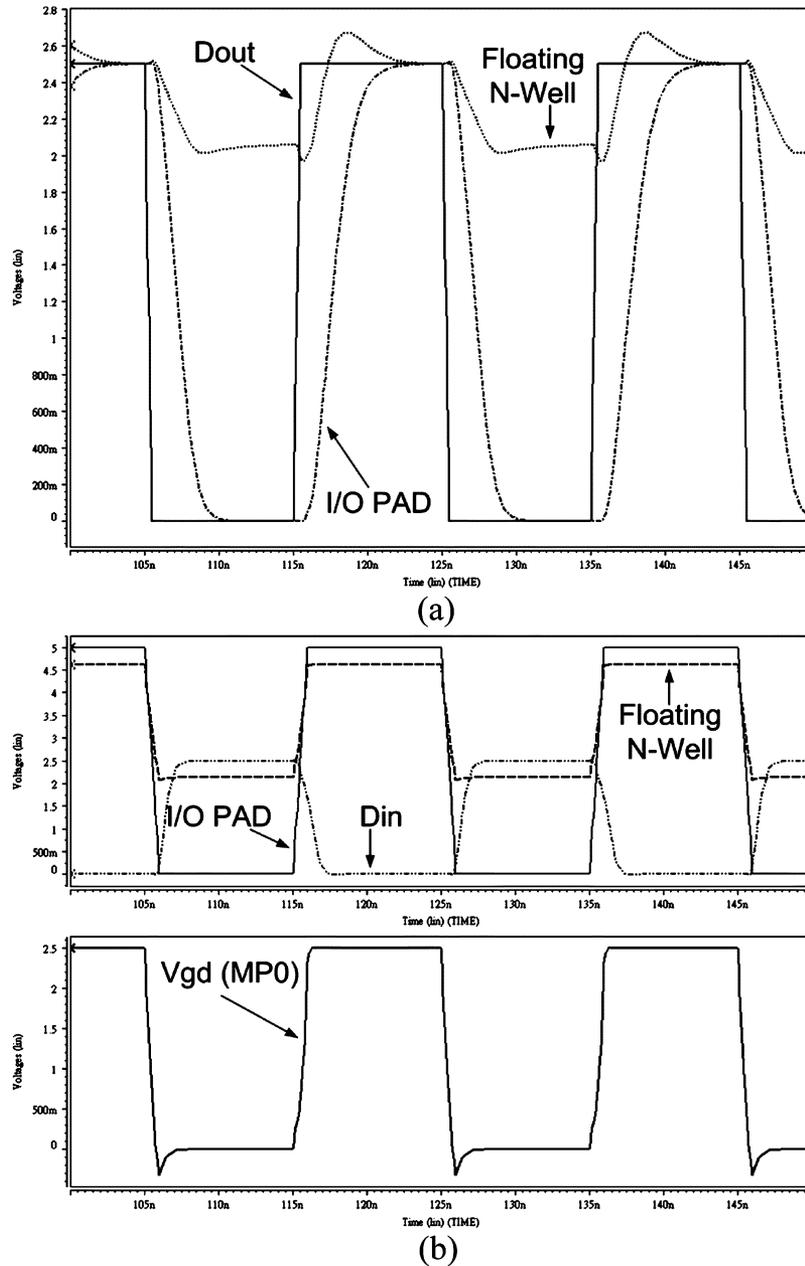
Fig. 10. Simulated waveforms of the new proposed mixed-voltage I/O buffer 1 with a 20-pF load and 50-MHz I/O signal in (a) the transmit mode, and (b) the tri-state (receive) mode.
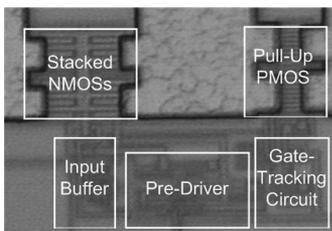

Fig. 11. Die photograph of the new proposed mixed-voltage I/O buffer 1 fabricated in a 0.25-μm 2.5-V CMOS process.

the tri-state input mode with 5-V input are shown in Fig. 12(a), (b), and (c), respectively. As shown in Fig. 12, the new proposed mixed-voltage I/O buffer can be successfully operated in

such a 2.5/5-V mixed-voltage I/O environment. The maximum operation frequency of the proposed I/O buffer depends on the output load and the device size of output circuit. Typically, the proposed mixed-voltage I/O buffer in this work has been successfully verified in silicon that can be operated up to 200 MHz with 20-pF load.

B. New Mixed-Voltage I/O Buffer 2

The floating n-well of the proposed mixed-voltage I/O buffer 1 in Fig. 9 is biased at $\sim$2.5 V and $\sim$5 V through the parasitic pn-junction diode in the transmit mode with 0-V output signal and in the receive mode with 5-V input signal, respectively. Thus, the voltage level of the floating n-well may be coupled with transient noise when the operating frequency
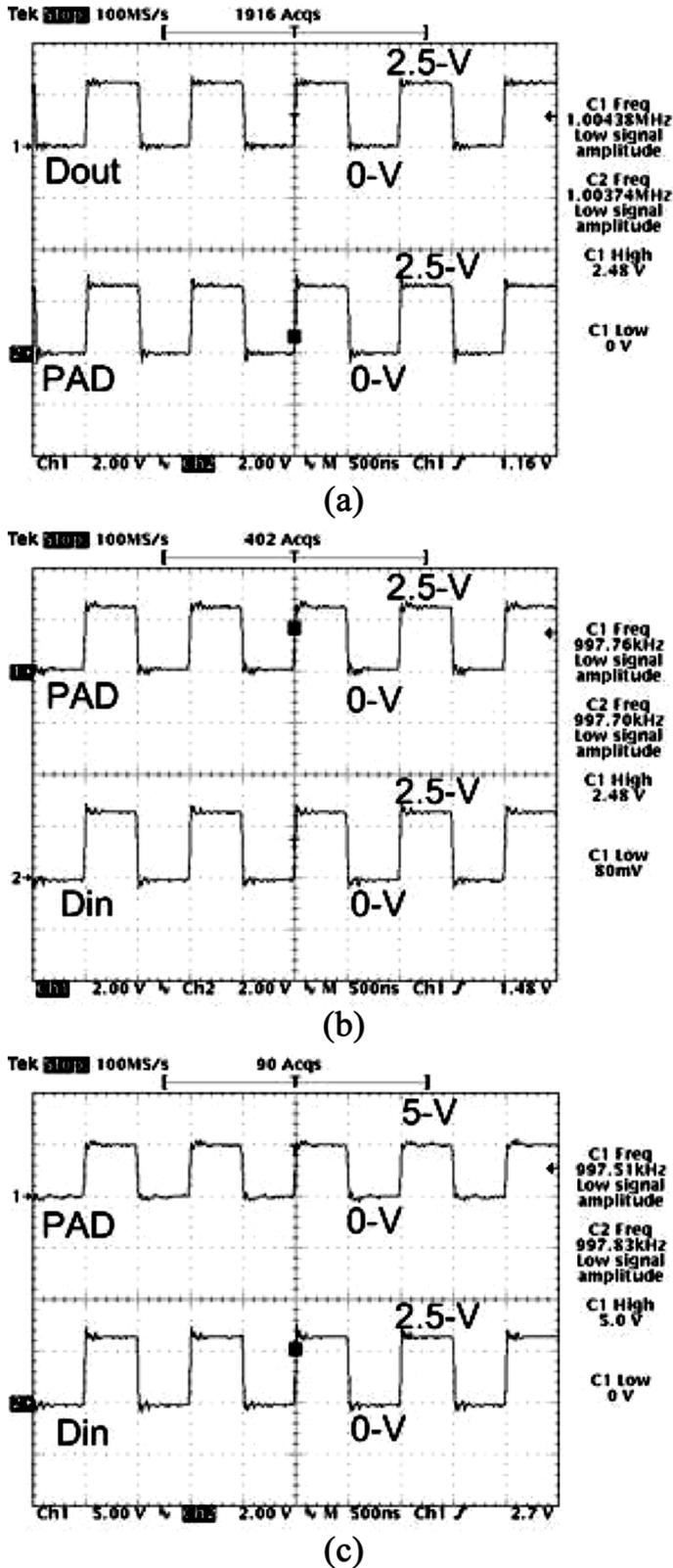
(a)

(b)

(c)

Fig. 12. Measured waveforms of the new proposed mixed-voltage I/O buffer 1 with 1-MHz I/O signal in (a) the transmit mode, (b) the tri-state input mode with 2.5-V input, and (c) the tri-state input mode with 5-V input.

of the mixed-voltage I/O buffer becomes higher. The lower floating n-well voltage results in the lower threshold voltage
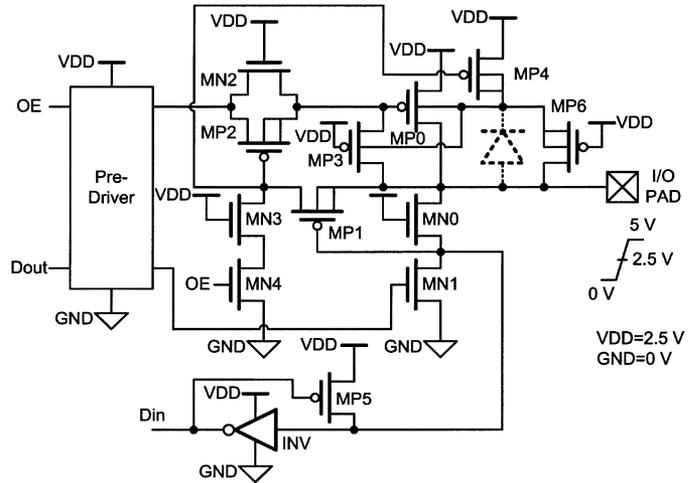

Fig. 13. New proposed mixed-voltage I/O buffer 2 with only thin-oxide devices.

(Vtp) of the pull-up PMOS, so that the subthreshold leakage current becomes large when the pull-up pMOS is in off state. Considering the coupled noise and the subthreshold leakage current issue due to the floating n-well, another new modified design of the proposed mixed-voltage I/O buffer without n-well floating is shown in Fig. 13. Comparing to the design in Fig. 9, the gate of transistor MP4 in Fig. 13 is connected to the gate of transistor MP2. Besides, two extra nMOS devices, MN3 and MN4, are added to pull the gate voltage of transistor MP4 to 0 V when the I/O buffer in Fig. 13 is operated in the transmit mode. In Fig. 13, transistor MN3 is used to protect transistor MN4 without the gate-oxide overstress, because the gate voltage of transistor MP4 may be as high as 5 V in the tri-state input mode. In the transmit mode, the gate voltage of transistor MP4 in Fig. 13 is pulled down to 0 V through transistors MN3 and MN4. Transistor MP4 is always turned on to bias the floating n-well at 2.5 V whenever the signal at I/O pad is 2.5 V or 0 V. In the receive mode with 5-V input signal, another pMOS device MP6 is turned on to bias the floating n-well at 5 V. Thus, whenever the proposed mixed-voltage I/O buffer 2 is in the transmit mode or the receive mode, the floating n-well is biased at 2.5 V or 5 V directly. The subthreshold leakage problem can be completely solved in the proposed mixed-voltage I//O buffer 2.

The proposed mixed-voltage I/O buffer 2 is simulated in a 0.25-μm 2.5-V CMOS process. Fig. 14(a) and (b) shows the simulated waveforms of the proposed mixed-voltage I/O buffer 2 operating in the transmit mode and the tri-state input mode, respectively. As shown in Fig. 14(a) and (b), the proposed mixed-voltage I/O buffer 2 can be operated correctly in the transmit mode and the tri-state input mode. Fig. 15 compares the simulated waveforms on the floating n-wells of the proposed mixed-voltage I/O buffer 1 (Fig. 9) and the proposed mixed-voltage I/O buffer 2 (Fig. 13) in the transmit mode. As shown in Fig. 15, the floating n-well of the proposed I/O buffer 2 is always kept at 2.5 V in the transmit mode. Thus, the proposed mixed-voltage I/O buffer 2 is recommended for high-speed and low-power applications.
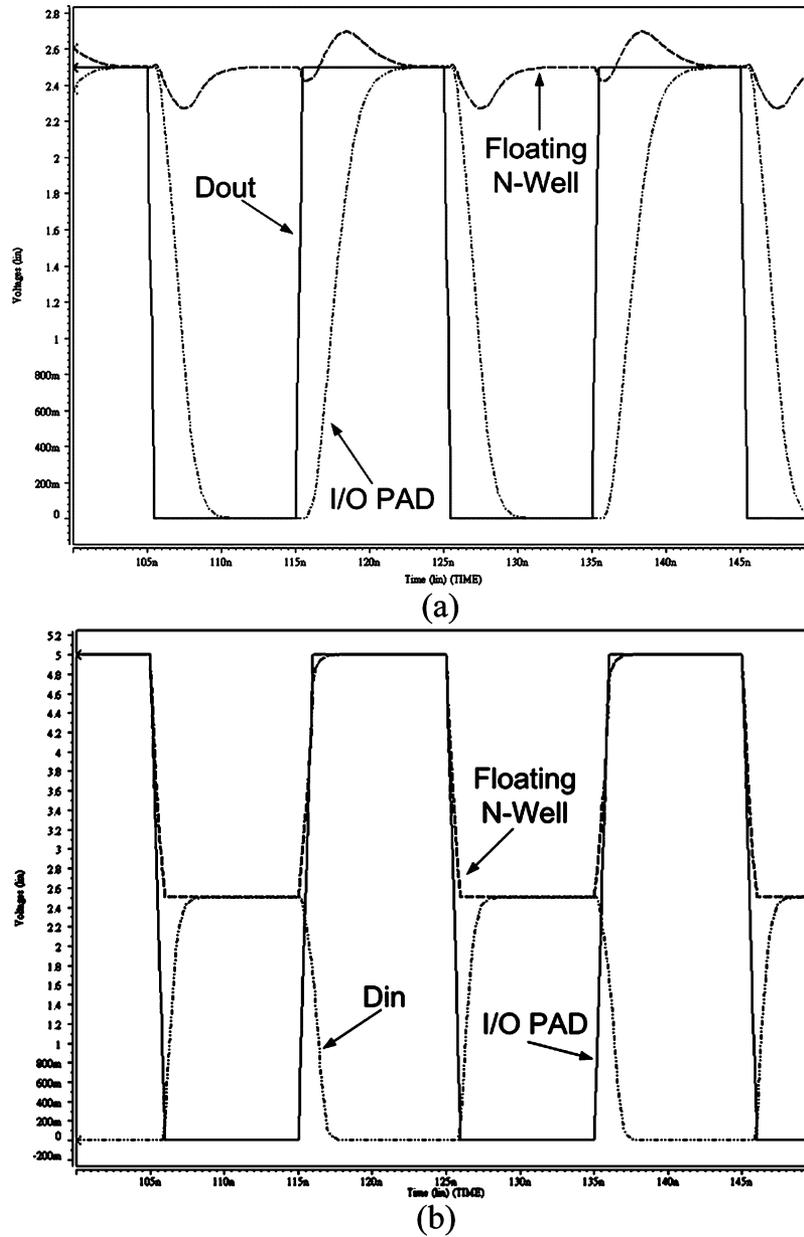
Fig. 14. Simulated waveforms of the new proposed mixed-voltage I/O buffer 2 with a 20-pF load and 50-MHz I/O signal in (a) the transmit mode, and (b) the tri-state input (receive) mode.

IV. DISCUSSION AND COMPARISON

A. Speed

The output loadings of these mixed-voltage I/O buffers include the I/O pad, the bonding wire, the package pin, the PCB trace, and so on. Therefore, the output loadings of these I/O buffers are usually very large. These mixed-voltage I/O buffers are simulated in a 0.25-μm 2.5-V CMOS process to compare their speed performances under the condition of the same output loading. Table I shows the simulated delay times from the node Dout to the I/O pad when these I/O buffers are in the transmit mode to drive a 20-pF output loading. As shown in Table I, the delay times of these I/O buffers in Figs. 6, 7, 8, 9, and 13 are almost the same, expect those of the

I/O buffers in Figs. 4 and 5. Although the driving capacities (by adjusting the device dimensions of output transistors) and the output capacitances of these I/O buffers are kept the same, the parasitic capacitances of the stacked pMOS devices in the output stage of the mixed-voltage I/O buffers in Figs. 4 and 5 are large. Besides, the larger threshold voltage of transistor MP0 in Fig. 4 (Fig. 5) owing to the body effect results in the lower driving capacity. Thus, these two I/O buffers in Figs. 4 and 5 have a little longer delay times than the other mixed-voltage I/O buffers.

B. Power Consumption

The power consumption of CMOS digital circuit includes three parts: the dynamic power consumption due to charging
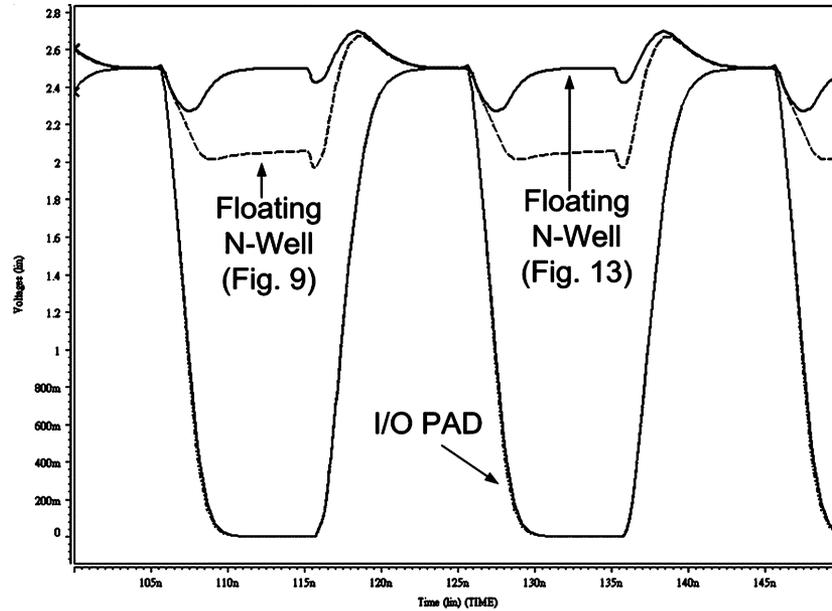
Fig. 15. Simulated waveforms to compare the voltage levels of the floating n-well in the mixed-voltage I/O buffers of Figs. 9 and 13, during the signal transition on the I/O pad.

TABLE I
COMPARISON ON DELAY AMONG THE MIXED-VOLTAGE I/O BUFFERS

Mixed-voltage I/O designs	Delay time (Dout to I/O pad)
Fig. 4 [14]	2.26 ns
Fig. 5 [15]	2.13 ns
Fig. 6 [16]	1.88 ns
Fig. 7 [17]	1.89 ns
Fig. 8 [18]	1.90 ns
Fig. 9 This work 1	1.81 ns
Fig. 13 This work 2	1.81 ns

TABLE II
COMPARISON ON POWER CONSUMPTION AMONG THE MIXED-VOLTAGE I/O BUFFERS IN THE TRANSMIT MODE

Mixed-voltage I/O designs	Average power consumption (Output load =20 pF, frequency=50 MHz)
Fig. 4 [14]	11.1 µW
Fig. 5 [15]	11.6 µW
Fig. 6 [16]	8.4 µW
Fig. 7 [17]	8.7 µW
Fig. 8 [18]	8.8 µW
Fig. 9 This work 1	9 µW
Fig. 13 This work 2	8.6 µW

and discharging the capacitance, the short-circuit power consumption, and the power consumption due to the dc leakage current. Because there should be no dc leakage current in the design of these mixed-voltage I/O buffers whenever they operate in the receive mode or transmit mode, the power consuming on the output loading dominates the total power consumption in these I/O buffers. Hence, the power consumptions of these mixed-voltage I/O buffers are almost the same if the output loadings are kept the same and the operating frequency is fixed. These mixed-voltage I/O buffers are simulated in a 0.25-μm 2.5-V CMOS process. The simulated power consumptions of these mixed-voltage I/O buffers in the transmit mode to drive the 20-pF output loading at the frequency of 50 MHz are compared in Table II. Although the output loadings of these mixed-voltage I/O buffers are all the same of 20 pF, the power consumptions of the I/O buffers in Figs. 4 and 5 are somewhat larger than those of the other I/O buffers. The reason is that the parasitic self output capacitances of the mixed-voltage I/O buffers in Figs. 4 and 5 are larger than those of the other I/O buffers.

C. Area

The total area of these mixed-voltage I/O buffers can be evaluated by calculating the total channel widths of transistors in these I/O buffers if the channel lengths of all devices in these I/O buffers are kept the same. Table III shows the calculated total widths of these mixed-voltage I/O buffers, where Wp and Wn are the unit width of the pMOS and nMOS devices, respectively. The total width is calculated including the widths of the devices in the pull-up and pull-down paths, the dynamic n-well bias circuit, the gate-tracking circuit, and the protecting devices of input buffer. Expect the devices in the pull-up and pull-down paths, the widths of the pMOS and nMOS devices in these I/O buffers are kept as Wp and Wn, respectively. For fair comparison, the driving capacities of the output stages in these mixed-voltage I/O buffers must be kept the same. Therefore, the widths of the pMOS and nMOS devices in the output stage

TABLE III
COMPARISON IN AREA (DEVICE SIZES) AMONG THE MIXED-VOLTAGE I/O BUFFERS

Mixed-voltage I/O designs	PMOSs in pull-up path	NMOSs in pull-down path	Other PMOSs	Other NMOSs	Total width of PMOSs in pull-up path	Total width of NMOSs in pull-down path	Total width of other PMOSs	Total width of other NMOSs	Total width of I/O buffer	Total width of I/O buffer in terms of Wn*
Fig. 4 [14]	MP0, MP1	MN0	MP2, MP3	MN1, MN2	12Wp	3Wn	2Wp	2Wn	14Wp+ 5Wn	47Wn
Fig. 5 [15]	MP0, MP1	MN0, MN1	MP2~4	MN2~4	12Wp	12Wn	3Wp	3Wn	15Wp+ 15Wn	60Wn
Fig. 6 [16]	MP0	MN0, MN1	MP1, MP2	MN2, MN3	3Wp	12Wn	2Wp	2Wn	5Wp+ 14Wn	29Wn
Fig. 7 [17]	MP0	MN0, MN1	MP1~5	MN2~6	3Wp	12Wn	5Wp	5Wn	8Wp+ 17Wn	41Wn
Fig. 8 [18]	MP0	MN0, MN1	MP1~8	MN2~5	3Wp	12Wn	8Wp	4Wn	11Wp+ 16Wn	49Wn
Fig. 9 This work 1	MP0	MN0, MN1	MP1~5	MN2	3Wp	12Wn	5Wp	1Wn	8Wp+ 13Wn	37Wn
Fig. 13 This work 2	MP0	MN0, MN1	MP1~6	MN2~4	3Wp	12Wn	6Wp	3Wn	9Wp+ 15Wn	42Wn

*Wp=3Wn

of stacked configuration are twice as those in the output stage of single device. In this calculation, the widths of the pMOS and nMOS devices in the output stage of single device are 3 Wp and 3 Wn, respectively. The widths of the pMOS and nMOS devices in the output stage of stacked configuration are 6 Wp and 6 Wn, respectively. Generally, Wp is triple as large as Wn in CMOS digital circuits [20]. Hence, the total widths of these mixed-voltage I/O buffers can be shown in terms of Wn for comparison. As shown in Table III, the total widths of the proposed mixed-voltage I/O buffers 1 and 2 are 37 Wn and 42 Wn, respectively. Although the total width of the I/O buffer in Fig. 6 is 19 Wn, this I/O buffer needs an extra pad to provide the external voltage to bias the n-well of the pull-up pMOS device. The area of this I/O buffer in Fig. 6, when it includes the extra pad into the chip, will become larger than that of the proposed I/O buffers.

D. Noise, Latch-Up and Subthreshold Leakage Issues

The n-wells of the pull-up pMOS devices in some mixed-voltage I/O buffers will be floated in some operation conditions. The I/O coupling noise into the floating n-wells of the pull-up pMOS devices could induce the latch-up issue. Therefore, the pull-up pMOS devices in these mixed-voltage I/O buffers must be carefully drawn in the layout. The guard rings must be used to surround the pull-up pMOS devices to isolate the I/O noise against the latch-up problem [21]. In addition, the lower threshold voltage of the pull-up pMOS device due to the lower floating n-well voltage results in the subthreshold leakage current. The proposed mixed-voltage I/O buffer 2 and the prior design [18] don't have the floating n-well issue. Thus, these two mixed-voltage I/O buffers are suitable for low-power applications.

E. Transient Stress

The stacked nMOS technique is used to avoid the gate-oxide overstress in the mixed-voltage I/O interface, as shown in Fig. 3. However, in some specified operation state, the upper transistor (MN0) may still suffer the hot-carrier issue. When the voltage on the I/O pad is initially kept at 5 V and then the transistor MN1 in Fig. 3 is turned on by its pre-driver circuit to pull down the pad voltage to 0 V, the drain–source voltage of transistor MN0 may exceed 2.5 V during this transient condition to suffer the hot-carrier degradation. Nevertheless, this transient-stress problem can be further solved by using three stacked devices and dynamically controlling the gate voltage of the top device [3].

Table IV lists the features among these mixed-voltage I/O buffers. Since the new proposed mixed-voltage I/O buffers and the prior I/O buffers reported in [14], [15], [17], and [18] use the dynamic n-well biased technique, no extra pad and power supply is required. The new proposed mixed-voltage I/O buffers in this work occupy smaller silicon area than the I/O buffers reported in [14]–[18]. Although the circuit structures of the mixed-voltage I/O buffers reported in [14], [15] are simpler, these two I/O buffers have the gate-oxide reliability problem. In Fig. 4, transistors MN0, MN1, and MP2 have the gate-oxide reliability problem in the tri-state input mode when the input signal has a 5-V voltage level. In Fig. 5, transistor MP2 has the gate-oxide reliability problem when the input signal at the I/O pad is 5 V in the tri-state mode. Besides, since the depletion pMOS is used to improve the gate-tracking circuit of the mixed-voltage I/O buffer reported in [16], extra mask and process modification are required to realize the depletion device. The prior mixed-voltage I/O buffers reported in [14], [15], [17] and the proposed mixed-voltage I/O buffer 1 may have the subthreshold leakage problem, but the prior mixed-voltage I/O buffer reported in [18] and the proposed mixed-voltage

TABLE IV
COMPARISON ON THE FEATURES AMONG THE MIXED-VOLTAGE I/O BUFFERS

Mixed-voltage I/O designs	N-well bias	Extra pad for n-well bias	Gate-oxide reliability issue	With special device	Subthreshold leakage issue	Area
Fig. 4 [14]	Dynamic bias	No	Yes	No	Yes	47Wn
Fig. 5 [15]	Dynamic bias	No	Yes	No	Yes	60Wn
Fig. 6 [16]	Fixed bias	Yes	No	Yes, Depletion PMOS	No	29Wn
Fig. 7 [17]	Dynamic bias	No	No	No	Yes	41Wn
Fig. 8 [18]	Dynamic bias	No	No	No	No	49Wn
Fig. 9 This work 1	Dynamic bias	No	No	No	Yes	37Wn
Fig. 13 This work 2	Dynamic bias	No	No	No	No	42Wn

I/O buffer 2 don't have. However, the proposed mixed-voltage I/O buffers occupy smaller silicon area than the prior I/O buffers [14], [15], [17], [18]. Thus, if the subthreshold leakage issue in the given CMOS process is not serious, the proposed mixed-voltage I/O buffer 1 is more recommended than the prior designs reported in [14], [15], [17]. If the subthreshold leakage problem in the given CMOS problem is serious, such as the 0.13- μm, 90-nm or below CMOS process, the proposed mixed-voltage I/O buffer 2 is recommended.

V. CONCLUSION

The prior designs of the mixed-voltage I/O buffers have been overviewed in this work. In addition, two new mixed-voltage I/O buffers with the stacked nMOS technique, dynamic n-well technique, and gate-tracking circuit are presented in this paper. The proposed mixed-voltage I/O buffer 1 has been implemented in a 0.25- μm 2.5-V CMOS process, which can be operated in the 2.5/5-V signal environment without the gate-oxide reliability problem. The proposed mixed-voltage I/O buffer 2 can be applied for high-speed applications without the gate-oxide reliability problem and the circuit leakage issue. The proposed mixed-voltage I/O buffers can be easily scaled toward 0.18- μm (or below) CMOS processes to serve other mixed-voltage I/O interfaces, such as 1.8/3.3-V or 1.2/2.5-V interfaces in 0.18- μm or 0.13- μm CMOS processes.

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