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Journal of Magnetism and Magnetic Materials 304 (2006) e297–e299
Journal of magnetism and magnetic materials
www.elsevier.com/locate/jmmm

High-temperature magnetoresistance study of a magnetic tunnel junction

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Abstract

The thermal stability and the spin transportation phenomenon at room temperature and 140 °C of a series of magnetic tunneling junctions with the structure of bottom electrode/PtMn/Pinned layer/ AlO_x/CoFe/NiFe/top electrode have been investigated. The MR ratio decreases from 33.5% at room temperature to 29% at 140 °C. The MR ratio at room temperature increases roughly 0.8% after thermal treatment at temperatures above 60 °C. This is related to the thermal relaxation of the strains existing in the samples.

Keywords: Magnetic tunnel junction; Tunneling magnetoresistance; Temperature dependence; Thermal annealing

1. Introduction

Tunneling magnetoresistance (TMR) studies, both in theory and experiment, are currently the subject of much research [1–4]. The tunneling magnetoresistance behaviors are the resistances for parallel and antiparallel spin alignment states of two ferromagnetic layers in a tunneling junction, respectively, and are fundamentally important in understanding spin-polarized electron tunneling and applications in digital devices, such as sensors and magnetic random access memory (MRAM). The ratio of TMR can be generally understood by Julliere's model that polarization of magnetic layers plays a dominant role [5]. However, many essential factors, such as the interfacial effect, impurities, structures of the layers, and temperature, etc., change the properties of a TMR system [6]. Since the relatively high temperature due to post manufacturing processes after MTJ structure could cause considerable damage on the Magnetic tunneling junction (MTJ) structure and decrease the function of MRAM devices, the temperature dependence of TMR ratio is desired for practical application purpose [7–9].

In this study, we report an investigation of the temperature dependence between room temperature and 140 °C as well as the thermal annealing effect for the MTJ structure involved in MRAM devices which were made by commercial manufacturing process.

2. Experiments

The main shape of the MTJ pattern is an ellipse with 0.72 μm and 0.36 μm in the long axis and short axis, respectively. A series of standard manufacturing processes of photolithography, oxidization, etching, and metallization were used to construct the structure, SiO_2/Ta(20 nm)/PtMn(15 nm)/CoFe(2 nm)/Ru(0.8 nm)/CoFe(3 nm)/Al–O_x (1.2 nm)/CoFe(1 nm)/NiFe(3 nm)/Ta(60 nm). SiO_2 was chosen as a substrate, and the following metal layers were deposited on substrates by sputtering. The first layer is Ta(20 nm), used as a bottom electrode. PtMn(15 nm) serves as an antiferromagnetic layer which pins the following tri-layered SAF (synthetic antiferromagnet) structure, CoFe(2 nm)/Ru(0.8 nm)/CoFe(3 nm). During the depositing of the PtMn layer, an external magnetic

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doi:10.1016/j.jmmm.2006.02.062

field was also applied to define the direction of magnetization of the antiferromagnetic layer. Due to the exchange coupling effect, the two CoFe layers in the tri-layered SAF structure can form an antiparallel configuration of magnetization, so the tri-layered SAF structure can be used as a pinned layer. The insulator layer was made of Al–O$_x$ (~1.2 nm), which was manufactured by pre-depositing an Al thin layer(~9 Å) followed by a process of introducing O$_2$ for 25–30 s to cause oxidization. Then the CoFe(1 nm)/NiFe(3 nm) bilayer was used as a free layer. Finally, we deposited Ta(60 nm) as the top electrode layer. In order to ensure the function of the PtMn layer, a process of magnetic annealing is applied to the wafer. The conditions of magnetic annealing were at 275 °C and 8000 Oe for 5 h. After thin film depositing, the processes of photolithography and dry etching were used to pattern the MTJ figures and testing circuits.

The electrical properties of the TMR were measured by using a DC source with varying temperature from 25 through 140 °C.

3. Results and discussion

The temperature dependences of the resistance in both parallel and antiparallel states are plotted in Fig. 1. The crystallization of the PtMn layer was studied below 400 °C, and the MR ratio and exchange field were found to be closely related to the phase change of the structure of PtMn [10]. The samples were measured at a constant bias of 50mV with varying temperatures between 25 and 140 °C. The high resistance states (from roughly 28.5 kΩ down to 26 kΩ) are related to the antiparallel state in the two magnetic layers at both sides of the Al–O$_x$ layer, and the lower resistance states (from roughly 21.5 kΩ down to 20 kΩ) are related to the parallel state in the two magnetic layers.

Both curves show a negative temperature coefficient; i.e. the slope of the curves is −21.9 Ω/°C (−220.8 Ω/°C) for the high (low) resistance state. The decrease of resistance with increasing temperature can be easily explained by Fermi–Dirac distribution which gives us the probability that a state with specific energy is occupied at a specific temperature. Therefore, the higher the temperature the system is at, the more free electrons can be transported in the tunneling system.

Fig. 2 plots both the MR ratio and the difference of the resistance between the two magnetic configurations of the two magnetic layers as a function of temperature between room temperature and 140 °C. It is roughly linearly decreasing with increasing temperature. The decreasing of the MR ratio from 33.5% at room temperature down to 29% at 140 °C could be mainly due to the flipping of the conducting spin during tunneling through the barrier, and the higher temperature may provide more energy for the electron spin to flip. Another possible reason could be that the increasing temperature lowers the spin polarization rate of the magnetic electrode injecting spin polarized current into the tunnel junction.

In order to ensure that the MTJ structure will still be able to serve in MRAM devices after the post manufacturing process, the thermal annealing effect was studied. In Fig. 3, the values of MR ratio at room temperature after heat annealing are plotted as a function of the annealing temperature through 140 °C. It is clear that the MR ratio measured at room temperature increases roughly 0.8% after thermal treatment at temperatures above 60 °C. A possible explanation is that the thermal effect relaxed the strains existing in the layers of the sample after thermal annealing, so the polarization of the free layer could slightly increase.

In conclusion, from Figs. 2 and 3, we have experimentally shown that this series of MTJ structures can still normally perform the TMR function at higher tempera-

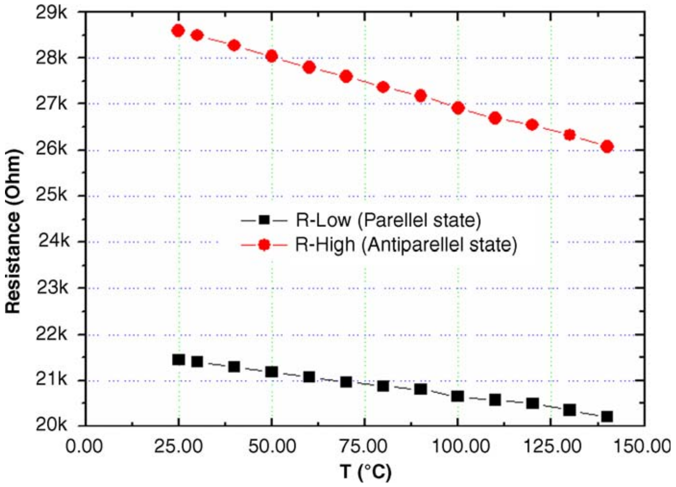

Fig. 1. Temperature dependent resistance in both parallel and antiparallel states.

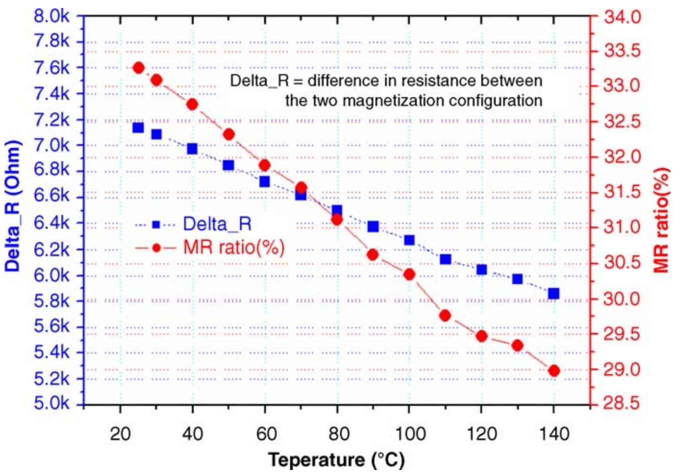

Fig. 2. The MR ratio (%) and the difference between the two configurations of magnetic states varying with temperature.

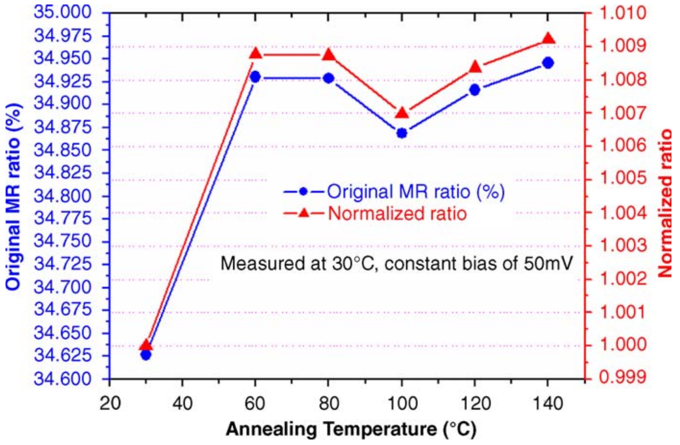

Fig. 3. The thermal annealing effect in MR ratio: each point of data was first heated to higher temperature then cooled down to 30 °C to measure its electrical resistance with an applied bias of 50 mV. The scale bar on the right indicates the normalized values of MR % in which the value without annealing equals 1.

tures (~140 °C). The MR ratio at 140 °C can still remain roughly 87% of that at room temperature. Generally speaking, in application, the local higher temperature which an electronic equipment can achieve is around 60–80 °C while operating, so the MR ratio of the MTJs at the operating situation can still remain a considerable portion (90–95%) of that at room temperature. However, a more important investigation is to perform time stress tests, that is, to apply a higher voltage across MTJs for a considerably long time. This test could provide more reliable information on the features of the MTJs.

Acknowledgment

The financial support from the NSC (National Science Council, Taiwan) and MTJ manufacturing support from both TSMC (Taiwan Semiconductor Manufacturing Company) and ERSO, ITRI (Electronics Research & Service Organization, Industrial Technology Research Institude, Hsinchu, Taiwan) are greatly appreciated.

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