

Enhancement of Brightness Uniformity by a New Voltage-Modulated Pixel Design for AMOLED Displays

Hau-Yan Lu, Po-Tsun Liu, *Member, IEEE*, Ting-Chang Chang, and Sien Chi

Abstract—This letter presents a new pixel design and driving method for active-matrix organic light-emitting diode (AMOLED) displays using low-temperature polycrystalline silicon thin-film transistors (TFTs). The proposed pixel circuit consists of five TFTs and one capacitor to eliminate the variation in the threshold voltage of the TFTs, and the drop in the supply voltage in a single frame operation by the source-follower-type connection and the bootstrap. The proposed pixel circuit has been verified to realize uniform output current by the simulation work using the HSPICE software. The novel pixel design has great potential for use in large-size and high-resolution AMOLED displays.

Index Terms—Active-matrix organic light-emitting diode (AMOLED), current-resistance (IR) drop, pixel design, polycrystalline silicon thin-film transistors (poly-Si TFTs), uniformity.

I. INTRODUCTION

ACTIVE-MATRIX organic light-emitting diode (AMOLED) displays based on polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have attracted much attention because of its superior characteristics in flat displays. These advantages include high brightness, wide viewing angle, and fast response time. The lifetime of organic light-emitting diode (OLED), however, needs to be improved. Furthermore, it is difficult to implement an AMOLED panel with good image quality because of variations in the threshold voltage and in the mobility of poly-Si TFTs among pixels [1]. Several voltage modulation and current programming schemes have been devised to solve the nonuniformity problem [2]–[5]. The voltage driving method formulated by Dawson *et al.* may effectively compensate for threshold voltage variations. The driving current in AMOLED panels and the number of scan lines should be increased with the panel size and brightness.

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H.-Y. Lu and S. Chi are with the Department of Photonics and the Institute of Electro-Optical Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C.

P.-T. Liu is with the Department of Photonics and the Display Institute, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: ptliu@mail.nctu.edu.tw).

T.-C. Chang is with the Department of Physics and the Institute of Electro-Optical Engineering, National Sun Yat-Sen University, Kaohsiung 804, Taiwan, R.O.C.

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The intrinsic display loading effects of a voltage drop across the parasitic resistance of the supply power line also causes nonuniformity of brightness in voltage-driven AMOLED panels. The drop in the supply voltage on the panel [V_{dd} current-resistance (IR) drop] is a critical issue leading to image degradation and crosstalk [6]. The use of AMOLED displays for large-size applications is expected to have many advantages, so the driving method and pixel structure should be applicable to large-size panels. However, most compensating pixel circuits with simple structures only solve one of the aforementioned problems [7], [8]. Some complicated designs have very uniform output current among pixels, but these may reduce the aperture ratio or require additional peripheral driving circuits [9], [10].

This letter presents a new driving scheme with the source-follower-type connection and the bootstrap to simultaneously eliminate the effect of threshold voltage variations in the driving TFT (DTFT) and the drop in the supply voltage. The simulation results demonstrate that the variation in the current driving OLED among pixels can be significantly reduced.

II. PROPOSED PIXEL STRUCTURE AND DRIVING METHOD

In the conventional architecture, the OLED is driven by the current generated by the potential difference between the gate and the source (V_{gs}) of the DTFT, which is given by $|V_{data} - V_{dd}|$. However, the driving current that passes through the supply power electrode causes a voltage drop due to the parasitic resistance of the power line, as shown in Fig. 1. Even if the pixel circuit can compensate for the variation of the threshold voltage in the DTFT, the V_{gs} in each DTFT still varies from pixel to pixel along the electrode, generating various driving currents. This phenomenon causes the brightness to be nonuniform from the top to the bottom of the panel.

Fig. 2(a) presents the proposed circuit and its driving scheme. The design includes one DTFT, four switching TFT (T1, T2, T3, and T4), and one capacitor (Cst). V_{data} represents a voltage data signal line, and V_{dd} refers to a constant voltage source line. The operation of the proposed circuit is divided into three stages shown in Fig. 2(b). During stage (1), [n]Scan and [n]EM are set at the high level to turn on T1, T2, and T3, so that the node voltage of DTFT connected to the right side of Cst is increased to V_{dd} , and this node becomes the source of DTFT. Therefore, the pixel circuit is a p-type source follower. The next stage is the V_{th} detecting period. Only [n]EM is set

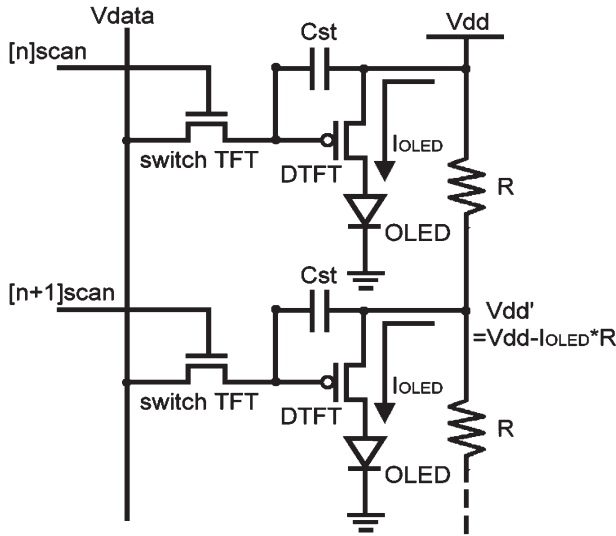


Fig. 1. Circuit scheme of the conventional pixel circuit (2T1C) and the voltage drop caused by the intrinsic parasitic resistance (R) at the V_{dd} supply power line.

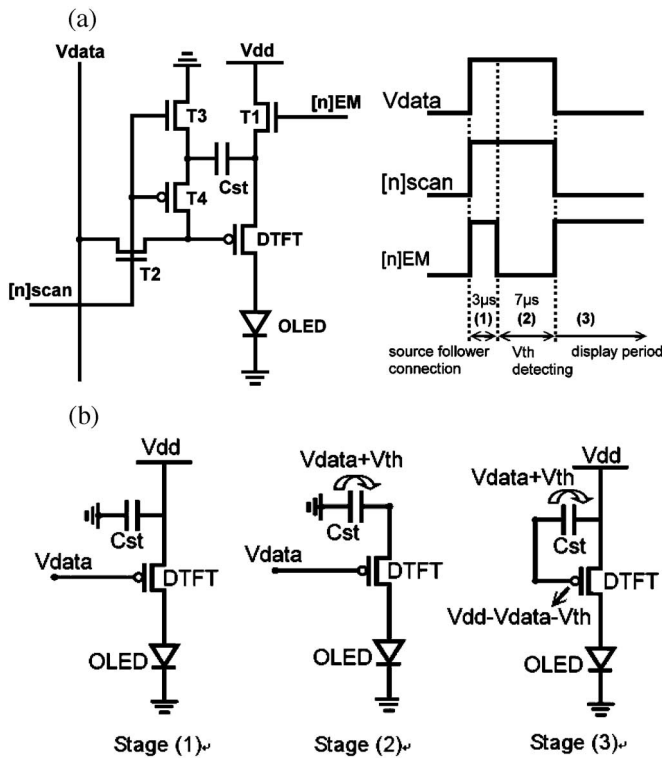


Fig. 2. (a) Proposed pixel design and timing scheme of the signal line. (b) Equivalent circuit at each stage in operation.

low to turn off T1, whereas scan[n] remains high. The source voltage of DTFT is discharged until it is turned off. This node voltage settles from V_{dd} to $V_{data} + V_{th}$, where V_{th} is the threshold voltage of DTFT. Accordingly, the threshold voltage of DTFT and the data signal are stored in the right side of Cst. The left side of Cst is set to ground during stages (1) and (2). After the pixel scanning period, the third stage, which is the display period, is implemented. During stage (3), [n]scan is set to low to turn off T2 and T3 but turn on T4, and [n]EM is

set to high again so that the gate of DTFT can be connected to the left side of Cst; the source voltage of DTFT is charged up to V_{dd} from $V_{data} + V_{th}$. Immediately, the gate voltage of DTFT should be boosted to $V_{dd} - V_{data} - V_{th}$ by the conservation of charge in the capacitor as bootstrap is performed. Accordingly, DTFT starts to generate current (I_{OLED}), which drives the OLED. Cst sustains the gate voltage of DTFT $V_{dd} - V_{data} - V_{th}$ for the period of a frame. I_{OLED} is also the saturation current of DTFT. In this letter, the minimum design rule for the channel length of TFT devices is $5 \mu\text{m}$, so that the second-order effect is not thereby considered in the proposed analysis. Thus,

$$\begin{aligned} I_{OLED} &= K[V_{gs} - V_{th}]^2 \\ &= K[(V_{dd} - V_{data} - V_{th}) - (V_{dd}) - (-V_{th})]^2 \\ &= K[V_{data}]^2. \end{aligned}$$

Therefore, I_{OLED} is independent of the threshold voltage of DTFT and the supply voltage and is affected only by data voltage.

III. SIMULATION RESULTS

The HSPICE software with the Rensselaer Polytechnic Institute (RPI) poly-Si TFT model (Level = 62) was used to verify the proposed circuit. The aspect ratio, mobility, and threshold voltage of DTFT were 3.3/5, $80 \text{ cm}^2/\text{V} \cdot \text{s}$, and -2 V . Cst was set to 0.5 pF , V_{dd} and the high level of the signals ([n]Scan and [n]EM) were set to 5 and 9 V, respectively. The initial supply voltage was modulated such that the I_{OLED} in the following cases was approximately $1 \mu\text{A}$ as luminance and resolution were designed to be 300 cd/m^2 and 133 ppi. From the 600 TFTs tested, the maximum shift of the threshold voltage is about 0.2 V at a mean threshold voltage of -2.41 V . In this letter, the variation of the threshold voltage of DTFT is set at 0.3 V to validate the worst case design.

Fig. 3(a) plots the simulation result of the proposed pixel structure when the threshold of the DTFT was set to -1.7 , -2 , and -2.3 V . The simulation results indicate that the variation of I_{OLED} in the proposed pixel is clearly reduced using the adoption of the new threshold voltage compensation method. In a display period, the variation of I_{OLED} in the proposed design is very small, which is between around 1.01 and $0.99 \mu\text{A}$. Therefore, the strong immunity to the variation of the threshold voltage in the DTFT in the proposed pixel structure is verified. Fig. 3(b) shows that simulated degradation of the supply voltage on the panel is 0.5 V . According to Fig. 3(b), the deviation of I_{OLED} in the presented pixel structure is less than 2.5% , confirming the effectiveness of the prevention against the degradation of the supply voltage.

Fig. 4 shows the comparison of the I_{OLED} degradation in the conventional pixel structure (2T1C) with that in the proposed structure (5T1C), which is caused by the drop in the supply voltage as the number of scan lines increases (240, 480, 600, 768) [11]. The x -axis indicates the distance from the supply voltage point to each pixel by the number of scan lines. By

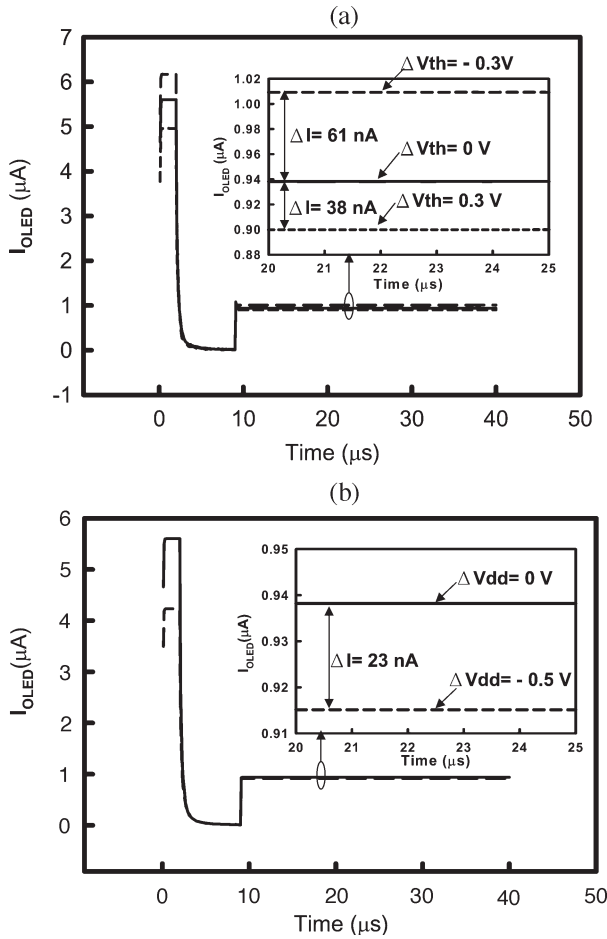


Fig. 3. (a) Transient simulation results for the proposed pixel structure. With the threshold voltage shift of DTFT set as $\pm 0.3V$, the variation of output current is about $1.01-0.99 \mu A$. (b) Transient simulation results for the proposed pixel structure. The deviation of I_{OLED} in the proposed pixel structure is less than 2.5%, and the degradation of the supply voltage on the panel is 0.5 V.

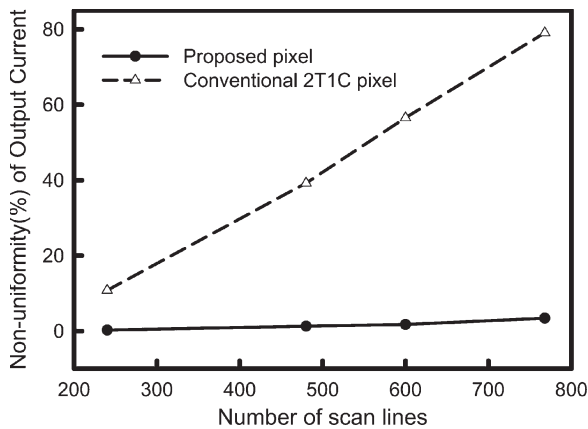


Fig. 4. Comparison of nonuniformity of output current between the conventional pixel structure (2T1C) and the proposed one (5T1C) caused by the drop in supply voltage with an increasing number of scan lines (240, 480, 600, 768).

increasing the number of scan lines for large-size or high-resolution AMOLED displays, the resistance of the power line leads to the larger supply voltage drop in the conventional 2T1C pixel design. In contrast, in the proposed 5T1C pixel design, the

nonuniformity of the output current remains almost constant while the number of scan lines increases, and the maximum degradation of I_{OLED} is just approximately 3.1%. Therefore, the proposed pixel structure is a promising candidate for use in large-size and high-resolution AMOLED displays.

IV. CONCLUSION

A new voltage modulation pixel circuit is developed for application to large-size and high-resolution AMOLED displays. The nonuniformity of the output current is improved substantially using the proposed compensation operation. The average deviation of the TFT driving current is about 50 nA as the threshold voltage is varied by 0.3 V, and the nonuniformity of the I_{OLED} with increasing number of scan lines in the proposed pixel structure is less than 3.1%. The simulation results successfully demonstrate that the proposed circuit has high immunity to both the voltage variation in poly-Si TFTs and the drop in the supply voltage.

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