HfSiON n-MOSFETs Using Low-Work Function $HfSi_x$ Gate

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***Abstract*—The authors have developed a novel high-temperature stable $HfSi_x$ gate for high-κ HfSiON gate dielectric. After a 1000 °C RTA, the $HfSi_x$/HfSiON devices showed an effective work function of 4.27 eV and a peak electron mobility of 216 $cm^2/V \cdot s$ at 1.6-nm equivalent oxide thickness, with additional merit of a process compatible with current very large scale integration fabrication lines.**

***Index Terms*—HfSi, HfSiON, n-MOSFETs.**

I. Introduction

TO CONTINUE the very large scale integration (VLSI) scaling trend, the using metal gate and high-κ gate dielectric are needed to reduce the dc power consumption and gate depletion [1]–[12]. However, one of the difficult challenges for metal-gate/high-κ MOSFET is the large threshold voltage (V_t) by Fermi-level pinning that is opposite to scaling trend. To overcome this problem, low- and high-work-function metal gates are required to reduce the pinning effect. Previously, we have reported the Ir_xSi gate on HfAlON has high effective work-function ($\phi_{m-\text{eff}}$) of 4.9 eV [12] and useful for p-MOS. For n-MOSFET, the novel TaC gate has shown low $\phi_{m-\text{eff}}$ [1], [2]. However, the full silicidation (FUSI) gate [3]–[5], [8]–[13] for n-MOS is still needed to develop, which is due to the inherent advantage of the process compatibility with current poly-Si gate CMOS technology. In this letter, we have used the similar method of previously reported Ir_xSi for p-MOS [12] to develop the low-work-function $HfSi_x$ gate for n-MOSFET. This is because the Hf has very low work function of 3.5 eV in the Periodic Table. The $HfSi_x$ gate on HfSiON, formed by Hf deposition on thin amorphous Si, gives a low $\phi_{m-\text{eff}}$ of 4.27 eV and a good electron mobility of 216 $cm^2/V \cdot s$. In addition, the $HfSi_x$/HfSiON can sustain a high rapid thermal annealing (RTA) temperature of 1000 °C that is compatible with current VLSI process line. Since both process and mechanism of $HfSi_x$ and Ir_xSi, with respective low and high $\phi_{m-\text{eff}}$, are the same, these results indicate the high possibility to realize dual work-function metal-gate/high-κ CMOS with large $\phi_{m-\text{eff}}$ difference.

II. Experimental Procedure

We have used the 12-in p-type Si wafers in this letter. After standard clean, the HfSiO was deposited by atomic-layer deposition (ALD) and the HfSiON was formed by applying direct nitrogen plasma to HfSiO surface. Then, amorphous Si with various thickness of 50 to 5 nm was deposited on HfSiON as a silicide layer and metal barrier for subsequently deposited 20-nm-thick Hf by physical vapor deposition (PVD). A Mo layer (30-nm thickness) was also deposited to cover the Hf to prevent oxidation. The MOS capacitor was formed by patterning and RTA at 1000 °C for 10 s. For n-MOSFET, additional 150-nm-thick amorphous Si was deposited on Hf/Si/HfSiON to prevent ion implantation penetration through gate, where the n^+ source–drain regions are formed by using a phosphorus ion implantation at 35 KeV. Then, the 1000 °C RTA was applied to activate the implanted dopant and the n-MOSFET was fabricated by this self-aligned gate first process. Since both the MOS capacitor and MOSFET follow the same high-temperature RTA, there should be no fundamental difference in gate stack even though they were covered by different Mo or poly-Si for device fabrication. Note that the FUSI $HfSi_x$ gate is formed at high-temperature RTA and similar to previous Ir_xSi gate [12], which are different from conventional low-temperature salicide process. At such high 1000 °C RTA temperature, the fast silicidation reaching to the Si/HfSiON interface may also reduce the reaction of thin amorphous Si (5 nm) with high-κ dielectric to cause Fermi-level pinning. For comparison, Al gated devices on HfSiON were also formed. The fabricated devices were characterized by capacitance–voltage (C–V) and current–voltage (I–V) measurements.

III. Results and Discussion

Fig. 1(a) and (b) shows the C–V and J–V characteristics for $HfSi_x$/HfSiON and control Al/HfSiON capacitors, where the $HfSi_x$ gate was formed at 1000 °C RTA. The Al-gated capacitor with work-function of 4.1 eV was used as a reference [13] since it is known to have little Fermi-level pinning of low-temperature deposited pure metal gate on high-κ dielectric [7]. For thicker amorphous Si of 50 and 10 nm on HfSiON, the capacitance density decreases with increasing the thickness of amorphous Si indicating in $HfSi_x$ gate on HfSiON not fully silicided.

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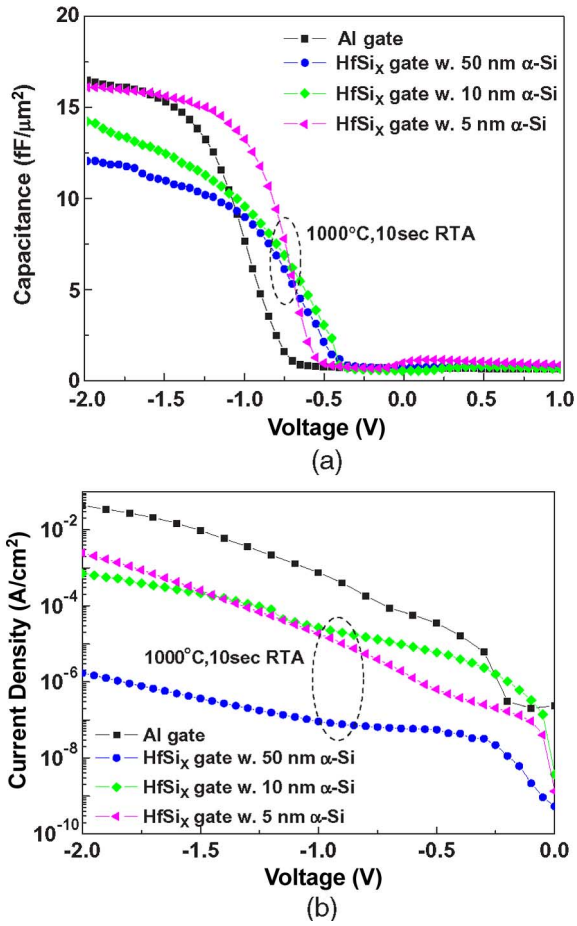

Fig. 1. (a) C–V and (b) J_g–V_g characteristics for high-temperature RTA formed $HfSi_x$/HfSiON and low-temperature Al/HfSiON capacitors. The device area was 100×100 μm. (Color version available online at http://ieeexplore.ieee.org.)

This in turn gives a higher flat-band voltage $(V_{\rm fb})$ due to the Fermi-level pinning on high-κ dielectric. This result is similar to the measured relative high $\phi_{m\text{-eff}}$ of 4.5 eV in HfSi/SiO_2 devices [14], where the silicidation was formed at 600 °C–750 °C low-temperature RTA. In contrast, the $HfSi_x$ formed by thin 5-nm amorphous Si shows the same capacitance density with control Al gate suggesting the successful FUSI gate formation. From the C–V shift referenced to the control Al gate, an extracted $\phi_{m\text{-eff}}$ of 4.27 eV is obtained for $HfSi_x$/HfSiON that is suitable for n-MOS application. The low $V_{\rm fb}$ and $\phi_{m-\rm eff}$ for $HfSi_x$ gate capacitors with 5-nm amorphous Si may be due to the Hf diffusion toward the HfSiON surface through thin amorphous Si that decreases the work function. This is the same mechanism for achieving high $\phi_{m-\rm eff}$ in high-work-function metal-rich Ir_xSi on high-κ HfAlON [12]. high In addition, low leakage current of 1.9×10^{-5} A/cm at -1 V is measured at an equivalent oxide thickness (EOT) of $\sim$ 1.6 nm, which suggests the good thermal stability of $HfSi_x$ gate on HfSiON dielectric even after 1000 °C RTA. Therefore, improved Fermi-level pinning, reasonable low $\phi_{m-\rm eff}$ of 4.27 eV and a low gate dielectric leakage current can be achieved in $HfSi_x$/HfSiON MOS capacitors at the same time.

Fig. 2 shows the transistor I_d–V_d characteristics as a function of V_g–V_t for the 1000 °C RTA-annealed $HfSi_x$/HfSiON

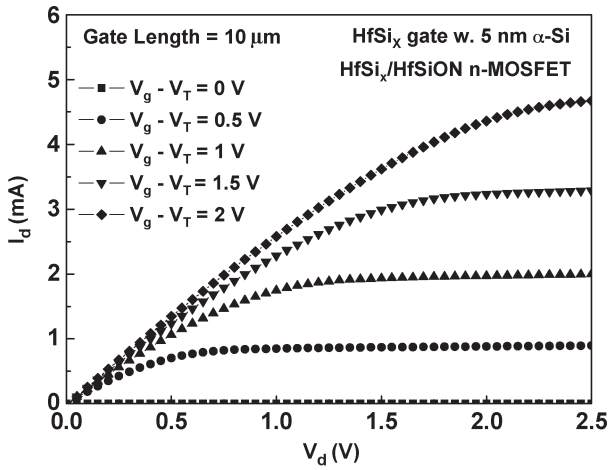

Fig. 2. I_d–V_d characteristics of an $HfSi_x$/HfSiON n-MOSFET. The amorphous Si on HfSiON was 5 nm and gate length was 10 μm.

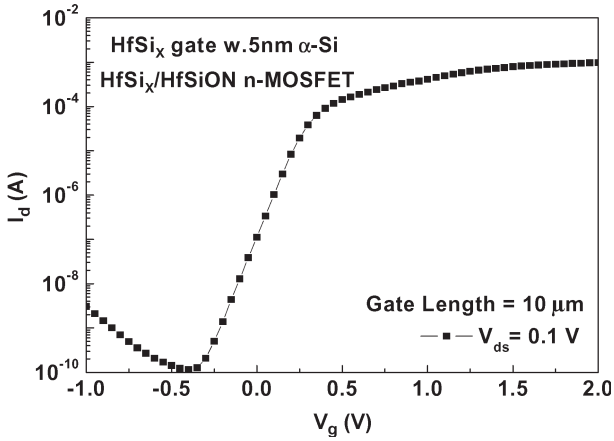

Fig. 3. I_d–V_g characteristics an $HfSi_x$/HfSiON n-MOSFET. The amorphous Si on HfSiON was 5 nm and gate length was 10 μm.

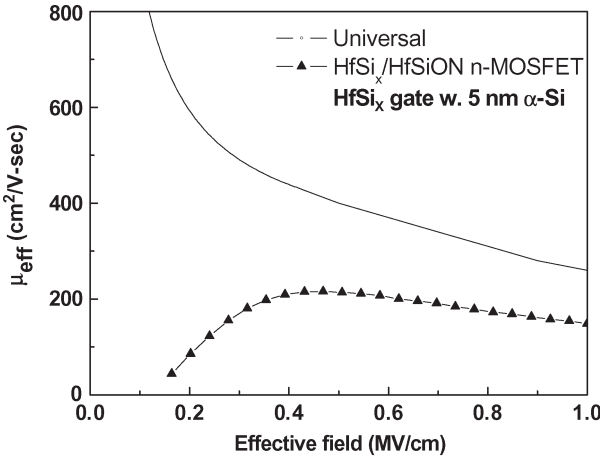

Fig. 4. Electron mobility of $HfSi_x$/HfSiON n-MOSFETs.

n-MOSFETs. The well-behaved I_d–V_d curves indicate the good device performance by using an $HfSi_x$ gate. Fig. 3 displays I_d–V_g characteristics of the $HfSi_x$/HfSiON n-MOSFETs. A low V_t of only 0.14 V was measured from the linear I_d–V_g plot, which is due to the low $\phi_{m-\rm eff}$ of 4.27 eV from the C–V measurements.

Fig. 4 shows the electron mobility extracted from the measured I_d–V_g curves of the n-MOSFETs. A peak electron mobility of 216 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ was obtained for the HfSi_x/HfSiON n-MOSFETs, which is close to published data in literature [15], [16].

IV. Conclusion

Using the novel HfSi_x gate formed by thin amorphous Si on HfSiON, good device performance has been obtained for n-MOSFETs with low $\phi_{m-\mathrm{eff}}$ and V_t values. This promising HfSi_x/HfSiON n-MOSFET has additional merit of full process compatibility with current VLSI lines.

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