RFIC TaN/$SrTiO_3$/TaN MIM Capacitors With 35 fF/μm^2 Capacitance Density

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***Abstract*—A very high density of 35 *fF*/μm^2 is measured in a radio frequency (RF) metal-insulator-metal (MIM) capacitor using high-κ (κ = *169*) *$SrTiO_3$* fabricated by very large scale integration (VLSI) back-end integration. A very small capacitance reduction of 4.1% from 100 kHz to 10 GHz, low leakage current of 1×*10^{-7} A/cm^2* at 1 V are simultaneously measured. The small voltage dependence of a capacitance $\Delta C/C$ of 637 ppm is also obtained at 2 GHz, which ensures this MIM capacitor useful for high precision circuits operated at a RF regime.**

***Index Terms*—Capacitor, International Technology Roadmap for Semiconductors (ITRS), metal-insulator-metal (MIM), radio frequency integrated circuit (RF IC), $SrTiO_3$.**

I. INTRODUCTION

CONTINUOUS down-scaling of component size is the technology trend for very large scale integration (VLSI), which is important to reduce the die size and chip cost. For radio frequency integrated circuits (RF ICs), the active MOSFETs scale down by 70% in length every two years and also give higher RF gain and lower noise. However, the passive RF metal-insulator-metal (MIM) capacitor scales down at a much slower rate and consumes a large portion of the whole die area. Therefore, it is necessary to increase the capacitance density ($\varepsilon_0\kappa/t_d$) for a smaller device area of RF capacitors that are widely used for impedance matching, dc blocking, and filtering in RF ICs. To achieve this goal, high dielectric constant (κ) material is required since the decreasing dielectric thickness (t_d) will exponentially increase the undesired leakage current. Therefore, high-κ dielectric has been continuously evolving from SiON (κ ~4–7) [1]–[3], Al_2O_3 (κ = 10) [4]–[6], and HfO_2 (κ ~ 20) [7] or Ta_2O_5 (κ ~ 24) [8], [9], according to International Technology Roadmap for Semiconductors (ITRS). For κ value larger than 25, ternary dielectric is needed and we have previously shown good RF characteristics of MIM capacitors using TaTiO (κ ~ 45) [10], [11]. In this study, we have further developed high performance RF MIM capacitors with the very high-κ Strontium Titanate oxide ($SrTiO_3$). The $SrTiO_3$ (STO) is also listed in the future DRAM manufacturing roadmap due to its high κ value of ~300 and paraelectricity (no fatigue or aging problem) [14]. We report the very high density of 35 fF/μm^2, small capacitance reduction of 4% from 100 KHz to 10 GHz, and small leakage current of 1×10^{-7} A/cm^2 for TaN/STO/TaN MIM capacitors. Such excellent results are due to the very high κ value of 169 [1]–[11]. Such large capacitance density can drastically reduce the area of current foundry-provided RF capacitor by ~35 times with additional advantages of full process compatibility to the current VLSI line and capable to integrate with DRAM for multifunctional system-on-chip (SoC).

II. EXPERIMENTAL PROCEDURE

After depositing thick isolation SiO_2 on standard Si wafers using VLSI back-end process, the TaN/Ta bi-layer was deposited on SiO_2/Si-substrate by sputtering and patterned to form the bottom capacitor electrode. Such bi-layer structure with thick Ta is needed to reduce the RF ohmic loss. To further improve the diffusion barrier property, the TaN was treated by NH_3 plasma nitridation. Such nitrogen-plasma (N^+) nitridation is important to reduce the leakage current and improve the capacitance density. Then a 43-nm thick STO dielectric layer was deposited by RF sputtering with a ceramic target in a gas mixture of O_2/Ar, followed by subsequent 450 °C post-deposition anneal (PDA) for 30 min ~ 1 h under oxygen (O_2) ambient. It is important to notice that the device performance improvements with N^+ nitridation are due to the reduced interfacial TaON formation on TaN during PDA under O_2, as measured by secondary ion-mass spectroscopy (SIMS). However, such O_2 PDA is needed to reduce the oxygen deficiency in STO and improve the trap-assisted tunneling leakage current via defects in TaON. Finally, the TaN/Al metal was deposited and patterned to form both the top capacitor electrode and the RF transmission line. The fabricated RF MIM capacitors were characterized using a HP4284A precision LCR meter to 1 MHz, and the HP8510C network analyzer for S-parameters measurement to 10 GHz. The measured S-parameters were followed by a standard deembedding procedure using a dummy open device [5], [11]–[13]. The series parasitic impedances in RF transmission lines are also deembedded using a through dummy device [10]–[13]. The RF frequency capacitance value was extracted from measured S-parameters using an equivalent circuit model [5], [11].

III. RESULTS AND DISCUSSION

A. *C–V and I–V Characteristics*

Fig. 1 shows the C–V characteristics for TaN/STO/TaN MIM capacitors. A very high capacitance density of 35 fF/μm^2 or 0.99 nm capacitance-equivalent-thickness (CET) is measured at

Manuscript received March 15, 2005; revised May 12, 2006. This work was supported in part by the National Science Council, Taiwan, R.O.C., under Grants NSC 93-2215-E-009-001 and NSC 94-2215-E-009-062..

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Digital Object Identifier 10.1109/LMWC.2006.880709

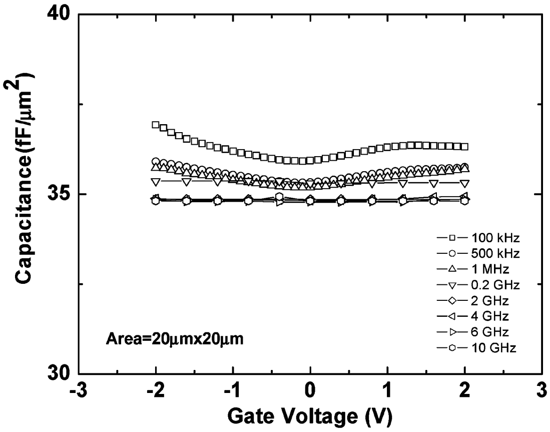


Fig. 1. C–V characteristics of TaN/STO/TaN MIM capacitors. Very high capacitance density of 35 fF/μm^2 is measured at 1 MHz with small capacitance variation. The C–V results from 100 kHz to 1 MHz are measured from LCR meter and the data from 0.2 GHz to 10 GHz are obtained from the S-parameters.

1 MHz. Such high capacitance density provides a 35 times area reduction than the $\sim$ 1 fF/μm^2 value provided by foundry [3]. In addition, a near constant capacitance value with little voltage and frequency dependence is obtained for the STO MIM capacitor, which is important for RF IC under large voltage swing condition. Such high capacitance density is due to the very high κ value of 169 in STO dielectric that is significantly larger than the κ $\sim$20 of HfO$_2$ used in current DRAM manufacture and also higher than the κ $\sim$45 in TaTiO MIM capacitors [10], [11]. Since the STO is also shown in the future DRAM technology roadmap [14], it is highly possible to integrate the RF capacitor with DRAM for multifunctional SoC application.

Fig. 2 shows the J–V characteristics of STO MIM capacitors. Small leakage current of 1×10^{-7} A/cm^2 is obtained at 1 V with high capacitance density of 35 fF/μm^2. Even at 2 V, the leakage current is still kept to only 7×10^{-7} A/cm^2. The small leakage current under positive bias voltage (electron injection from bottom electrode) indicates the good bottom STO/TaN interface. The higher leakage current under negative bias (electron injection from top TaN electrode) is attributed to the surface roughness as measured by Atomic Force Microscopy (AFM), which was originated from STO crystallization. However, such crystallization is needed for STO to give a much higher κ value than amorphous HfO$_2$ and TaTiO [10]. For a typical large 1-pF capacitor used in RF IC, a very small leakage current of only 29 fA is obtained due to the very high κ value, which is much smaller than the off-state current of a MOSFET with deep sub-100 nm gate length [12], [13].

B. High Frequencies Characteristics

Fig. 3(a) shows the measured S-parameters for the 35 fF/μm^2 density TaN/STO/TaN capacitors. The capacitance values at RF frequency were extracted using the equivalent circuit model in Fig. 3(b): the MIM capacitor is modeled by R_p and C, where the R_p originates from the high-κ dielectric loss. In addition, the R_s, L_{s1}, and L_{s2} represent the parasitic impedances in the coplanar transmission line used for RF measurements. Good agreement between measured and simulated data are obtained over the entire frequency range from 200 MHz to 10 GHz indicating the equivalent circuit model suitable and reliable for the TaN/STO/TaN modeling and capacitance value extraction.

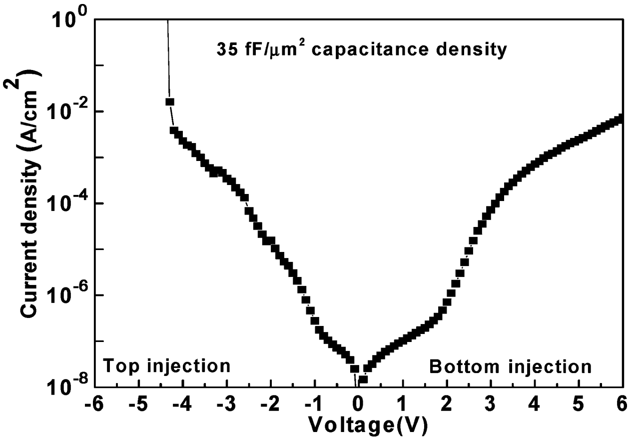
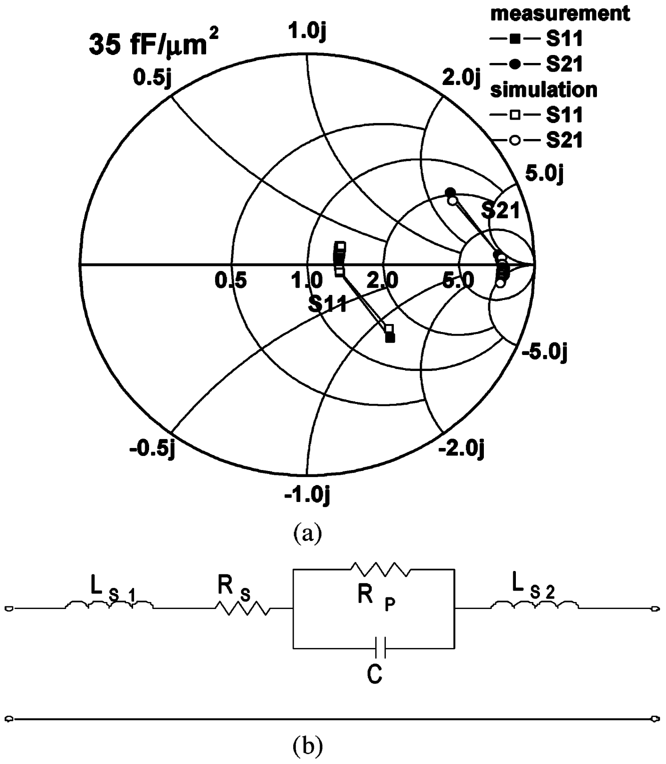


Fig. 2. Measured J–V characteristics of TaN/STO/TaN MIM capacitors with large 35 fF/μm^2 density.

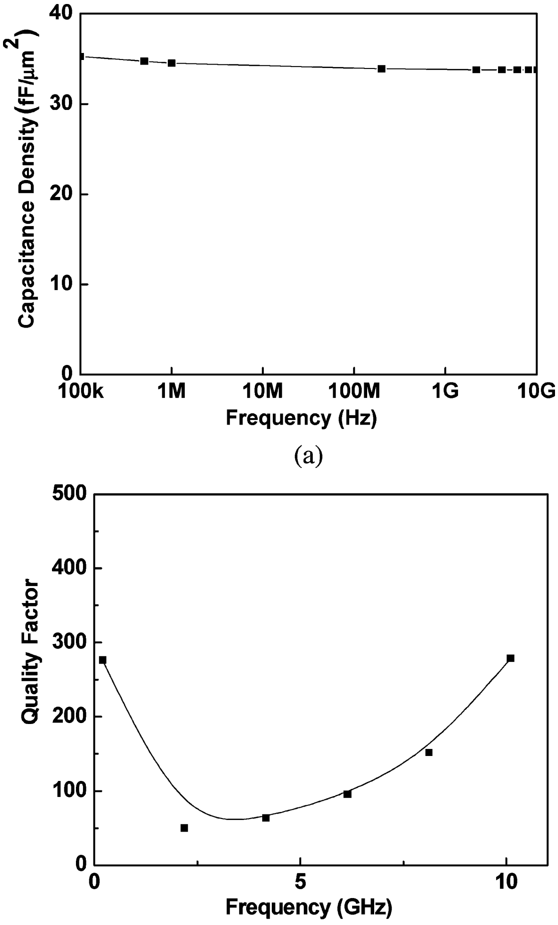


(a)

(b)

Fig. 3. (a) Measured and simulated two-port S-parameters for STO MIM capacitors, from 200 MHZ to 10 GHz. (b) The equivalent circuit model for capacitor value extraction from measured S-parameters.

Fig. 4(a) shows the dependence of capacitance density as a function of frequency, where the data at the RF frequency region is extracted from the circuit model with well matched S-parameters and the data at intermediate frequency (IF) are obtained from the measured C–V characteristics. A small capacitance reduction of only 4.1% from 100 kHz to 10 GHz is obtained indicating the good quality of device performance over the IF to RF range [10], [11]. The device quality (Q) factor is shown in Fig. 4(b), which was extracted from measured S-parameters



(a)

(b)

Fig. 4. (a) Frequency-dependent capacitance density and (b) Q-factor of TaN/STO/TaN MIM capacitors biased at 2 V.

using a circuit model [5], [11] at RF frequencies. A capacitance value of 14 pf was obtained and consistent to the 35 fF/μm^2 density measured by C–V. A good Q-factor >50 is obtained for RF application before a resonant frequency (f_r) of ~13 GHz, where the relative low f_r is due to the large capacitance.

IV. CONCLUSION

Very high 35 fF/μm^2 capacitance density, low capacitance reduction of 4% from 100 kHz to 10 GHz, and small leakage of 1×10^{-7} A/cm^2 at 1 V were simultaneously achieved in very high-κ TaN/STO/TaN MIM capacitors. This high density MIM capacitor is important for largely down-scaling the capacitance size and integration with DRAM.

ACKNOWLEDGMENT

The authors would like to thank G. W. Huang, National Nano-Device Laboratory, for his help with the RF measurements.

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