DC-Balance Low-Jitter Transmission Code for 4-PAM Signaling

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***Abstract*—This investigation proposes a novel dc-balanced low-jitter transmission code, a 4-PAM symmetric code, for a 4-PAM signaling system. The 4-PAM symmetric code preserves all of the useful characteristics of the 8B/10B code such as dc-balanced serial data and guaranteed transitions in the symbol stream for clock recovery. Moreover, the proposed method decreases the jitter of the timing transition of the data in the receiver and consumes half of the data bandwidth, because it transmits in 4-PAM. The design results using the UMC 0.18-μm process demonstrate that the new transmission code can decrease the jitter of the transition point by $\pm 25\%$ of the transition region. The operation speed of the encoder/decoder for the 4-PAM symmetric code is 819 MHz with 16-b inputs (13.1 Gb/s) and 704 MHz with 16-b outputs (11.3 Gb/s).**

***Index Terms*—Low jitter, 4-PAM, transmission code, 8B/10B code.**

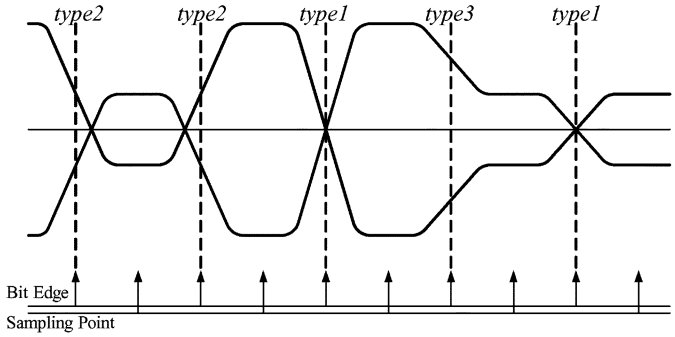

Fig. 1. Three transition types in the differential 4-PAM symbol stream. Type 1: central crossing; type 2: misplaced crossing; type 3: no crossing.

I. Introduction

In a serial-link data transmission system, a data clock is not transmitted with the data. In the receiver end, phase noise (jitter) in the generated clocks, phase alignment of the sampling clocks to the received high-speed data, and data jitter all influence system performance [1]. Therefore, clock generation and receiver timing recovery are crucial functions in a high-speed signaling system.

The 8B/10B data transmission method has become the standard for many high-speed serial links today [2]. This method belongs to the physical network layer and is utilized in IEEE 1394, 1/10 Gigabit Ethernet, asynchronous transfer mode (ATM) and fiber-optic transmission link, and includes serial encoding and decoding rules, special characters, and error detection functions. The encoding scheme creates a dc-balanced bit stream to ensure an equal number of positive and negative pulses to prevent signal distortions associated with ac coupling. Moreover, the scheme guarantees at least one signal transition for five transmitted bits in the symbol stream and thus provides sufficient transitions for clock recovery and significantly increases the probability of detecting single or multiple errors during data transmission.

The channel (e.g., cable or wire) bandwidth limitation increases the importance of 4-PAM signaling transmission, which only adopts half of the bandwidth of 2-PAM signaling [3]. This investigation proposes a novel dc-balanced low-jitter transmission code, a 4-PAM symmetric code. The 4-PAM symmetric code preserves all of the useful characteristics of 8B/10B code; moreover, it can decrease the jitter of the timing transition of the data in the receiver for 4-PAM signaling. The remainder of this investigation is organized as follows. Section II describes the design of the proposed 4-PAM symmetric code. Section III presents the architecture design and the implementation of the 4-PAM symmetric encoder/decoder. Finally, Section IV draws conclusions.

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II. Design of the 4-PAM Symmetric Code

A differential 4-PAM stream has three different transition types, as illustrated in Fig. 1. Of these three transitions, only type 1 makes a transition to the same magnitude but opposite polarity (symmetric transition). A type-1 transition generates a zero crossing precisely at the midpoint between two symbols and is therefore the most appropriate for clock recovery. Type-2 and type-3 transitions shall be avoided since they convey incorrect phase information [4]. For two adjacent 4-PAM symbols (e.g., symbol a and symbol b), we can have the formula

$$y = [\mathrm{MSB(a)} \oplus \mathrm{MSB(b)}] \cdot [\mathrm{LSB(a)} \oplus \mathrm{LSB(b)}] \qquad (1)$$

where $\oplus$ is the XOR operation and $\cdot$ is the AND operation. If $y = 1$, it means that this transition is a type-1 transition. Therefore, using (1), the receiver can detect the type-1 transition and ignore type-2 and type-3 transitions. To improve the jitter on the data transition, a 4-PAM symmetric code is proposed, providing at least one type-1 transition of the differential 4-PAM signal for every ten transmitted symbols. By the 4-PAM symmetric coding scheme, the differential 4-PAM data streams have sufficient density of type-1 transitions, and only type-1 transitions perform synchronization in the receiver. By doing so, it

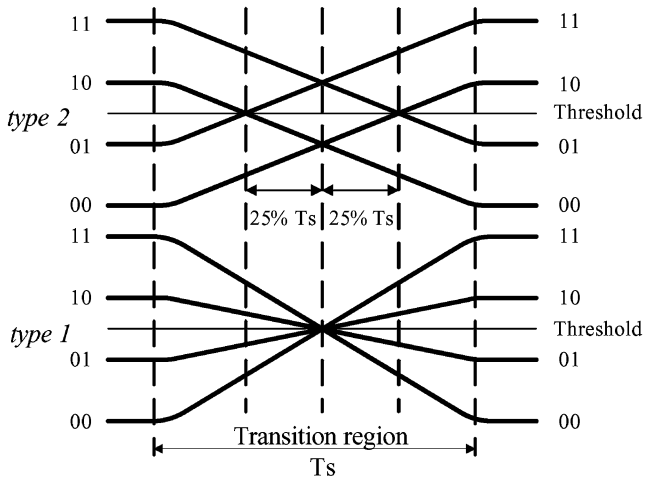


Fig. 2. Comparisons of type-1 and type-2 transitions in the differential 4-PAM signals.

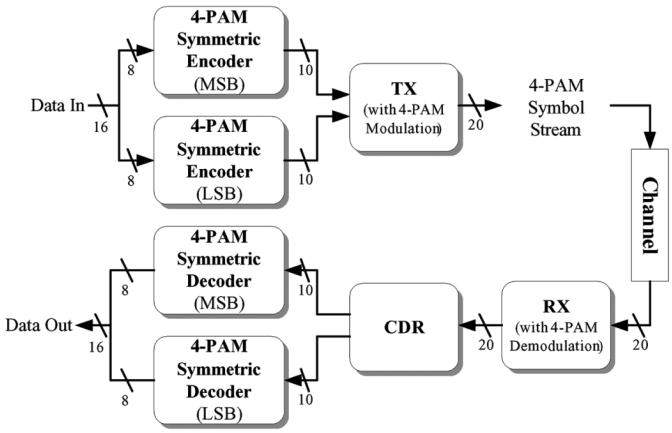


Fig. 3. Structure of 4-PAM symmetric encoders and decoders for a 4-PAM signaling system.

will reduce the jitter by $\pm 25\%$ of the data transition region (Ts) as illustrated in Fig. 2.

A. Structure of 4-PAM Symmetric Code

The 4-PAM symmetric code translates byte-wide data into a 10-b serial data stream as the 8B/10B transmission code. The proposed 4-PAM signaling structure adopts parallel inputs of 16-b data to two 4-PAM symmetric encoders, each of which has 8-b data input, as depicted in Fig. 3. The two encoders encode the MSB and LSB part individually and output 20-b data from LSB and MSB encoders outputs. The MSB and LSB output bits are combined to generate one symbol with four levels in amplitude. A data rate of 10 Gb/s requires a line rate of 6.25 GBd (one symbol transmitted two bits). Thus, the output of both the MSB encoder and the LSB encoder consists of two 10-b data words clocked at 625 MHz (which is equivalent to 10 Gb/s in the source data). Therefore, the 4-PAM symmetric code for 4-PAM transmission requires only half of the bandwidth required for 2-PAM transmission.

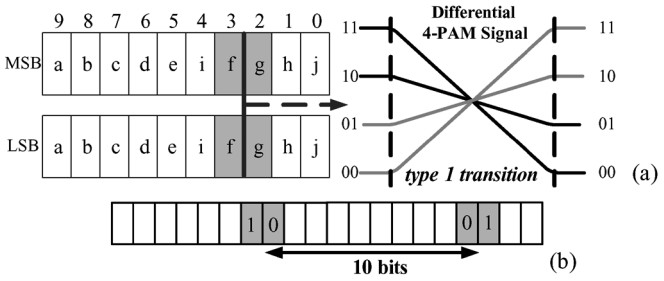


Fig. 4. (a) Type-1 transition in the 4-PAM symmetric code and (b) frame synchronization.

B. Low Jitter of Data Transitions

In every cycle (ten symbols), the 4-PAM symmetric code guarantees at least one type-1 transition, which is different from that of the 8B/10B encoder in the differential 4-PAM signal. To obtain the type-1 transition of the differential 4-PAM signal, bits 3 and 2 of the 4-PAM symmetric code must always be coded for (1, 0) or (0, 1), as illustrated in Fig. 4(a) with f $=\sim$ g. Combining one MSB bit and one corresponding LSB bit forms one symbol, and then symbol 3 to symbol 2 will be 11/00 to 00/11 or 01/10 to 10/ 01. Therefore, symbol 3 to symbol 2 produces a type-1 transition, and at least one type-1 transition is generated in every ten symbols. Furthermore, the third symbol of every ten symbols experiences a type-1 transition, and we can obtain the ten-symbol frame synchronization by observing the data stream to find the intervals with the highest average density of type-1 transitions, as illustrated in Fig. 4(b).

C. Design Concept of Running Disparity

DC balancing is achieved by running disparity. The disparity designates the difference between the numbers of 1's and 0's in a defined block of digits or the instantaneous deviation from the long-term average value of the running digital sum. The 4-PAM symmetric encoder translates byte-wide data into a 10-b serial data stream composed of 6-b and 4-b subblocks. The serial data stream controls the numbers of 1's and 0's in each subblock transmission to help balance the dc level between the voltage levels denoting 1 and 0. No distinction is made between 6-b and 4-b subblocks, which are therefore used to compensate for each other.

The unit cell concept is used to explain running disparity of the 4-PAM symmetric code. Fig. 5 plots the disparity (rd) as a function of time or digit intervals (n). For a binary or two-level code (d), each 1 is denoted by a line segment extending over a one-digit interval and rising at a 45° angle, and a 0 is denoted by a falling line. A waveform corresponding to a possible signal during a unit interval is assigned an algebraic value corresponding to its dc component. The 1's and 0's are typically assigned values of $+1$ and -1, respectively. The formula of disparity is

$$\mathrm{rd(n)} = \mathrm{rd(n-1)} + (-1)^{\mathrm{d}+1}. \tag{2}$$

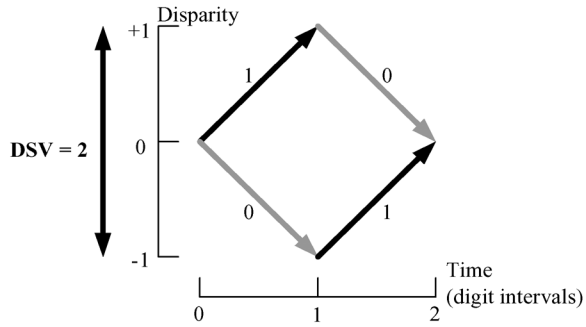


Fig. 5. Unit cell of running disparity.

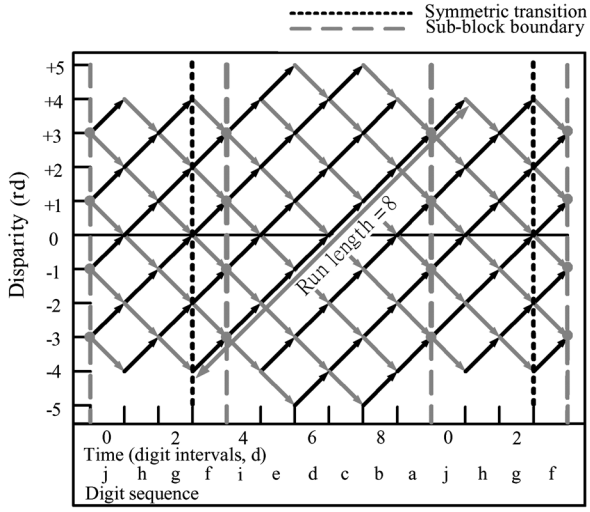


Fig. 6. Disparity versus time plot.

The digital sum variation (DSV) is given as the variation in the running disparity sum of the encoded data stream.

Individual 6-b and 4-b subblocks are complemented in accordance with disparity rules, and the difference between the number of 1's and 0's is always 0, ± 2, or ± 4. The running disparity is positive ($+1$ or $+3$) if two or four more 1's than 0's have been transmitted, respectively, and negative (-1 or -3) if two or four more 0's than 1's are transmitted. The running disparity remains unchanged from the previous transmission if the code contains an equal number of 1's and 0's. As illustrated in Fig. 6, all subblock boundaries have running disparity values of ± 1 or ± 3, which are different from the 8B/10B code boundaries of ± 1. The running disparities of ± 1 and ± 3 make very little difference to the long-term average dc offset. Fig. 6 clearly demonstrates that the disparity (or DSV) is bounded and that the run length of the 4-PAM symmetric code is eight, because a fixed type-1 transition occurs in the bit 3 and bit 2 positions. The DSV bounded range makes the resultant code dc-balanced, i.e., zero spectral power at zero frequency, which is one of the most frequently required code characteristics in transmission via ac-coupled channels.

D. Error Detection

Like the 8B/10B code design concepts, the error detection in the 4-PAM symmetric code can be implemented in two ways.

TABLE I
8B/10B, 8B5Q AND 4-PAM SYMMETRIC TRANSMISSION CODES FOR THE 4-PAM SYSTEM

	8B/10B Code	8B5Q Code	4-PAM Symmetric Code
DC-balanced	Yes	No	Yes
Bounded disparity	(+1,-1)	No	(+3,+1,-1,-3)
Run length	5 bits	No	8 bits
Error detection	Yes	No	Yes
Low jitter for timing recovery	No	Yes	Yes
Frame synchronization	No	No	Yes

The first approach checks each packet transmitted for redundancy. Additionally, the first approach validates the transmission of each packet, using a media access control (MAC) layer to identify errors based on the start and end delimiters. A delimiter is a special character that characterizes synchronization. The second approach adopts cyclic redundancy checking (CRC) to identify errors on individual 6-b or 4-b code blocks. If the code is a legal 4-PAM symmetric code and does not violate the disparity rules, then no errors arise. In addition to 256 data characters, the 4-PAM symmetric code defines 12 out-of-band indicators which are the same as those of the 8B/10B code and are called special control characters. Special characters are typically used for transmitting link diagnostics and codewords such as ABORT, RESET, SHUTDOWN, and IDLE.

E. Comparison of Transmission Codes

Another novel transmission code 8B5Q that encodes 8 bits into five 4-PAM symbols removing all full-swing transitions to reduces the baud rate and achieves low jitter of timing recovery [5]. For the 4-PAM system, Table I gives the comparison of the 8B/10B code and the 8B5Q code with the 4-PAM symmetric code. The 4-PAM symmetric code has good characteristics, including dc-balanced, finite run-length, special characters, and error detection as the 8B/10B code. For the 4-PAM system, the 4-PAM symmetric code can guarantee sufficient type-1 transitions for low jitter of timing recovery, but the 8B/10B code does not have such a property. The 8B5Q code reduces the jitter of timing recovery for the 4-PAM system, but does not have good characteristics like those of the 8B/10B code and the 4-PAM symmetric code.

III. ARCHITECTURE AND IMPLEMENTATION OF A 4-PAM SYMMETRIC ENCODER/DECODER

The overall block diagram of the 4-PAM symmetric encoder architecture is illustrated in Fig. 7. The straightforward data flow of 4-PAM makes it easy to pipeline to speed up the encoding rate. In this case, the encoder is partitioned into three stages so that it can operate at 13.1 Gb/s. A character is encoded in four clock cycles. The 4-PAM symmetric encoder is clocked by a byte rate clock (*clk*). The *Adder* block estimates the number of 1 s in *data_in[7:0]*, as demonstrated in Fig. 7. The *Disparity*

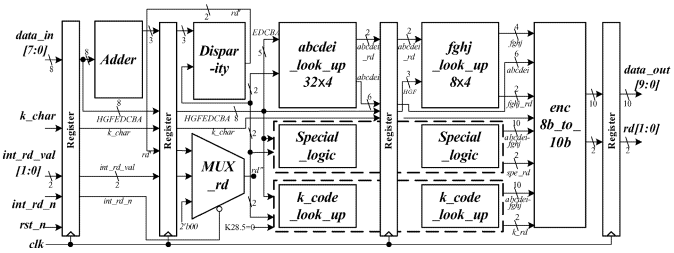


Fig. 7. Block diagram of the 4-PAM symmetric encoder.

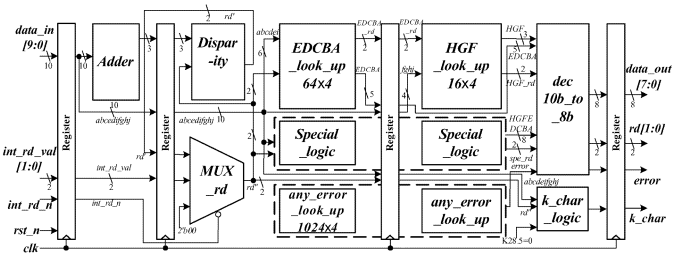


Fig. 8. Block diagram of the 4-PAM symmetric decoder.

block predicts the next state running disparity state based on the number of 1's of *data_in[7:0]*.

The *MUX_rd* block specifies the running disparity from the reset mode signals *int_rd_val[1:0]* or the *Disparity* block output. The control signal *k_char* denotes whether the *data_in[7:0]* represents data or control information. For encoding, each incoming byte is split into two subblocks. The five binary lines *EDCBA* (*data_in[4:0]*) are encoded into the six binary lines *abcdei* by the*abcdei_look_up* block. Similarly, the three bits *HGF* (*data_in[7:5]*) are encoded into the four bits *fghj* by the *fghj_look_up* block. The disparity of each subblock indicates the difference between the numbers of 1's and 0's, where positive and negative disparity numbers represent an excess of 1's and 0's, respectively. The permitted disparity of both *abcdei* and *fghj* is 0, ± 4, or ± 2. Therefore, encoding scheme is dc free by complementing the disparity of each subblock.

The *Special_logic* block encodes the eight bits *FGHEDCBA* (*data_in[7:0]*) into the ten bits *abcdeifghj* when *FGHEDCBA* cannot directly be encoded by the *abcdei_look_up* and *fghj_look_up* blocks. When the signal *k_char* is high, the *k_code_look_up* block generates special characters. Finally, the *enc8b_to_10b* block integrates the above results and determines the final outputs (*rd[1:0], data_out[9:0]*).

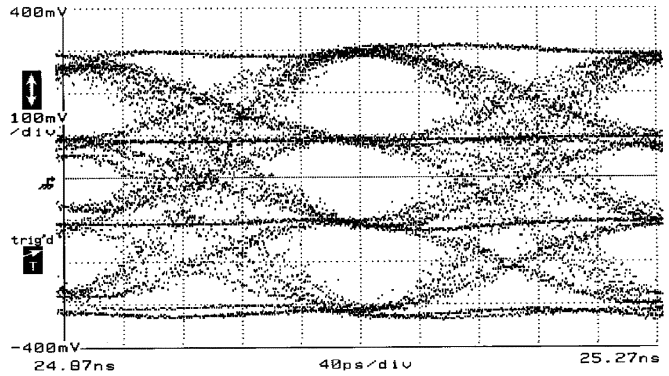
The overall block diagram of the 4-PAM symmetric decoder architecture is illustrated in Fig. 8. In this case, the 4-PAM symmetric decoder is pipelined, and therefore a character is decoded in four clock cycles. The 4-PAM symmetric decoder is clocked by a byte rate clock (*clk*). As demonstrated in Fig. 8, the *Adder* block is applied to estimate the number of 1's in *data_in[9:0]*, which is employed by the *Disparity* block to predict the next state of running disparity. The *MUX_rd* block determines the running disparity from the reset mode *int_rd_val[1:0]* or the *Disparity* block output. For decoding purposes, each incoming 10-b data is partitioned into two subblocks. The *EDCBA_look_up* block then decodes the six binary lines *abcdei data_in[9:4]*) into five binary lines *EDCBA*. Similarly, the four bits *fghj data_in[3:0]*) are decoded into the three bits *HGF* by the *HGF_look_up* block. The disparity of each subblock of the incoming data is the difference between the number of 1's and 0's; positive and negative disparity numbers denote an excess of 1's and 0's, respectively. For both the *abcdei* and *fghj*, the permitted disparity is 0, ± 2, or ± 4. The *Special_logic* block decodes the ten bits *abcdeifghj data_in[9:0]*) into eight bits *HGFEDCBA* when they cannot be directly decoded by the *EDCBA_look_up* and *HGF_look_up* blocks. The *abcdeifghj* value is uniquely decoded according to only the *HGFEDCBA* value, without any reference to disparity or other parameters. However, because of the propagation properties of the 4-PAM symmetric code that may identify many errors and output to the *error* signal by the *any_error_look_up* block, even a single-bit error might not be discovered until several characters after the error is introduced. The *k_char_logic* block determines whether the *data_in[9:0]* denotes data or control information and generates the *k_char* signal. If the *k_char* signal is high, then the *data_in* contains a special character; otherwise, it contains a data character. Finally, the *dec10b_to_8b* block integrates the above results and obtains the final outputs *rd[1:0]*, *k_char*, *data_out[7:0]*, and *error*.

TABLE II
SYNTHESIS RESULTS OF THE 4-PAM SYMMETRIC ENCODER/DECODER

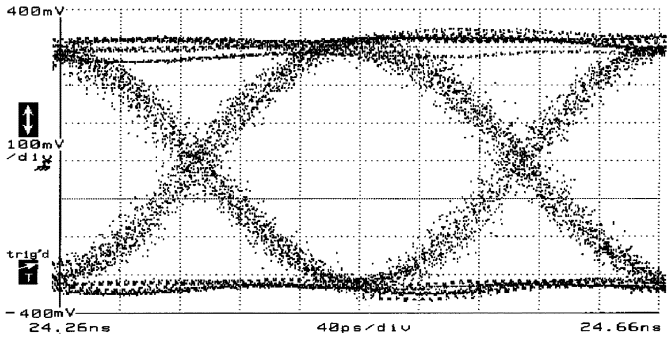
	4-PAM Symmetric Encoder	4-PAM Symmetric Decoder
Technology	UMC 0.18um	
Maximum Clock rate / Throughput	819 MHz /13.1 Gbps (16-bit intput)	704 MHz /11.3 Gbps (16-bit output)
Cell Area (gate count)	2506	2915

A 4-PAM symmetric encoder/decoder were implemented using UMC 0.18-μm standard cell to synthesize the design. The results are summarized in Table II. For the source data rate to achieve 10 Gb/s, the area of the 4-PAM symmetric encoder/decoder must be larger than the 8B/10B encoder/decoder by 1000$\sim$1500 gate count. The area is measured in equivalents of two-input NAND gates.

Fig. 9 shows the measurement results of a devised 4-PAM serial-link transmitter [6] outputs with all types of transitions (like the 8B/10B for 4-PAM signaling) and data containing only a maximum-swing type-1 transition. The measurement results operated at 10 Gb/s and Ts is about 0.6 unit interval (UI). These results demonstrate the peak-to-peak jitter of all types of transitions, and the jitter of only maximum-swing type-1 transitions are about 0.75 and 0.25 Ts. The measurement results are in agreement with our estimation. Therefore, in the receiver, if the 4-PAM symmetric coding scheme with only type-1 transitions is used, then the timing jitter of the data can be decreased by $\pm 25\%$ Ts. When the data or clock jitter decreases, the bit error rate (BER) will decrease exponentially [1]. For example, assume that the standard deviation of clock jitter is 0.02 UI and Ts is about 0.16 UI. In an ideal situation, the data jitter of the data stream encoded by a 4-PAM symmetric code and uncoded data



(a)



(b)

Fig. 9. Measurement results [6] of (a) all types of transitions and (b) only maximum-swing type-1 transitions of the differential 4-PAM signal.

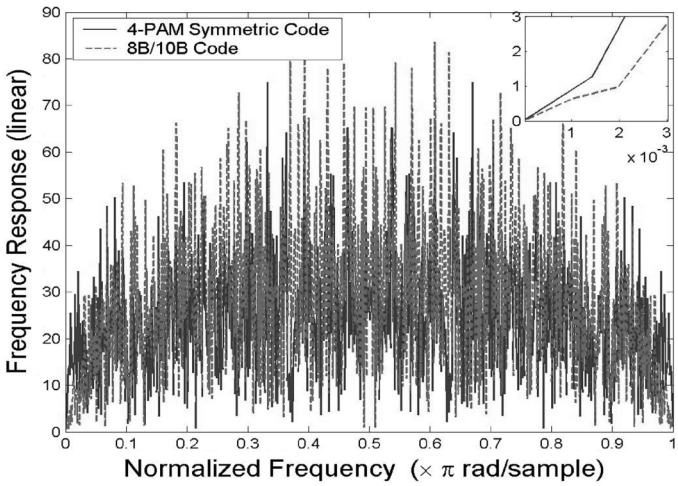


Fig. 10. Frequency responses of the 4-PAM symmetric code and the 8B/10B code.

stream are $0/\pm 25\%$ Ts. The BERs are about $10^{-15}/5\times 10^{-13}$ for encoded/uncoded data, respectively.

The 4-PAM symmetric code can also be used in a 2-PAM system (binary) and preserve all useful characteristics of the 8B/10B code. Fig. 10 displays the frequency responses of a random binary data stream encoded by the 4-PAM symmetric code and the 8B/10B code and demonstrates that the 4-PAM symmetric code, like the 8B/10B code, has zero spectral power at zero frequency. Therefore, the 4-PAM symmetric code is dc-balanced. Although the 4-PAM symmetric code has frame synchronization, the frequency response of the 4-PAM symmetric code does not exhibit any strong tones. The frequency response of the 4-PAM symmetric code is similar to that of the 8B/10B code.

IV. Conclusion

This investigation presents a novel low-jitter transmission code, the 4-PAM symmetric code, for 4-PAM signaling in serial links. The proposed method preserves all of the good characteristics of the 8B/10B code, such as dc-balanced, finite run-length, error detection, and special characters. Furthermore, the 4-PAM symmetric code guarantees at least one type-1 transition every ten transmitted symbols and thus can decrease the jitter of transition time by $\pm 25\%$ Ts in the 4-PAM system. Using a UMC 0.18-μm standard cell, 13.1-Gb/s/11.3-Gb/s encoding/decoding can be attained with about 2506/2915 gates.

Acknowledgment

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