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Prospect of cobalt-mix-tetraethoxysilane method on localized lateral growth of carbon nanotubes for both *p*- and *n*-type field effect transistors

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To apply carbon nanotubes (CNTs) to nanoelectronics, researchers must effectively control the placement and manipulation of massive numbers of CNTs. In this work, we demonstrate a precise growth of single-walled carbon nanotubes (SWNT) on preassigned locations with only cobalt as catalyst. This is in contrast to the laborious and time-consuming physical manipulation of numerous nanotubes one at a time used in the conventional approach. Laterally grown CNTs were accomplished in preassigned areas using an integrated circuit compatible process in this study. In order to synthesize SWNT as the channel of a field effect transistor (FET), the cobalt-mix-tetraethoxysilane (CMT) solution and catalytic chemical vapor deposition were used. The CMT solution has the unique property of well dispersing the cobalt catalyst and uniformly embedding it in predetermined locations after the CMT solution has solidified. Our results show that laterally grown bundled-CNTs could be formed in atmospheric chemical vapor deposition with ethanol, by properly controlling the temperature of process, the process time, and the hydrogen reduction time. Since our bundled-CNTs were exposed to the air, all the as-grown CNT-FETs we manufactured exhibit *p*-type characteristics. Furthermore, we also demonstrate air-stable *n*-type CNT-FETs successfully without resorting to any additional and complicated annealing process by simply depositing a silicon nitride film on the as-grown *p*-type devices by plasma enhanced (PECVD) at 390 °C. The use of prepatterned catalyst islands, CVD method, and flexibility of simultaneously manufacturing both *n*- and *p*-type CNT-FETs may open a new era for applications of CNT-based nanoelectronics. © *2006 American Vacuum Society.* [DOI: 10.1116/1.2345207]

I. INTRODUCTION

The carbon nanotube (CNT) is a hollow tube composed of carbon atoms with its diameter ranging from a few nanometers to tens of nanometers. CNTs have been extensively studied and analyzed since their discovery[1] in 1991 as their excellent electrical and mechanical properties appear to be promising for many micro- and nanoelectronic applications, such as field-emission displays,[2] sensors,[3,4] and field-effect transistors[5] (FET). A CNT has several impressive properties, including ultrahigh mobility, high current density capacity, and a suitable on/off ratio for FET purposes.[6] Generally, CNTs depict two different types of electrical characteristics (i.e., metallic or semiconducting type), depending mainly on the CNTs' chirality. Since CNTs exhibit two different types of electrical properties, they can be employed as FETs as well as interconnects/vias/contact holes. However, there are challenges that need to be tackled before their adoption to many practical applications, especially the process compatibility with the existing silicon-based semiconductor technologies, controlling the placement and manipulation of massive numbers of CNTs at precise locations, the chirality of the CNTs, and the manufacturing of both *n*- and *p*-type CNTs simultaneously on the same substrate. Among these challenges, an effective method must be developed for efficiently controlling the placement of massive numbers of CNTs because conventional silicon-based micro- or nanoelectronics often consist of millions of devices. To use CNTs as a replacement building block for silicon-based devices, millions or even billions of nanotubes must be placed accurately over the chip. It is obvious that the physical manipulation of numerous nanotubes one at a time is laborious and impractical for mass production, thus the ability to form massive numbers of CNTs in precise locations remains a key issue for CNTs in nanotechnology applications. A number of techniques have been proposed to achieve a regular CNT network by controlling the gas flow direction,[7] using porous

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templates,[8] using electric-field-assisted assembly,[9,10] utilizing chemically functionalized template,[11] adopting fluidic alignment,[12,13] or using electric-field-directed-growth of CNTs.[14] Although these methods all achieve acceptable results in both the growth direction and the length of CNTs, they require additional equipments.[15] It is obvious that the aligned-CNT-growth methods[16] are more promising than postgrowth-assembly-of-CNT methods for CNT-FETs. One of the aligned-CNT-growth methods, which has emerged as the most popular method, involves the catalytic disproportionation of carbon source (carbon monoxide usually) on bimetallic catalysts containing molybdenum/cobalt in chemical vapor deposition (CVD) system.[17]

Although catalytic mixtures of cobalt (Co) and molybdenum have been considered essential for the growth of single-walled carbon nanotubes (SWNTs) from carbon monoxide or hydrocarbons by the CVD method, we demonstrate, the growth of bundled-CNTs with only Co particles as the catalyst[18,19] and ethanol as the carbon source in this work. Some previous reports also indicated that CNTs manufactured by CVD methods with a Co catalyst usually resulted in predominantly multiwalled tubes.[20,21] In this article, our reiterative and systematic experiments show that the selective growth of bundled-CNTs produces mostly SWNTs.

For CNT-FETs and biosensors, it is necessary to employ SWNTs instead of multiwalled carbon nanotubes (MWNTs) because of the unique semiconducting property of the SWNTs. In order to obtain SWNTs, the catalyst size should be reduced to as small as possible.[18] In this work, a method is proposed to synthesize SWNTs and form bridged-CNTs between two catalyst islands. The dominant parameters in the aligned growth of SWNTs are found to be the size and the location of catalyst nanoparticles. The characteristics of embedded Co nanoparticles in patterned cobalt-mix-tetraethoxysilane (CMT) islands for SWNT growth are discussed under different hydrogen reduction conditions, catalyst concentrations, and carbon ratios during CNT growth.

Since for the mainstream complementary metal-oxide-semiconductor (CMOS) circuit applications, both *p*- and *n*-type metal-oxide-semiconductor field effect transistors are called for simultaneously on the same chip. It is thus necessary to fabricate *n*-type, in addition to *p*-type CNT-FETs, on the same chip for the complementary circuits. In general, the CNT-FET acts like a p-type conduction device when the CNT is exposed to air.[22–26] However, it is quite difficult to manufacture *n*-type CNT-FETs. Several approaches have been previously reported to form *n*-type CNT-FETs by employing complex doping processes (i.e., adopting alkali metals)[27–29] or thermal/electrical annealing processes.[30] These approaches, however, require extra processing and masking steps to convert generic *p*-type CNT-FETs in vacuum or in the inert gas. In contrast, no extra annealing steps are needed to form air-stable *n*-type CNT-FETs[31–33] using the passivation method proposed in this study (details are described in Sec. III F).

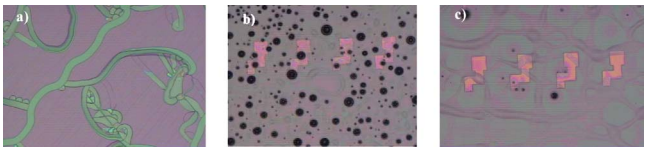

FIG. 1. Influence of moisture and stirring time on the preparation of CMT solution. (a) CMT film cracks after first soft bake (CMT was exposed to moisture when stirred). (b) Co particles aggregate together after first soft bake if the CMT solution without proper stirring. (c) Co particles disperse well after first soft bake with proper stirring of the CMT solution. Note that the patterns in (b) and (c) are predefined n^+-poly bottom gate electrodes.

II. EXPERIMENT

A. Preparation of cobalt-mix-tetraethoxysilane solution and formation of catalyst islands

First, 25 ml tetraethoxysilane [(TEOS) reagent grade] was added into 25 ml absolute alcohol (ethanol) and slowly stirred for 20–30 min, then 1.5 M Co^{2+} [$Co(NO_3)_2 \cdot 6H_2O$ +ethanol] solution was added slowly over 90 min by using clean burette ($\sim$10 ml/90 min@$23\pm2\,^{\circ}C$ and relative humidity: $43\% \pm 5\%$ in class 10 clean room). After adding Co^{2+}, cares were taken to protect the solution from moisture, and the solution was stirred slowly for over 24 h. It should be noted that if the solution was exposed to moisture or stirred unevenly, the CMT film would crack easily after the first 133 °C soft bake as shown in Fig. 1(a). Figure 1(b) shows that lots of Co particles are aggregated together if the stir time is shortened to about 12 h. Figure 1(c) shows that the Co particles will disperse well if the CMT solution is stirred long enough under a well-controlled environment.

Figure 2 illustrates a bridged-CNT FET process flow of the proposed CMT method. In order to fabricate CNT-FETs, the gate dielectric layer under the CNT channel must first be considered. Different gate dielectric layers would exhibit different surface characteristics and the choice of this layer would be critical for the dispersion of the CMT solution. In the proposed process, a 600 nm field oxide (SiO_2) layer was first grown as an insulating layer by wet oxidation at 985 °C on the 4-in. *p*-type silicon wafers. Then, a 300–350 nm n^+-poly silicon layer was deposited by low-pressure CVD, and subsequently patterned and etched to serve as the bottom-gate electrodes. Afterwards, another oxide or nitride layer was grown on the wafers to serve as the gate insulator [Fig. 2(a)]. Then the CMT solution was spun onto the gate dielectric layer as the catalyst layer. The oxidation and activation of the CMT layer were carried out by a prebake at 133 °C in the atmosphere, followed by a hot-bake at 550 °C in an argon (Ar) environment. After the annealing process, the catalyst islands were patterned on the CMT layer by using standard lithography and dry/wet etching processes [Fig. 2(a)].

B. Growth of carbon nanotubes

The growth of CNTs was conducted in a customized quartz tube reactor placed in a horizontal tubular furnace. After the formation of catalyst islands described in Sec. II A,

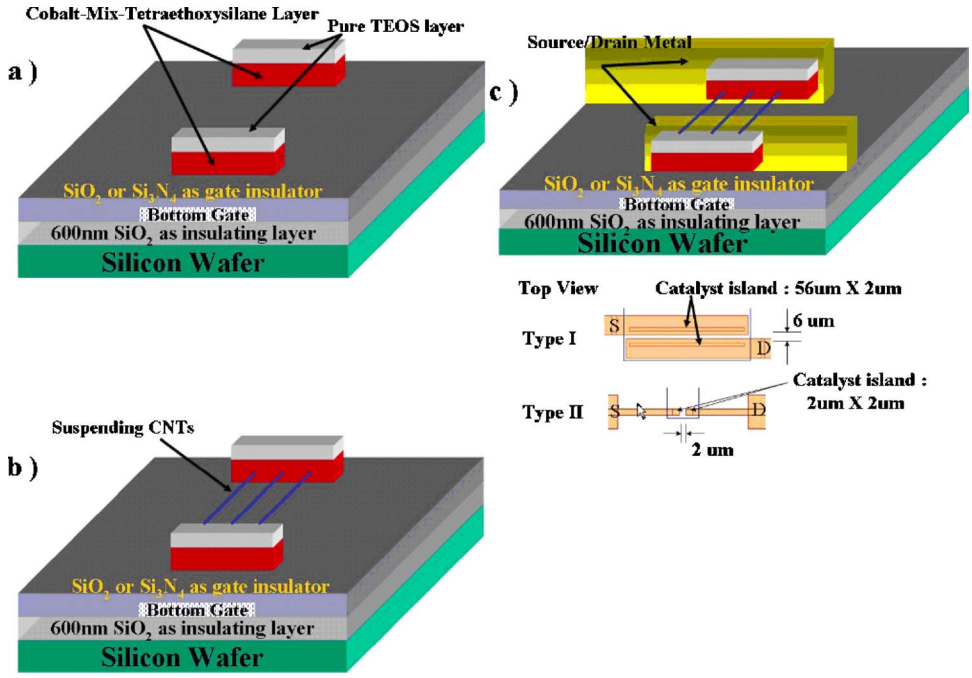

FIG. 2. Process flow for the growth of bundled-CNTs. (a) Catalyst mixed TEOS (CMT) and pure TEOS layers were spun on oxidized substrate with patterned bottom gates, followed by photolithography and RIE processes to form the CMT catalyst islands. (b) Growth of suspending SWNTs connecting two neighboring catalyst islands. (c) Ti metal lift-off process to form the S/D electrodes. The inset of Fig. 2(c) shows two kinds of catalyst islands and S/D metal pads in our layout design. Note that the individual bottom n^+-poly gate and the gate oxide or nitride layer were both formed before the CMT was spun.

wafers were heated in pure H_2 for 5–15 min at 550 °C to convert Co^{2+} to metal particles. Then the process temperature was raised to 850 °C in Ar at a flow rate of 5000 sccm, and subsequently ethanol was introduced into an atmospheric CVD (APCVD) furnace as the carbon source with Ar as the carrier gas at a flow rate of 3500–5000 sccm for 40 min in ambient atmosphere. After completion of the reaction, the power was turned off and the reactor was cooled down under flowing Ar. Finally, the suspended CNTs were grown between two neighboring catalyst islands by APCVD with ethanol/Ar [Fig. 2(b)].

After blanket coating a photoresist layer, and using a photolithographic step with a negative source/drain (S/D) pattern mask to etch away the photoresist from the S/D area, a titanium (Ti) layer was deposited by radio frequency sputtering at room temperature. Next, an ultrasonic instrument and acetone were used for the Ti lift-off process, leaving the Ti film only on the S/D regions [Fig. 2(c)]. The spacing between the source and the drain electrodes was designed to be 2 μm (i.e., the channel length of the devices).

A commercial HP-4155A was applied for measuring the I_d-V_g transfer curves and I_d-V_d of the CNT-FETs. The raw nanotubes were examined by high-resolution transmission electron microscopy (TEM) (JEOL JEM 2000EX).

III. RESULTS AND DISCUSSIONS

A. Transition metal contamination

Since an integrated circuit (IC)-compatible process is highly desirable, we adopt a standard IC process to manufacture our catalyst islands and grow the CNTs. However, the catalyst metals, which belong to the transition metals, can potentially contaminate the expensive semiconductor equipments. As such the foundry is usually reluctant to allow such materials to enter their production lines. When the dimensions of integrated circuits become smaller, the thickness of the gate oxide is being reduced to virtually atomic levels. With oxide thicknesses being less than a few tens of angstroms, the metal impurities can have serious effects on the oxide properties. Generally, transition metals, such as Fe, Co, Ni are commonly used as catalysts for carbon nanotube growth. Unfortunately, these transition metals can be unintentionally left on the surface of the chamber at a number of processing steps ranging from wet chemical etching, dry etching, photolithography, and chemical vapor deposition. Therefore, trace transition metals analysis has become essential for the development of CNT processes that are compatible with silicon circuit technologies.

In order to clarify the contamination issue, monitors were set up to measure the cobalt ion concentration in the process chambers (including loadlock chambers and robot arms). The key machines monitored included dry etchers and the CVD machine (Table I). In addition, particle levels were also monitored in our I-line stepper, chemical stations, and spin dryers. The monitor results showed that the monitored particle levels were quite normal (within our specification). In our study, VG-PQ3, an inductivity coupled plasma-mass spectrometer, was used to analyze the monitor wafers which were processed by the semiconductor equipments in question. From Table I, we can conclude that no noticeable increase in cobalt ion concentration is observed.

TABLE I. Co^{2+} residues in major process equipments

	Metal etcher	Chemical vapor deposition chamber	Dry etcher
Background wafer (before cobalt process)	3546 ppt	1015 ppt	3858 ppt
Monitor wafers (after cobalt catalyst processings)	Wafer No. 11: 2736 ppt Wafer No. 04: 1890 ppt	Wafer No. 20: 966 ppt Wafer No. 14: 2102 ppt	Wafer No. 09: 4297 ppt Wafer No. 10: 2445 ppt
Monitor wafers (dry/wet cleaned after Co catalyst processings)	Wafer No. 18: 2059 ppt (wet clean)	Wafer No. 08: 3204 ppt (dry clean)	Wafer No. 17: 3509 ppt (dry clean)

B. Diameter of cobalt catalyst

Figure 3(a) shows the TEM picture of Co catalyst distribution in CMT powder. The diameters of the embedded Co catalysts range between 10 and 20 nm, which is a parameter crucial to confining the width of the CNTs. Figure 3(b) demonstrates the bundled-SWNTs that were synthesized from CMT powders with a diameter of 10 nm. After the SWNTs were grown, some bridged SWNTs were found between the CMT powders, as shown in Fig. 3(c). These results suggest that the CNT bundle can indeed be naturally bridged between two CMT catalyst islands. It is worth noting that the diameters of Co catalysts are strongly related to the formation procedure of CMT described in Sec. II B such as the stir time and process environment.

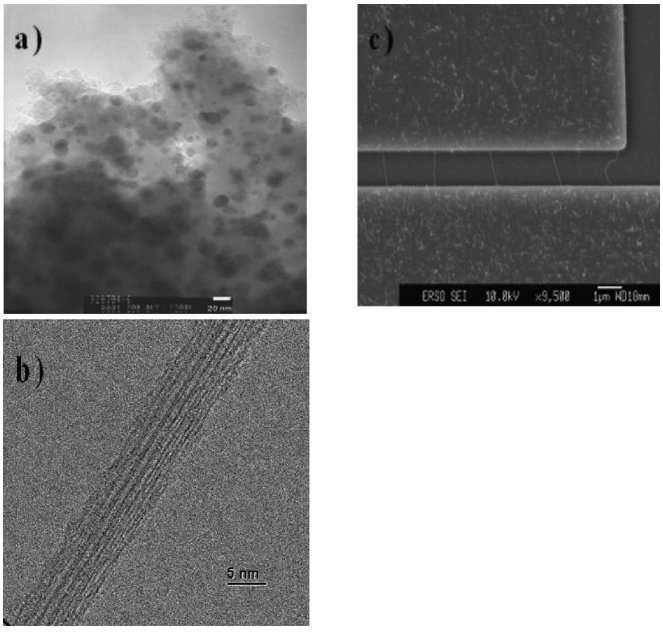

FIG. 3. TEM pictures for CMT layer and bridged-CNT. (a) Cobalt nanoparticle uniformly embedded in oxide layer. (b) Bundled-SWNT synthesized from CMT powders with 10 nm in diameter. (c) Many bridged SWNTs were formed between the CMT catalyst islands.

C. Adhesion of the CMT layer on different bottom gate dielectric layers

In this study, we investigate the dispersion/adhesion of our CMT on different bottom gate dielectric layers (i.e., either thermal oxide or nitride). Figure 4 shows that the CMT can disperse/adhere well and can be patterned well (by dry etching), as evidenced by the vernier structure (i.e., the arabic numerals in the scanning electron microscopy (SEM) pictures is an indicator for the resolution of photolithography and the finest pattern after dry etching) on thermal oxide layer. Unfortunately, the oxide bottom gate dielectric layer with its hydroxyl (–OH) bonds is undesirable for many biosensor applications. To avoid the complication of hydroxyl bonds, nitride in lieu of oxide can be adopted as the bottom gate dielectric layer. However, our data show that the adhesion of CMT layer on nitride is quite poor [Fig. 4(b)], so the direct spinning of the CMT solution on nitride film is not

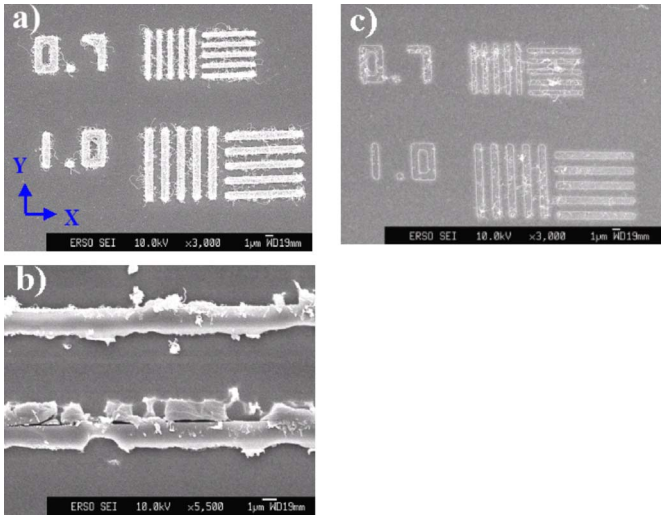

FIG. 4. Adhesion of CMT layer on different layers. The vernier structure (i.e., the scale bars) indicates the resolution of photolithography and the finest pattern after dry etching. (a) CMT spun well on thermal oxide layer. (b) Poor adhesion of CMT layer on nitride. (c) By adding a HMDS layer before CMT spinning, good CMT catalyst islands are obtained on nitride layer suitable for biosensor purposes.

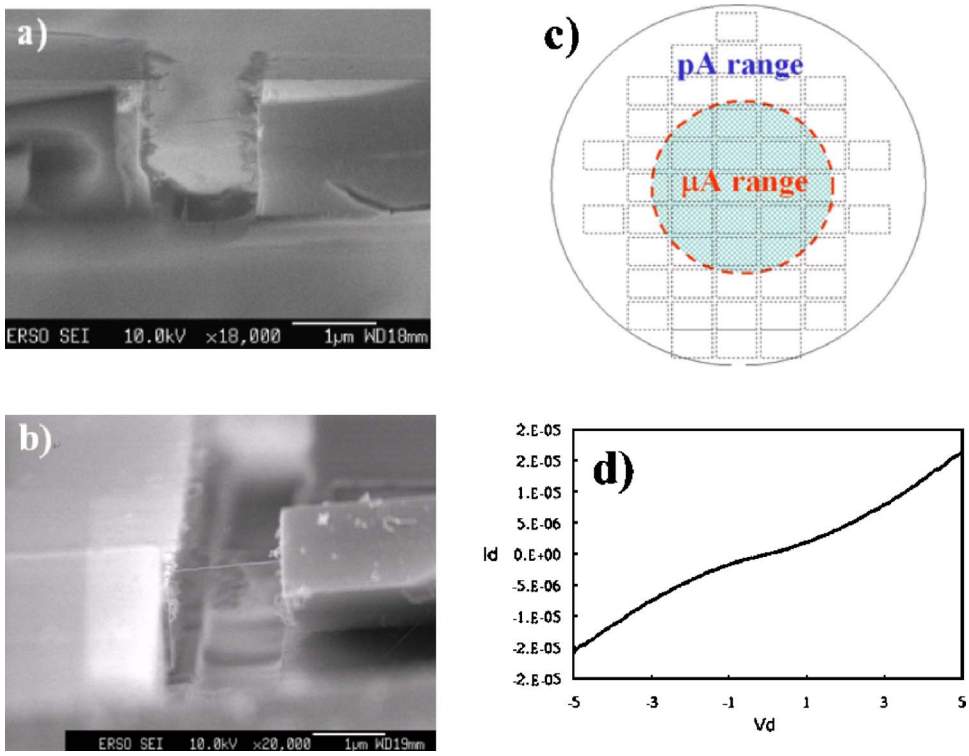

FIG. 5. SEM pictures of lateral-grown CNTs (a) formed by dry etching; (b) formed by wet etching. The bundled CNTs bridge the CMT layer from the catalyst. (c) and (d) The leakage current range without any post treatment by using dry etcher to form the catalyst islands. Note the leakage current is in the μA range because of the residues of Co particle/CMT layer, which can leave a conductive layer on the wafer surface and short the CNT-FETs.

practical. In this work, we found that by adding a hexamethyldisilazane (HMDS) layer on the nitride film before spinning the CMT, good CMT catalyst islands can be formed on the nitride layer for biosensor purposes [Fig. 4(c)].

D. Effects on the CMT patterns by using a dry or wet etching process

Figure 5 illustrates the effects on the CMT patterns when growing CNTs using either dry or wet etching process. Figure 5(a) shows the cross-sectional SEM picture of the pattern by dry etching. It can be seen that a suspending CNT is formed between the CMT patterns. In addition, sidewall polymers, which are frequently produced in the dry etching process, can be found all over the trench. These sidewall polymers will inhibit the formation of the CNTs. In contrast, no obvious polymer is found in the wet etching process by BOE (5:1) (buffered oxide etch solution, six parts 40% NH_4F and one part 49% HF), as shown in Fig. 5(b). Nevertheless, it is known that the control of the pattern profile and gap is quite poor in the wet etching process because of the isotropic etching nature. Since the CMT layer is vulnerable to severe overetching because of its porosity, we eventually adopt the standard reactive ion etching (RIE) dry etching process for the formation of the catalyst islands.

In this work, postetch cleaning was employed to remove the sidewall polymer (i.e., residue) and some cobalt/CMT debris spreads everywhere. In order to quantify the amount of the residue, we applied a voltage to two random positions on the blanket portion of the wafer and measured the current. In general, the current was expected to be very small (i.e., less than a picoampere) on the blank region theoretically. Figure 5(c) shows the distribution of leakage current level on the blanket portion of the wafer without receiving any post treatment after using dry etcher to form the catalyst islands. Figure 5(d) indicates that the leakage current is in tens of microamperes (μA) range around the wafer center. Moreover, the dice with the leakage current in the μA range account for about 33.3% of the total dice (17 out of a total of 51 dice). We believe the high leakage current is caused by the conducting residues or the incomplete etching of the conducting CMT layer at the center of the wafer because the CMT is much denser there, so the wafer surface becomes conductive and the leakage current reaches the μA range (compared with the insulator whose current level should fall in the picoampere range). These high leakage on the wafer surface could result in the malfunction of the transistors. In order to minimize the leakage current, post treatment (i.e., descum process) after our dry etching process is necessary to remove these residues. To effectively remove the residue, the thickness of bottom gate dielectric layer was increased and the overetching time of our dry etching was prolonged.

E. Other factors that affect the length of CNTs

For CNT-FET applications, vertical distribution and lateral growth of CNTs by the proposed CMT method are critical and must therefore be studied thoroughly. It should be noted, however, that the length of the CNT is also important

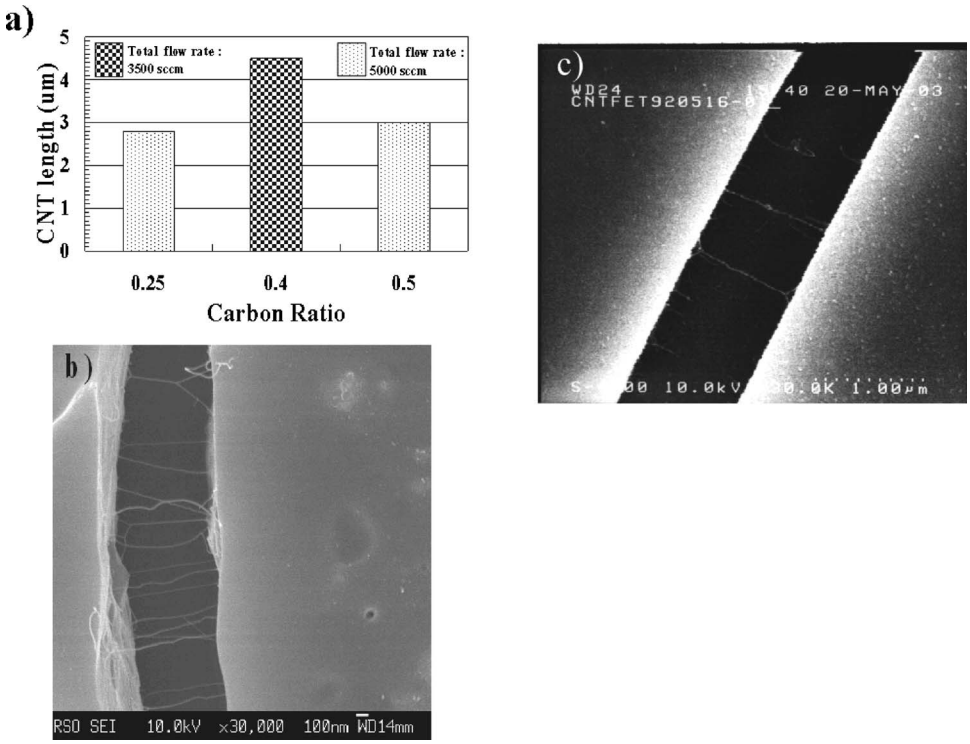

FIG. 6. (a) Lateral length of CNT vs gas composition, (b) SEM picture of CNTs when Co^{2+} concentration is 1.5 M, and (c) SEM picture of CNTs when Co^{2+} concentration is 0.5 M.

for some device applications. These include biosensors and dual/multiple-gated devices where longer CNT bundles are necessary.

In our reiterative experiments, the major parameter that affects the CNT length and the CNT tip-growth rate is found to be the concentration of carbon atoms. This parameter can be controlled by adjusting the reactive gas ratio (ethanol to Ar).[21] Figure 6(a) shows the results of the CNT length versus the composition of the reaction gas. For a given Ar flow rate of 5000 sccm, the length of CNT increases as the ethanol to Ar ratio increases from 0.25 to 0.5. This is ascribed to more carbon atoms being carried to the surface of the cobalt catalyst. A higher carbon concentration within the cobalt-carbon mixed catalyst will probably increase both the growth rate and the length of the CNTs. However, when the ethanol/Ar ratio approaches one, it is found that the CNT length does not increase any further, perhaps due to the accumulation of excess carbon atoms on the catalyst nanoparticles that eventually poison the catalysts. When the total gas flow rate reduces from 5000 to 3500 sccm, the length of CNT increases to greater than 4.5 μm. Since our APCVD chamber pressure remains unchanged, when the gas flow rate is decreased, the exhaust speed is also reduced simultaneously. Consequently, the carbon atoms can stay much longer around the Co catalyst. Therefore, the solubility of carbon atoms into the Co increases, resulting in the increase of the growth rate and the length of the CNTs. Under this process condition, a CNT is found to bridge the six μm gap, as shown in Fig. 8(b).

Besides controlling ethanol/Ar ratio of the reactive gas, the density of CNTs can be tuned by the concentration of Co^{2+} ion in the CMT solution. Figures 6(b) and 6(c) show SEM images of the CNTs grown by different Co^{2+} concentrations of 1.5 and 0.5 M, respectively. When the Co^{2+} concentration is 1.5 M, the CMT solution is more viscous, and the final thickness of catalyst islands is about 150 nm. The resultant density of the CNTs is higher as shown in Fig. 6(b), in which CNTs grow on the catalyst islands' sidewalls. However, when the Co^{2+} concentration is reduced to 0.5 M, the viscosity of the CMT solution is reduced and the thickness of the catalyst layer reduces to 20 nm. Obviously the density of the CNTs grown by the 0.5 M CMT solution is lower, and all the CNTs are located just in one layer, as shown in Fig. 6(c).

In our experiments, for longer hydrogen (H_2) reduction time, the growth mechanism favors the base-growth-type CNT. While for shorter hydrogen reduction time, the growth mechanism favors the tip-growth mechanism (Fig. 7), resulting in longer CNTs. So it appears that H_2 reduction time also plays a role on activating the Co particle as catalyst in our CMT method. This result is not consistent with other group who used Co and carbon monoxide to synthesize CNTs.[18]

The effects of the process gas flow direction in the APCVD quartz tube were also investigated in this study, no obvious difference was found when the gas flow is in either *X* or *Y* direction [Fig. 4(a)].

F. Performance of CNT-FET devices

Out of a total 1173 devices produced on one test wafer, 493 metallic bundled-CNTs (42.03%), 204 semiconducting-type CNT-FETs (17.39%) with an on/off ratio of less than or

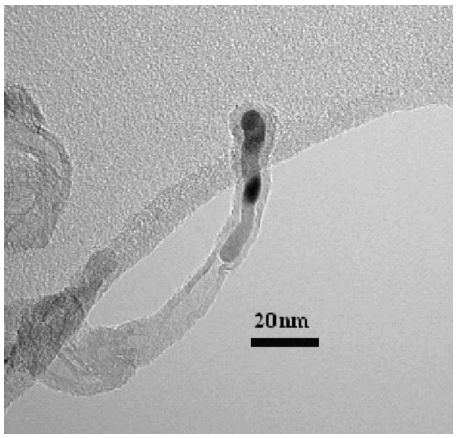

FIG. 7. SEM picture of tip growth.

equal to two orders, and 17 semiconducting-type CNT-FETs (1.45%) with an on/off ratio ranging from two to six orders, were obtained in this study. It is worth noting that in a batch of as-grown CNTs, both metallic and semiconducting type CNTs were present.[22] When at least one metallic CNT is included in the bundle, the bundled CNTs would show a gradual transition to metallic character. It is plausible that if the number of metallic CNTs is small, the bundled CNTs will still exhibit weak semiconducting characteristics. On the contrary, if the number of metallic CNTs is large, the bundled CNTs will show metallic characteristics. In general, when the on/off ratio of our CNT-FETs is about 10–100, less than 5–10 metallic CNTs are included in the channel (i.e., the space between two catalyst islands). Only when all CNTs in the bundle are semiconducting can a high performance in the CNT-FETs be expected.

Since our bundled CNTs were exposed to the air [Fig. 2(c)], all the as-grown CNT-FETs manufactured in this study were *p*-type semiconducting in nature.[34,35] Figure 8(c) shows the electrical properties (i.e., I_d-V_d and I_d-V_g) of an as-grown *p*-type CNT-FET with five orders of on/off ratio. The bottom gate voltage applied in Fig. 8(c) varies from 0 to −10 V (at a step of −2 V) at V_{ds}=−1 V. It should also be noted that the CNT-FETs with one to two orders of on/off ratio are rendered acceptable to serve the role of sensors. However, if we want to manufacture complementary CNT-FET structure (similar to conventional silicon-based CMOS devices) for broader applications, *n*-type CNT-FETs are indispensable. Previously, our group has successfully manufactured air-stable *n*-type CNT-FETs[31–33] without resorting to any additional and complex annealing process. After measuring the electrical properties of some wafers that depict generic *p*-type CNT-FETs in this work, a 300–400 nm silicon nitride (Si_3N_4) film was deposited on the wafer as passivation layer by plasma enhanced CVD (PECVD) at 390 °C. Afterwards, the contact holes of the source/drain and bottom gate regions were etched in the same MERIE dry etcher. Our experimental data confirmed that the generic *p*-type CNT-FETs are converted to air-stable *n*-type CNT-FETs, as shown in Fig. 8(d).

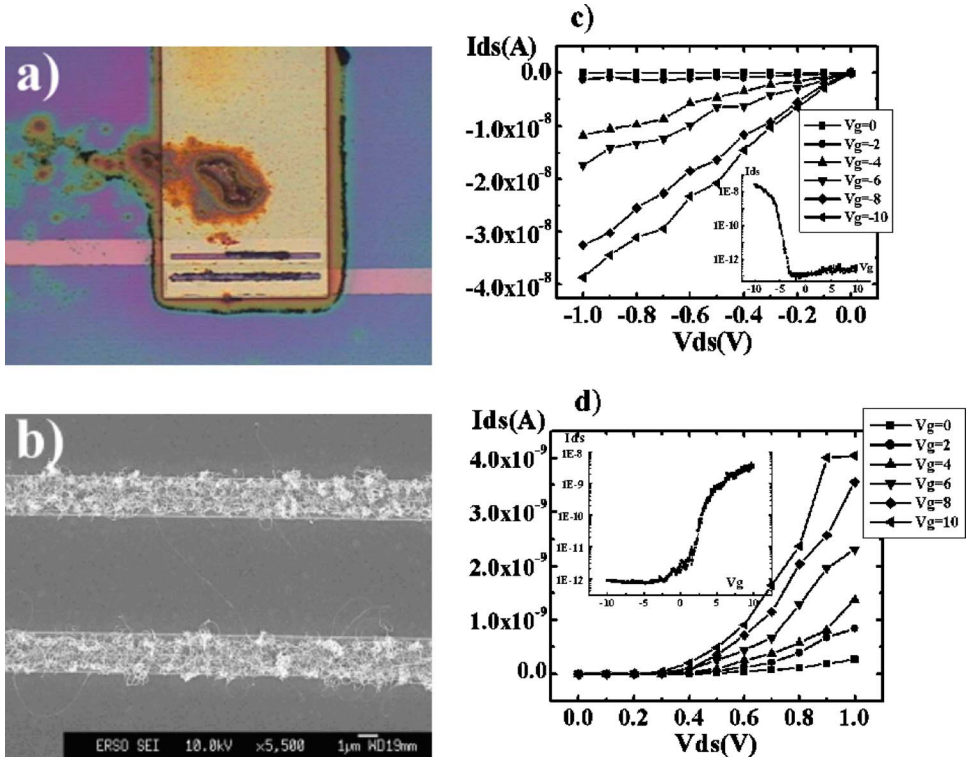

FIG. 8. Picture of an as-grown semiconducting-type CNT-FET and its I_{ds}-V_{ds} curve. Insets show the corresponding transfer curves (I_{ds}-V_g). (a) The optical microscope image of the type-I device in Fig. 2(c). Note the black clusters are CNTs (without a TEOS layer covering CMT catalyst islands). (b) SEM morphology of 6-μm long CNT grown between two catalyst islands. (c) An as-grown *p*-type CNT-FET with five orders of on/off ratio. (d) Converted *n*-type CNT-FET after depositing a 300 nm Si_3N_4 film on the the *p*-type CNT-FET shown in (c).

The converted *n*-type CNT-FETs depict one to four orders of on/off ratio when the bottom gate is biased from 0 to 10 V (at a step of 2 V) at $V_{ds}=1$ V. This is ascribed to the use of PE-nitride film as the passivation layer whose deposition temperature was high enough to simultaneously remove the oxygen atoms from the CNTs or CNT/metal interface in the PECVD deposition chamber. The approach offers a feasible method to fabricate air-stable *n*-type CNT-FETs by converting the generic *p*-type CNT-FETs.

It is worth noting that theoretically both *n*- and *p*-type CNT-FETs can be fabricated on the same chip by selectively converting some of the generic *p*-type CNT-FETs on the chip, while leaving other *p*-type CNT-FETs on the same chip untouched. The design of a photomask set is currently under way which will allow us to test the feasibility of the idea.

Although the device performance of our proposed process has yet to be optimized, our initial results are encouraging and suggest a viable method of fabricating functional CNT-FETs. Using the CNT growth method proposed in this article, we believe it is possible, with further process refinement, to manufacture semiconducting-type CNT-FETs suitable for many applications, especially sensors. As mentioned earlier, the CNTs synthesized in this study contain a high percentage of metallic-type CNTs, representing about 42.03% of metallic bundled CNTs out of the total as-grown devices. We do believe, however, that after optimizing the growth conditions and applying plasma treatment on the as-grown CNT-FETs, a much higher percentage and a higher on/off ratio of semiconducting-type CNT-FETs are achievable.[36]

IV. CONCLUSIONS

To the best of our knowledge, only SWNTs can show the semiconducting-type behaviors. And judging from our electrical measurement results and the TEM pictures [Fig. 3(b)], we deduce that the CNTs we synthesized are mostly bundled SWNTs. This result is also consistent with earlier study.[37]

In order to synthesize long CNTs, it is critical to balance the rate of ethanol decomposition and the rate of carbon atom diffusion. In other words, the carbon supply route needs to remain open during processing. The rate of carbon diffusion will be dominated mostly by the temperature, and the ethanol decomposition rate will be affected by both the synthesis temperature and the flow rate of the carrier gas (Ar). The work for improving the CNT-FET performance are still on-going and the result will be reported later.

In short, we have developed an IC compatible process for fabricating CNT-FETs successfully with a shorter hydrogen reduction time in this study. Longer CNT length can be obtained by optimizing carbon ratio during synthesis, and the accumulation of carbon on the catalyst tip can be controlled by mixing inert gas with the carbon source. This IC compatible process seems to be promising for fabricating a prealigned single-walled carbon nanotube matrix for both *n*- and *p*-type CNT-FETs.

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