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We investigate the electronic transport characteristics of a one-dimensional (1D) narrow constriction defined in a GaAs/$Al_xGa_{1-x}As$ heterostructure by a simple triple-gate structure consisting of a pair of split gates and an additional surface Schottky gate (center gate) between them. Comparison between devices with and without a center gate reveals that the center gate, even when zero biased (V_{CG}=0 V), significantly modifies the surface potential and facilitates the 1D confinement in a deep two-dimensional electron system. The pinch-off voltages at V_{CG}=0 V for various channel widths W (=0.4–0.8 μm) and lengths L (=0.2–2 μm) are well described by the analytical formula based on the pinned-surface model [J. H. Davies *et al.*, J. Appl. Phys. **77**, 4504 (1995)]. Nonlinear transport spectroscopy with an additional dc bias shows that the lowest 1D subband energy separation ($\Delta E_{1,2}$) changes linearly with V_{CG} and can be enhanced by 70% for V_{CG}=0.8 V. A simple model assuming an infinitely long channel and no self-consistent potential well reproduces the overall behavior of the measured $\Delta E_{1,2}$. In addition, effects of impurities, occasionally found for long-channel devices ($L \geqslant 1$ μm), are found to be greatly reduced by applying positive V_{CG} and thereby enhancing $\Delta E_{1,2}$. Data are also presented for the transport anomaly below the first conductance plateau, the so-called "0.7 anomaly," demonstrating that the triple-gate structure is useful for the study of density-dependent phenomena in a 1D system. © *2006 American Institute of Physics*.
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I. INTRODUCTION

Electron transport through one-dimensional (1D) narrow constrictions such as quantum point contacts[1,2] (QPCs) or quantum wires[3] has been a focus of research in mesoscopic systems. When the mean free path of electrons is larger than the channel length and the width of the constriction is comparable to the de Broglie wavelength of electrons, the conductance (G) through the constriction is quantized in units of $2e^2/h$ ($\equiv G_0$),[1,2] where e is the electronic charge and h is Planck's constant with the factor of 2 arising from the spin degeneracy. Advances in nanoprocessing and material growth have led to successful fabrication of such structures with high integrity, thus providing opportunities to investigate physics emerging in a clean 1D system.[3,4] In addition, QPCs are building blocks for other mesoscopic devices such as quantum dots or artificial atoms and can be integrated into more sophisticated devices as a sensitive charge detector[5] or a readout device of a qubit.[6] Therefore, the capability to precisely tune the characteristics of QPCs or quantum wires is becoming increasingly important for both fundamental physics and applications for quantum-information devices.

Typically, narrow constrictions are defined in a two-dimensional electron gas (2DEG) confined at a modulation-doped GaAs/$Al_xGa_{1-x}As$ heterostructure by using a pair of split surface Schottky gates to deplete the 2DEG underneath and then squeeze the channel in between.[1,2] The important structural parameters are the width and length of the split-gate opening, the density of the 2DEG, and its distance from the surface; these predetermine the ultimate characteristics of the device, such as the 1D subband energy separation (ΔE) and the number of conductance plateaus resolved.[7] Thus far, various approaches have been taken to add *in situ* control over these characteristics, by incorporating an additional gate, either a back gate[8,9] that varies the density of the whole 2DEG or a top gate separated by the split gates by etched trenches[10] or an insulator.[11,12] While these studies have dem-

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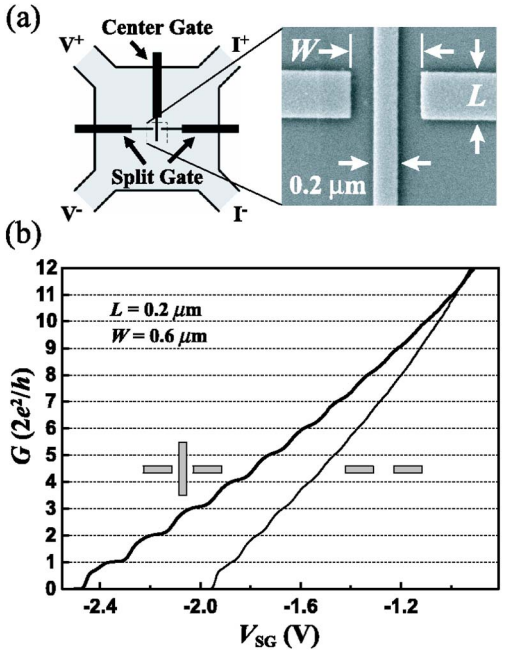

FIG. 1. (a) Schematic illustration of device structure (left) and SEM image of the fine gate pattern (right). $V^{\pm}$ ($I^{\pm}$) indicates voltage (current) probes. (b) Conductance G measured at 1.5 K as a function of split-gate voltage V_{SG} of devices with (thick line) and without (thin line) center gate. The two devices have the same split-gate geometry, $L=0.2$ μm and $W=0.6$ μm.

onstrated the *in situ* control of the transport characteristics, they require additional fabrication processes[10–12] or special care in order to avoid shorting the Ohmic contacts to the additional gate.[8–10]

In this paper, we examine a simple triple-gate structure that incorporates an additional surface Schottky gate (center gate) in between the pair of split gates. Comparison between samples with and without a center gate reveals that the center gate, even when zero biased, significantly affects the surface potential and thereby facilitates the 1D confinement in a deep 2DEG. Nonlinear transport spectroscopy with an additional dc bias[13] shows that ΔE changes linearly with the center-gate voltage (V_{CG}) and can be enhanced by 70% for $V_{CG}=0.8$ V. A simple model is used to calculate the lowest subband energy separation ($\Delta E_{1,2}$), which well reproduces the overall behavior of the measured $\Delta E_{1,2}$. In addition, effects of impurities,[14] occasionally found for long-channel devices, are shown to be greatly suppressed by applying a positive V_{CG} and thereby enhancing $\Delta E_{1,2}$. We also present data for the transport anomaly below the first conductance plateau, the so-called "0.7 anomaly,"[3] to demonstrate that the triple-gate structure is useful for the study of density-dependent phenomena in a 1D system.

II. EXPERIMENTAL DETAILS

Figure 1(a) shows a schematic illustration of the device structure and a scanning electron microscopy image of the fine gate patterns. The device was fabricated from a GaAs/$Al_xGa_{1-x}As$ ($x=0.3$) heterostructure grown by molecular beam epitaxy on a Si-doped n^+-GaAs (100) substrate, which functions as a back gate. The heterostructure comprises a 30-nm-wide GaAs quantum well modulation doped with Si at a 90 nm setback in the upper $Al_xGa_{1-x}As$ barrier. The quantum well is separated from a heavily Si-doped (10^{18} cm^{-3}) GaAs buffer layer by 20 nm of $Al_xGa_{1-x}As$ and 1.2 μm of AlAs/GaAs short-period (2 nm/2 nm) superlattice that prevents leakage to the back gate.[15] The distance d between the surface and the center of the quantum well (and hence the 2DEG) is 260 nm, considerably larger than the typical value (~100 nm) for defining mesoscopic structures. As grown, the structure has a sheet electron density (n_{2D}) of 1.5×10^{11} cm^{-2} and a mobility of 3×10^6 cm^2/V s at 1.5 K, which correspond to a mean free path of 20 μm.

The wafer was processed into a square-shaped mesa (120×120 μm^2) with four arms on the corners, to which Ohmic contacts were formed by alloying AuGeNi (80:10:10 wt) at 390 °C for 1 min in H_2.[15] The fine gate patterns were defined by electron-beam lithography and lift-off of evaporated 20-nm-thick Ti/Au. The length (L) and width (W) of the split gates were varied as $L=0.2-2$ μm and $W=0.4-0.8$ μm, respectively, while the width of the center gate was fixed at 0.2 μm.[16,17] We also fabricated control samples without a center gate for comparison.

Transport measurements were performed with the sample cooled in pumped ^{4}He ($T=1.4-1.5$ K) or ^{3}He ($T=0.24-1.4$ K) cryostats in the dark without illumination. A standard lock-in technique was used with an ac modulation voltage of 20 μV at 13 or 77 Hz. To eliminate effects of contact resistance, a four-terminal setup was used to measure the voltage across the constriction as well as the current flowing through it [Fig. 1(a)]. For the determination of ΔE, a finite dc bias ($|V_{dc}|\leq3$ mV) was added to the ac modulation voltage.[13] Note that some fraction of the applied dc voltage drops at the Ohmic contacts, which then varies with the current and hence with the split-gate bias (V_{SG}). To extract the voltage across the constriction, we separately measured the dc voltage between the voltage probes, which we denote as V_{SD}. The range of the applied center-gate bias was $-0.45\leq V_{CG}\leq0.9$ V, for which the leakage current was negligibly small. Unless otherwise specified, the back-gate bias (V_{BG}) was kept at zero.

III. RESULTS AND DISCUSSION

A. Effects of center gate on the surface potential

We start by comparing samples with and without a center gate. Figure 1(b) shows the measured G at 1.5 K of the devices with (thick line) and without (thin line) a center gate as a function of V_{SG}. The split gates of the two devices have the same dimensions, $W=0.6$ μm and $L=0.2$ μm. For the sample with the center gate, V_{CG} was set to zero. The data reveal that, even when $V_{CG}=0$ V, the center gate significantly affects the characteristics of the device. The pinch-off voltage (V_P) is found to be much deeper (i.e., more negative) in the sample with the center gate. Furthermore, with the center gate the conductance plateaus are seen to be better defined. We have confirmed similar behavior in other devices with different W and L. Note that the rather poor conductance quantization in the samples without a center gate is partly due to the large depth of the 2DEG in our heterostructure.[18] The much improved quantization in the

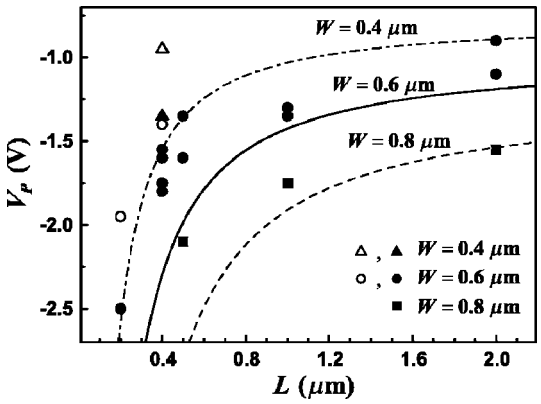

FIG. 2. Pinch-off voltage V_P of devices with different channel widths W, plotted as a function of channel length L. The solid (open) symbols indicate devices with (without) center gate. For those with center gate, the center-gate bias is kept at $V_{CG}=0$ V. Three curves represent the pinch-off voltages calculated as a function of L for different W using Eq. (5.2) of Ref. 19.

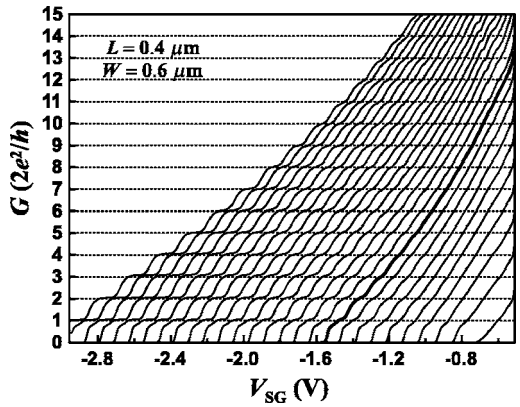

FIG. 3. G of a device with $L=0.4$ μm and $W=0.6$ μm measured at 1.5 K as a function of V_{SG}. From left to right, the center-gate voltage V_{CG} is varied from 0.9 to −0.45 V in 0.05 V step. The thick line corresponds to $V_{CG}=0$ V.

samples with a center gate, in turn, suggests that the center gate helps defining constrictions in a deep 2DEG.

We investigated the pinch-off characteristics of many devices with various W and L. The results are summarized in Fig. 2, where V_P of each device is plotted as a function of L. The solid (open) symbols represent devices with (without) a center gate. For the samples with a center gate, V_{CG} is kept at zero. It is seen that, for a given W, V_P becomes shallower (i.e., less negative) with increasing L and then tends to saturate for larger L. In addition, the plot reveals that the devices without a center gate have consistently shallower V_P compared to those with one. This clearly shows that, even when $V_{CG}=0$ V, the center gate significantly affects the electric potential at the constriction.

In the figure, we plot the pinch-off voltages calculated from the analytical formula for the standard rectangular split-gate geometry [Eq. (5.2) of Ref. 19]. The model assumes a pinned surface for the exposed semiconductor surface. Although the pinned-surface model may not be appropriate for GaAs at cryogenic temperatures,[20] it greatly simplifies the mathematical treatment, allowing for the analytical expression of V_P. The parameters used in the calculation are $d=0.26$ μm and $V_t=-0.45$ V, the latter being the split-gate gate voltage at which the 2DEG underneath the gate is depleted. As the figure shows, the calculation reproduces the behavior of the devices with a center gate very well. On the other hand, the agreement is poorer for those without a center gate, which exhibit V_P much shallower than the calculation. This is consistent with the analysis in Ref. 19, where it was shown that the frozen-surface model results in a shallower pinch-off voltage than the pinned-surface model. In our triple-gate structure, the potential at the surface just above the 1D channel is kept at zero by the center gate, making the pinned-surface model more appropriate. On the other hand, for the standard split-gate geometry, the frozen-surface model is more appropriate. Hence, the difference between the devices with and without a center gate can be interpreted as due to the difference between the pinned surface and the frozen surface.[21]

As shown in Ref. 19, the pinned surface results in a stronger 1D confinement than the frozen surface. This is consistent with our results that the conductance plateaus are better developed in devices with a center gate. The more negative V_{SG} required to squeeze the 1D channel in those devices results in a correspondingly stronger confinement, thereby facilitating the conductance quantization even in a deep 2DEG as used here. In the following, we focus on samples with a center gate and describe how the transport characteristics can be modified by V_{CG}.

B. Control of 1D confinement with center gate

Figure 3 presents results for a device with $W=0.6$ μm and $L=0.4$ μm, where the measured G at 1.5 K is plotted as a function of V_{SG} for different V_{CG} ranging from −0.45 to 0.9 V. The thick line corresponds to $V_{CG}=0$ V. For this sample, having a larger L of 0.4 μm, the pinch-off voltage at $V_{CG}=0$ V is shallower, and correspondingly, only a small number of conductance plateaus are visible for $V_{CG}=0$ V. However, as V_{CG} is made progressively positive, V_P shifts linearly with V_{CG} to more negative values, and accordingly, an increasing number of plateaus become resolved. For the highest V_{CG} of 0.9 V, as many as 14 conductance steps are clearly observed. On the other hand, when V_{CG} is made negative, the features become obscured until no structure except the 0.7 anomaly[4] is discernible at $V_{CG}=-0.4$ V.

In order to clarify the effects of the center gate on the confinement, we determined the 1D subband energy separation by adding a finite dc voltage ($|V_{dc}| \leqslant 3$ mV) to the small ac modulation voltage.[13] Figure 4(a) displays the gray-scale plots of the transconductance (dG/dV_{SG}) at 0.24 K for different values of V_{CG}. The data are plotted against V_{SG} (horizontal axis) and V_{SD} (vertical axis), the latter being the dc voltage across the constriction measured separately. The transconductance was calculated by numerically differentiating the measured G with respect to V_{SG}. The bright features represent peaks in dG/dV_{SG}, which occur when the bottom of a 1D subband matches the electrochemical potential of either the source or drain reservoir.[22] The energy separations between adjacent subbands (ΔE) can be determined by the

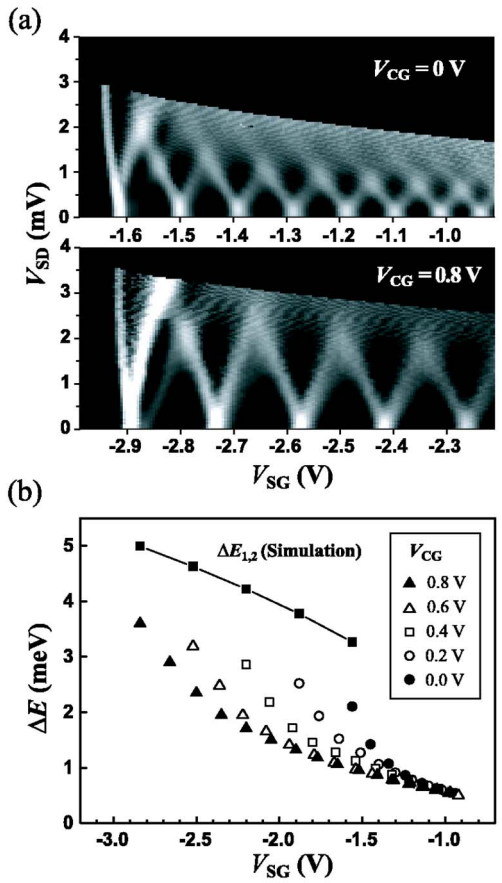

FIG. 4. (a) Gray-scale plots of transconductance dG/dV_{SG} measured at $T=0.24$ K as a function of V_{SG} and source-drain bias (V_{SD}) for $V_{CG}=0$ (upper panel) and 0.8 V (lower panel). The bright features indicate peaks in dG/dV_{SG}. The sample is the same as in Fig. 3 ($L=0.4$ μm and $W=0.6$ μm). (b) Energy separation ΔE of adjacent subbands deduced from the transconductance data, plotted as a function of V_{SG} for various V_{CG} varied from 0 to 0.8 V in 0.2 V step. The leftmost data point for each V_{CG} corresponds to the lowest subband energy separation $\Delta E_{1,2}$. The solid squares represent $\Delta E_{1,2}$ calculated for each set of V_{SG} and V_{CG}. The sample is the same as in Fig. 3 ($L=0.4$ μm and $W=0.6$ μm).

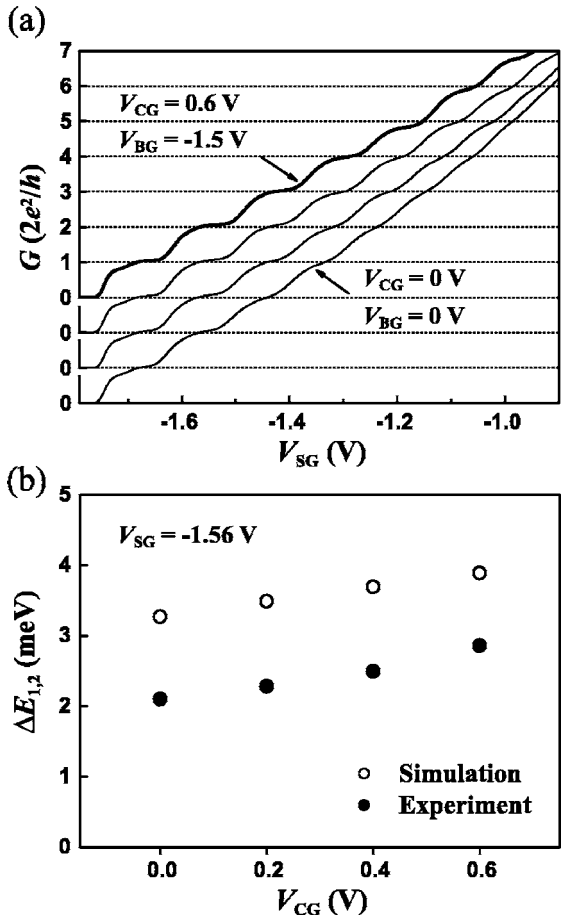

FIG. 5. (a) G vs V_{SG} for different combinations of V_{CG} and V_{BG} at 1.5 K. From bottom to top, V_{CG} is increased from 0 to 0.6 V in 0.2 V step while V_{BG} is decreased from 0 to -1.5 V in 0.5 V step to keep the same pinch-off voltage. The sample is the same as in Figs. 3 and 4 ($L=0.4$ μm and $W=0.6$ μm). (b) $\Delta E_{1,2}$ for each set of V_{CG} and V_{BG}, plotted as a function of V_{CG}. The open and closed symbols represent results of simulation and experiment, respectively.

value of V_{SD} at which two lines forming an apex meet at the top. The data clearly show that ΔE for the same subbands increases with V_{CG}.

Figure 4(b) plots the measured $\Delta E_{i,i+1}$ as a function of V_{SG} for different V_{CG}. Here, $\Delta E_{i,i+1}$ denotes the energy separation between the ith and $(i+1)$th subbands. The data show that $\Delta E_{1,2}$ has a linear relationship with V_{SG}. It is also seen that the position of each conductance step (in V_{SG}) moves in proportion to V_{CG}, which points to a linear relationship between $\Delta E_{1,2}$ and V_{CG}, similar to previous reports using different gate structures.[12] The values of $\Delta E_{1,2}$ for $V_{CG}=0$ and 0.8 V are 2.1 and 3.6 meV, respectively, corresponding to an enhancement of 70%. If we extrapolate the linear relationship between $\Delta E_{1,2}$ and V_{CG}, the values of $\Delta E_{1,2}$ for the data in Fig. 3 are estimated to be 1.4 and 3.8 meV for $V_{CG}=-0.4$ and 0.9 V, respectively, corresponding to a change by a factor of 2.7.

We simulated $\Delta E_{1,2}$ using a simple model assuming an infinitely long 1D channel and no self-consistent potential from the electrons in the 1D channel.[23] As shown below, the approximation of no self-consistent potential is reasonable for the present case of calculating $\Delta E_{1,2}$, where only one subband is occupied and so the electron density is low. The electric potential in the two-dimensional (2D) plane perpendicular to the 1D channel was obtained by solving the Poisson equation using a finite element method. Then, using the extracted 1D potential transverse to the channel, the Schrödinger equation was solved to obtain the 1D subband energies. The calculated $\Delta E_{1,2}$ is plotted in Fig. 4(b) for comparison with experiment. The simulation shows $\Delta E_{1,2}$ consistently larger than the experiment, which is a result of the infinitely long channel assumed. However, it well reproduces the linear dependence of $\Delta E_{1,2}$ on V_{SG} and hence on V_{CG}.

The enhanced $\Delta E_{1,2}$ for positive V_{CG} is partly due to the more negative V_{SG} required to squeeze the channel. We therefore examined $\Delta E_{1,2}$ for different V_{CG} while keeping V_{SG} constant by using a back gate. Figure 5(a) depicts the measured G of the same device as in Fig. 3, where the combinations of V_{CG} and V_{BG} are chosen to keep V_P constant, varying in equal steps from $V_{CG}=V_{BG}=0$ V to $V_{CG}=0.6$ V and $V_{BG}=-1.5$ V. The data demonstrate that, even though V_P is kept constant, the conductance plateaus become better resolved with increasing V_{CG}. The 2DEG density estimated from a separate Hall measurement is $n_{2D}=1.5\times10^{11}$ cm^{-2}

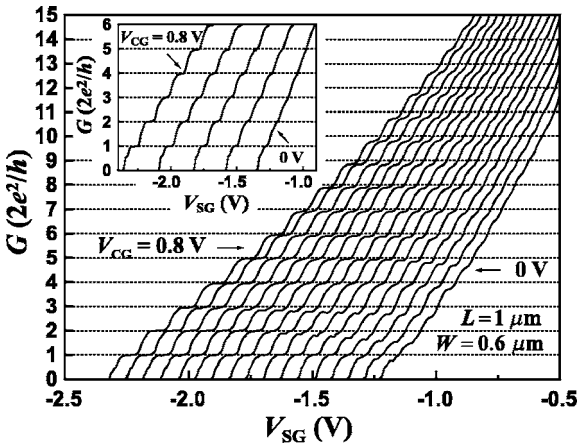

FIG. 6. G vs V_{SG} of a device with $L=1$ μm and $W=0.6$ μm ($T=1.4$ K). From left to right, V_{CG} is increased from 0 to 0.8 V in 0.05 V step. Inset: G vs V_{SG} of the same device for a different cool-down.

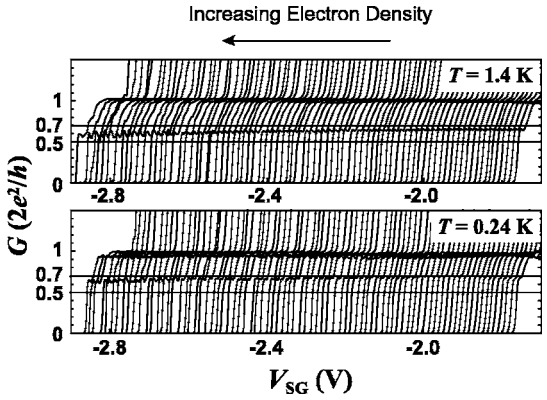

FIG. 7. G vs V_{SG} of the same device as in Fig. 6 ($L=1$ μm and $W=0.6$ μm), measured at 1.4 K (upper panel) and 0.24 K (lower panel). From right to left, V_{CG} is increased from 0 to 0.8 V in steps of 0.01 V. Here, positive back-gate bias of $V_{BG}=1$ V is applied to enhance ballistic transport. The two horizontal lines indicate the positions of $(0.7)2e^2/h$ and $(0.5)2e^2/h$.

for $V_{BG}=0$ V, which decreases to $n_{2D}=0.7\times10^{11}$ cm^{-2} for $V_{BG}=-1.5$ V. The values of $\Delta E_{1,2}$ measured for these conditions are 2.1 and 2.9 meV. Even though the n_{2D} in the reservoir is significantly decreased by negative V_{BG}, the confinement in the constriction is improved by positive V_{CG}, resulting in $\Delta E_{1,2}$ enhanced by 40%. Figure 5(b) compares the measured and calculated $\Delta E_{1,2}$ as a function of V_{CG}. The calculation well reproduces the linear dependence of $\Delta E_{1,2}$ on V_{CG}.

C. Effects of 1D confinement and electron density on transport anomalies

1. Impurity effects

We next used the center gate to study effects of the 1D confinement and electron density on various transport anomalies. Figure 6 shows the measured G at 1.4 K of a long-channel device with $W=0.6$ μm and $L=1$ μm for different V_{CG} ranging from 0 to 0.8 V. Compared to the $L=0.4$ μm device shown in Fig. 3, the longer L of this device results in shallower V_P. For $V_{CG}=0$ V, the conductance plateaus are not well developed, and their positions are somewhat below the integral multiples of $2e^2/h$. Also note that the plateau positions are not equally spaced, indicating that each subband has a different contribution to the measured G. We have investigated many devices and found such behavior only in those with $L\geqslant1$ μm. By applying asymmetric biases to the split gates,[14] we have confirmed that this is due to an impurity near the 1D channel that happens to be charged in this particular case. Indeed, details of the conductance traces for these samples vary from cool-down to cool-down, and occasionally, the plateaus can be well aligned at integer multiples of $2e^2/h$, with no trace of impurity effects (inset of Fig. 6).

When positive V_{CG} is applied, the positions of the plateaus start to line up at integral multiples of $2e^2/h$. The measured $\Delta E_{1,2}$ for $V_{CG}=0,0.4$, and 0.8 V are 2.3, 3.0, and 4.1 meV, respectively.[24] The enhanced subband separation is also accompanied by an increase in the 1D electron density. The observed suppression of the impurity effects may therefore be ascribed to the enhanced confinement and the increased screening due to the increased 1D electron density, both of which would reduce impurity scattering and thereby facilitate the ballistic transport.

2. The 0.7 anomaly

It is widely known that the conductance of a 1D ballistic channel exhibits an additional plateaulike feature, the so-called 0.7 anomaly, around $G=0.7$ $(2e^2/h)$ below the first plateau.[4] While experiments have suggested that the 0.7 anomaly is associated with the spin degree of freedom,[4] its exact origin remains an issue of active research.[9,25–30] In our samples, the 0.7 anomaly is observed ubiquitously, as clearly seen in Figs. 1(b), 3, and 5(a). Since the 0.7 anomaly is known to exhibit complicated dependence on temperature,[4,25,26,29] electron density,[9,28,30] and channel length,[28,30] we here used the center gate to investigate the density dependence of the anomaly.

Figure 7 displays the measured G around the first plateau of the $L=1$ μm device with V_{CG} varied from 0 to 0.8 V. We here applied a positive back-gate bias of $V_{BG}=1$ V to further increase $\Delta E_{1,2}$ and enhance the ballistic transport. At $T=1.4$ K, the position of the additional feature evolved from $0.65G_0$ to $0.55G_0$ with increasing V_{CG} and hence increasing electron density. When the temperature was reduced to 0.24 K, the anomalous structure became slightly weaker and its positions were higher, evolving from $0.7G_0$ to $0.6G_0$. As also seen in Fig. 3, such density dependence was not observed for devices with $L\leqslant0.5$ μm. The observed dependence of the anomalous feature on the electron density and the channel length is consistent with a previous report[28] on ultralow-disorder quantum wires in which electrons were field induced through a top gate. These results demonstrate that the triple-gate structure provides an alternative and simpler way of investigating density-dependent phenomena in a clean 1D system.

IV. SUMMARY AND CONCLUSIONS

We have fabricated 1D narrow constrictions defined by a triple-gate structure incorporating an additional surface Schottky gate (center gate) in between the pair of split gates

and studied their transport characteristics at low temperatures. Comparison between devices with and without a center gate revealed that the center gate, even when zero biased, affects the surface potential and significantly enhances the 1D confinement. Because of the fixed surface potential above the 1D channel, the pinch-off voltage of these devices can be well predicted by an analytical formula based on the pinned-surface model. Nonlinear transport spectroscopy showed that the energy separation between the lowest 1D subbands varies in proportion to the center-gate bias V_{CG} and can be enhanced by 70% for $V_{CG}=0.8$ V. The enhanced 1D confinement for positive V_{CG} greatly enhanced 1D ballistic transport, as manifested by the better-developed conductance plateaus and the suppression of impurity scattering in long-channel devices. For a 1-μm-long channel device, the anomalous plateaulike feature below the first conductance plateau (the "0.7 anomaly") was observed to evolve toward $0.5(2e^2/h)$ with increasing V_{CG} and hence increasing electron density.

These results clearly demonstrate that the triple-gate structure provides a simple way of controlling the characteristics of 1D constrictions and investigating density-dependent phenomena in a 1D system. In addition, its predictable pinch-off characteristics and enhanced 1D confinement are major advantages over the conventional split-gate structure, the latter being of particular importance when defining constrictions in deep 2DEGs. The structure, which does not require any additional fabrication steps or interfere with other parts of the device, will be particularly suited for lateral integration.

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