New Curvature-Compensation Technique for CMOS Bandgap Reference With Sub-1-V Operation

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***Abstract*—A new sub-1-V curvature-compensated CMOS bandgap reference, which utilizes the temperature-dependent currents generated from the parasitic n-p-n and p-n-p bipolar junction transistor devices in the CMOS process, is presented. The new proposed sub-1-V curvature-compensated CMOS bandgap reference has been successfully verified in a standard 0.25-μm CMOS process. The experimental results have confirmed that, with the minimum supply voltage of 0.9 V, the output reference voltage at 536 mV has a temperature coefficient of 19.5 ppm/°C from 0 °C to 100 °C. With a 0.9-V supply voltage, the measured power noise rejection ratio is −25.5 dB at 10 kHz.**

***Index Terms*—Bandgap voltage reference, curvature-compensation technique, temperature coefficient, voltage reference.**

I. Introduction

REFERENCE circuits are the basic building blocks in many applications from pure analog, mixed-mode, to memory circuits. The demand for low-voltage operation is especially apparent in the battery-operated mobile products, such as cellular phones, PDAs, camera recorders, and laptops [1].

In CMOS technology, parasitic vertical bipolar junction transistors (BJTs) have been used in high-precision bandgap voltage references. The conventional CMOS bandgap references did not work with a sub-1-V supply voltage. The reason why the minimum supply voltage can not be lower than 1 V is constrained by two factors. One is due to the bandgap voltage of silicon around 1.25 V [2], [3], which exceeds a 1-V supply. The other is that the low-voltage design of the proportional to absolute-temperature current generation loop is limited by the input common-mode voltage of the amplifier [2], [4]. These two limitations can be solved by using the resistive subdivision methods [5], [6], low-threshold voltage (or native) device [5]–[7], BiCMOS process [4], or DTMOST device [8]. However, the bandgap reference working with a low supply voltage often has a higher temperature coefficient than that of a traditional bandgap reference. This has resulted in the development of new temperature-compensated techniques, such as quadratic temperature compensation [9], exponential temperature compensation [10], piecewise-linear curvature correction [11], [12], and resistor temperature compensation [13], [14]. To implement those advanced mathematical functions with high accuracy, the development of the low-voltage bandgap structure requires precision matching of current mirrors or a preregulated supply voltage. Cascode current mirror [9], [11] and preregulated circuit [15] are good methods to solve this problem, but the minimum supply voltage is the tradeoff to use such methods.

In this brief, a new sub-1-V curvature-compensated CMOS bandgap reference is proposed to be successfully operated with sub-1-V supply in a standard 0.25-μm CMOS process. The new proposed sub-1-V curvature-compensated bandgap voltage reference with a stable output voltage $\mathrm{V_{REF}}$ of 536 mV and temperature coefficient of 19.5 ppm/°C under supply voltage of 0.9 V has been verified in the silicon chip [16].

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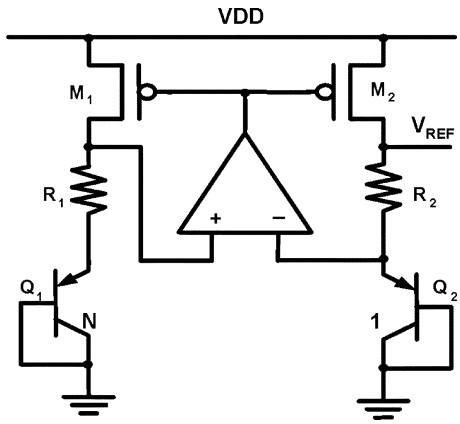

Fig. 1. Traditional bandgap voltage reference circuit in CMOS technology.

II. Traditional Bandgap Voltage Reference Circuit

The typical implementation of a traditional bandgap voltage reference in CMOS technology is shown in Fig. 1. In this circuit, the output reference voltage is the sum of a base–emitter voltage (V_{BE}) of the BJT and the voltage drop across the upper resistance (R_2). The BJTs (Q_1 and Q_2) are typically implemented by the diode-connected vertical p-n-p BJTs. The output reference voltage of the traditional bandgap voltage reference circuit can be written as

$$V_{\mathrm{REF-TRAD}} = |V_{\mathrm{BE2}}| + \frac{R_2}{R_1}\frac{kT}{q}\ln(N) \tag{1}$$

where k is Boltzmann's constant (1.38×10^{-23} J/K), q is electronic charge (1.6×10^{-19} C), and N is the emitter–area ratio of the BJTs. The second item in (1) is proportional to the absolute temperature (PTAT), which is used to compensate for the negative temperature coefficient of V_{BE}. Usually, the proportional to the absolute temperature voltage (V_{PTAT}) comes from the thermal voltage (kT/q) with a temperature coefficient about $+0.085$ mV/°C which is quite smaller than that of V_{EB}.

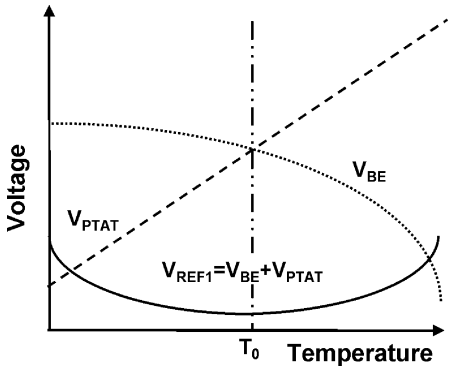

Fig. 2. Relationship between nonlinear temperature dependence $V_{\rm BE}$ and linear temperature dependence $V_{\rm PTAT}$ on the output reference voltage of bnadgap voltage reference circuit. The multiplying $V_{\rm PTAT}$ with $\rm K_{factor}$ is used to compensate the $\rm V_{BE}$.

After multiplying $V_{\rm PTAT}$ with an appropriate factor and summing with $V_{\rm BE}$, the bandgap voltage reference will have a low sensitivity to temperature variation. However, the relationship between $V_{\rm BE}$ of BJT and temperature is a nonlinear property that can be expressed by [17]

$$V_{\rm BE}=V_G(T_0)+\frac{T}{T_0}[V_{\rm BE}(T_0)-V_G(T_0)]-(\eta-m)\frac{kT}{q}\ln\left(\frac{T}{T_0}\right) \tag{2}$$

where V_G is the bandgap voltage of silicon extrapolated at 0 K, T is the absolute temperature in degrees kelvin (°K), η is a temperature constant depending on technology, m is the order of the temperature dependence of the collector current, and T_0 is the reference temperature. In (2), the term of $T\ln(T/T_0)$ is the nonlinear temperature-dependence factor to $V_{\rm BE}$. When (2) is expanded by Taylor series, it can be represented by [17]

$$V_{\rm BE}=a_0+a_1T+a_2T^2+\cdots+a_nT^n \tag{3}$$

where $a_0, a_1, \ldots,$ and a_n are the corresponding coefficients. The relationship between temperature dependence $V_{\rm BE}$ and linear temperature dependence $V_{\rm PTAT}$ on the output reference voltage of bnadgap reference is shown in Fig. 2. The first-order temperature compensation involves the cancellation of the T term by using the $V_{\rm PTAT}$, but the high-order temperature-dependence factor cannot be compensated with $V_{\rm PTAT}$ in the traditional bandgap voltage reference. Therefore, the traditional bandgap voltage reference working in low supply voltage has a higher temperature coefficient.

III. New Proposed Curvature–Compensated Method

A. Design Concept

The proposed bandgap voltage reference with new curvature-compensation technique is illustrated in Fig. 3. There are two types of bandgap voltage reference circuits in standard CMOS process. The first type uses the parasitic vertical p-n-p BJTs to realize the badgap voltage reference circuit, which has been widely used in many integrated circuits. The second type is realized with parasitic vertical n-p-n BJTs. The parasitic vertical n-p-n BJT in standard CMOS process is implemented with a deep n-well structure. Thus, there is no extra cost to have n-p-n parasitic transistor. The cross-sectional view of a parasitic vertical n-p-n BJT in CMOS process is shown in Fig. 4. The emitter,

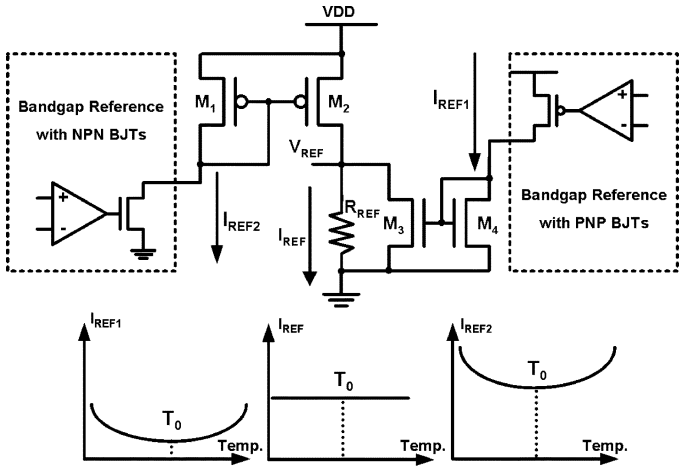

Fig. 3. New proposed sub-1-V curvature-compensated bandgap voltage reference circuit.

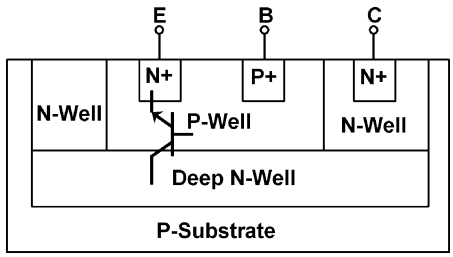

Fig. 4. Cross-sectional view of a parasitic vertical n-p-n BJT in CMOS technology.

base, and collector of the parasitic vertical n-p-n BJT are realized by the n+ diffusion, p-well, and deep n-well layers, respectively.

The new proposed curvature-compensation technique has two output reference currents, $I_{\rm REF1}$ and $I_{\rm REF2}$, which are formed by two bandgap voltage references. The current $I_{\rm REF1}$ comes from a bandgap voltage reference with p-n-p BJTs, whereas the $I_{\rm REF2}$ is produced by another bandgap voltage reference with n-p-n BJTs. The output reference currents act with concave-up shapes in the temperature range from 0 °C to 100 °C, which are designed with the same center temperature (T_0) where the temperature coefficient of $I_{\rm REF1}$ and $I_{\rm REF2}$ is zero. Through the current mirrors, a temperature-independent current generated from the difference between $I_{\rm REF1}$ and $I_{\rm REF2}$ can be produced to compensate for the high-order temperature-dependence factor of $V_{\rm BE}$.

In Fig. 3, an output reference voltage $V_{\rm REF}$ with very low sensitivity to temperature can be obtained across the resistance $R_{\rm REF}$. Thus, the new proposed curvature-compensated bandgap voltage reference has the excellent curvature-compensated result with low-voltage operation.

B. Circuit Implementation

The whole complete circuit to realize the new proposed sub-1-V curvature-compensated CMOS bandgap voltage reference is shown in Fig. 5. The new proposed sub-1-V curvature-compensated bandgap voltage reference is composed by two sub-1-V bandgap cores [2] with two operational amplifiers, which are designed with the two-stage structure. The startup circuit for the self-bias circuit is used to avoid the circuit working in the zero-current state, which is realized

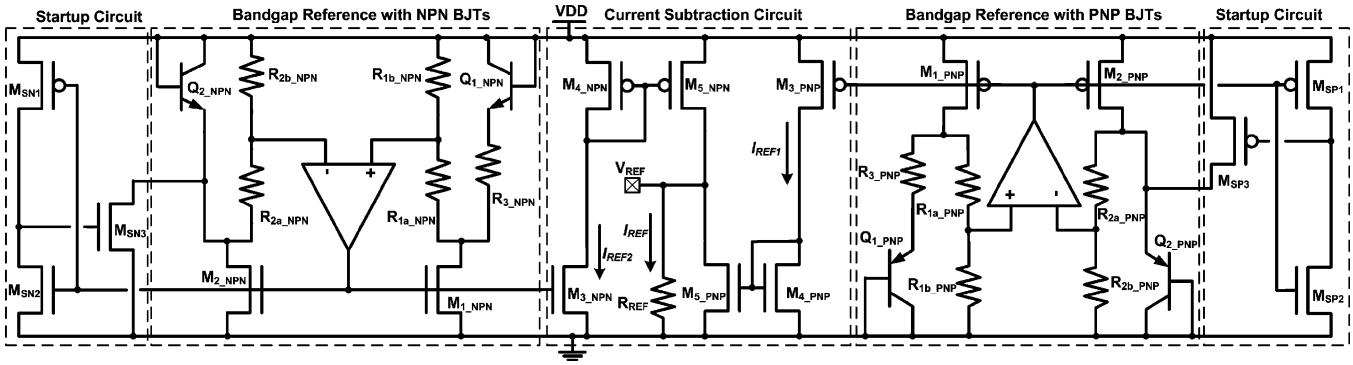

Fig. 5. Complete circuit of the new proposed curvature-compensated bandgap voltage reference for sub-1-V operation.

by $M_{SN1} \sim M_{SN3}$ ($M_{SP1} \sim M_{SP3}$) for bandgap reference with n-p-n (p-n-p) BJTs. $M_{SN1} \sim M_{SN2}$ and $M_{SP1} \sim M_{SP2}$ form the functions of the inverter in the startup circuits. The device dimensions (W/L) of M_{SN1} and M_{SP2} are chosen to be much less than one, respectively. To ensure a complete cutoff operation of M_{SN3} and M_{SP3}, the device dimensions (W/L) of M_{SN3} and M_{SP3} should be designed with the considerations of both maximum supply voltage and operating temperature [2]. The low-voltage operational amplifiers also need the startup circuit to avoid the zero-current state. The same startup circuits in Fig. 5 also use in the low-voltage operational amplifiers with two-stage structure. The current I_{REF1} in Fig. 5 is produced by a sub-1-V bandgap voltage reference with p-n-p BJTs and a p-channel input pair of operational amplifier. The I_{REF1} can be expressed as

$$I_{\mathrm{REF1}} = \frac{|V_{\mathrm{BE\_pnp}}|}{R_{1\_\mathrm{pnp}}} + \frac{1}{R_{3\_\mathrm{pnp}}}\frac{kT}{q}\ln N_{\mathrm{pnp}} \tag{4}$$

where R_{1_pnp} is set to $R_{1a\_\mathrm{pnp}} + R_{1b\_\mathrm{pnp}}$ (or $R_{2a\_\mathrm{pnp}} + R_{2b\_\mathrm{pnp}}$), $R_{1a\_\mathrm{pnp}} = R_{2a\_\mathrm{pnp}}$, and $R_{1b\_\mathrm{pnp}} = R_{2b\_\mathrm{pnp}}$. The current I_{REF2} is produced by another sub-1-V bandgap voltage reference with n-p-n BJTs and an n-channel input pair of operational amplifier. Similarly, I_{REF2} can be expressed as

$$I_{\mathrm{REF2}} = \frac{V_{\mathrm{BE\_npn}}}{R_{1\_\mathrm{npn}}} + \frac{1}{R_{3\_\mathrm{npn}}}\frac{kT}{q}\ln N_{\mathrm{npn}} \tag{5}$$

where R_{1_npn} is set to $R_{1a\_\mathrm{npn}} + R_{1b\_\mathrm{npn}}$ (or $R_{2a\_\mathrm{npn}} + R_{2b\_\mathrm{npn}}$), $R_{1a\_\mathrm{npn}} = R_{2a\_\mathrm{npn}}$, and $R_{1b\_\mathrm{npn}} = R_{2b\_\mathrm{npn}}$. Through the current mirrors, the difference current, I_{REF}, between the I_{REF1} and I_{REF2} can be written as

$$\begin{aligned} I_{\mathrm{REF}} &= K_2 I_{\mathrm{REF2}} - K_1 I_{\mathrm{REF1}} \\ &= \left(\frac{K_2 V_{\mathrm{BE\_npn}}}{R_{1\_\mathrm{npn}}} - \frac{K_1 |V_{\mathrm{BE\_pnp}}|}{R_{1\_\mathrm{pnp}}}\right) \\ &\quad + \frac{kT}{q}\left(\frac{K_2 \ln N_{\mathrm{npn}}}{R_{3\_\mathrm{npn}}} - \frac{K_1 \ln N_{\mathrm{pnp}}}{R_{3\_\mathrm{pnp}}}\right) \end{aligned} \tag{6}$$

where K_1 is the device ratio of M_{4_pnp} and M_{5_pnp}, and K_2 is the device ratio of M_{4_npn} and M_{5_npn}. If the $\ln N_{\mathrm{npn}}$ and $\ln N_{\mathrm{pnp}}$ have the same value and proper pairs of R_{1_npn}, R_{1_pnp}, R_{3_npn}, R_{3_pnp}, K_1, and K_2 are chosen, the difference current (I_{REF}) will ideally become a temperature-independence current. Therefore, a temperature-independence voltage can be achieved across R_{REF}, which has the lower temperature coefficient. The output reference voltage can be expressed as

$$\begin{aligned} V_{\mathrm{REF}} &= R_{\mathrm{REF}}(K_2 I_{\mathrm{REF2}} - K_1 I_{\mathrm{REF1}}) \\ &= R_{\mathrm{REF}}\left[\left(\frac{K_2 V_{\mathrm{BE\_npn}}}{R_{1\_\mathrm{npn}}} - \frac{K_1 |V_{\mathrm{BE\_pnp}}|}{R_{1\_\mathrm{pnp}}}\right)\right. \\ &\quad \left. + \frac{kT}{q}\left(\frac{K_2 \ln N_{\mathrm{npn}}}{R_{3\_\mathrm{npn}}} - \frac{K_1 \ln N_{\mathrm{pnp}}}{R_{3\_\mathrm{pnp}}}\right)\right]. \end{aligned} \tag{7}$$

Thus, the new proposed sub-1-V bandgap voltage reference with the new curvature-compensated technique has an excellent curvature-compensated result.

The minimum supply voltage of the new proposed sub-1-V curvature-compensated bandgap voltage reference can be expressed by

$$\begin{aligned} &V_{DD(\mathrm{Min.})} \\ &= \mathrm{Max}\left[\left(\frac{R_{1b\_\mathrm{pnp}}}{R_{1a\_\mathrm{pnp}} + R_{1b\_\mathrm{pnp}}}|V_{\mathrm{BE\_pnp}}| + |V_{\mathrm{THP}}| + 2|V_{\mathrm{DSsat}}|\right),\right. \\ &\quad \left.\left(\frac{R_{2b\_\mathrm{npn}}}{R_{1a\_\mathrm{npn}} + R_{1b\_\mathrm{npn}}}V_{\mathrm{BE\_npn}} - V_{\mathrm{THN}} + 2V_{\mathrm{DSsat}}\right)\right] \end{aligned} \tag{8}$$

where V_{THP} and V_{THN} are threshold voltages of the pMOS and nMOS transistors, respectively. Since the base–emitter voltages ($V_{\mathrm{BE\_npn}}$ and $V_{\mathrm{BE\_pnp}}$) of the bipolar transistors in (8) are multiplied by the resistance subdivision, this circuit can be operated with sub-1-V supply voltage.

Because the operational amplifier of the bandgap voltage reference is not ideal, the offset voltage (V_{OS}) of the operational amplifier will increase error on the output reference voltage of the bandgap voltage reference. The bnadgap voltage reference in CMOS technology suffers from the effect of the MOS transistor due to the mismatch of transistor dimensions and threshold voltage. In the new proposed sub-1-V curvature-compensated CMOS bandgap voltage reference, the relationship between the output reference voltage and offset voltage (V_{OS}) of the operational amplifier can be rewritten as

$$\begin{aligned} V_{\mathrm{REF}} &= R_{\mathrm{REF}}(K_2 I_{\mathrm{REF2}} - K_1 I_{\mathrm{REF1}}) \\ &= R_{\mathrm{REF}}\left[\left(\frac{K_2}{R_{1\_\mathrm{npn}}}V_{\mathrm{BE\_npn}} - \frac{K_1}{R_{1\_\mathrm{pnp}}}|V_{\mathrm{BE\_pnp}}|\right)\right. \\ &\quad + \frac{kT}{q}\left(\frac{K_2 \ln N_{\mathrm{npn}}}{R_{3\_\mathrm{npn}}} - \frac{K_1 \ln N_{\mathrm{pnp}}}{R_{3\_\mathrm{pnp}}}\right) \\ &\quad \left. + \frac{K_2 R_{1\_\mathrm{npn}}}{R_{1b\_\mathrm{npn}}}V_{\mathrm{OSN}} - \frac{K_1 R_{1\_\mathrm{pnp}}}{R_{1b\_\mathrm{pnp}}}V_{\mathrm{OSP}}\right)\right] \end{aligned} \tag{9}$$

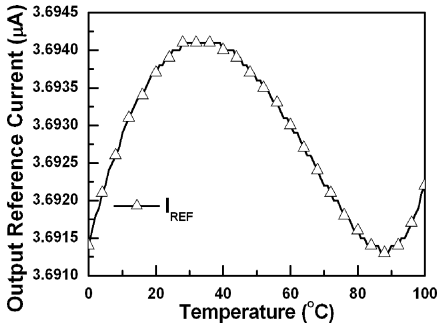

Fig. 6. Simulated output reference current ($I_{\rm REF}$) of the new proposed bandgap voltage reference under different temperatures from 0 °C to 100 °C with a supply voltage of 1 V.

where $V_{\rm OSN}$ and $V_{\rm OSP}$ are the offset voltage of the operational amplifiers with n-channel and p-channel input pairs, respectively. The effect of the $V_{\rm OSN}$ and $V_{\rm OSP}$ is amplified by the resistance ratio of $K_2R_{1\_{\rm npn}}/R_{1b\_{\rm npn}}$ and $K_1R_{1_{\rm pnp}}/R_{1b\_{\rm pnp}}$, respectively. However, this can be reduced by increasing the emitter–areas ratio of the BJTs ($N_{\rm npn}$ and $N_{\rm pnp}$), and the required resistance ratio of $K_2R_{1\_{\rm npn}}/R_{1b\_{\rm npn}}$ and $K_1R_{1\_{\rm pnp}}/R_{1b\_{\rm pnp}}$ is reduced to minimize the negative impact from $V_{\rm OS}$ [14]. In an operational amplifier, the systematic offset can be minimized by adjusting transistor dimensions and bias current in the ratio, while the random offset can be reduced by a symmetrical and compact layout.

IV. Verification

A. Simulation

The bandgap voltage reference with the new proposed curvature-compensated technique has been simulated during the operating temperature from 0 °C to 100 °C. The temperature coefficient of the bandgap voltage reference with the new curvature-compensated technique is around 7.5 ppm/°C under the supply voltage of 1 V. The dependence of $I_{\rm REF}$ (output reference current) on the operating temperature from 0 °C to 100 °C is shown in Fig. 6 under the supply voltage of 1 V.

B. Silicon Measurement

The new proposed sub-1-V curvature-compensated bandgap voltage reference has been fabricated in a 0.25-μm CMOS technology. The proposed sub-1-V curvature-compensated bandgap voltage reference consists of the bandgap cores, bipolar transistors, and resistors. Fig. 7 shows the overall die photograph of the new proposed sub-1-V curvature-compensated bandgap voltage reference. The occupied silicon area of the new proposed curvature-compensated bandgap voltage reference is only 480 μm$\times$ 226 μm. The active devices (MOSFETs) have been drawn in a common centroid layout to reduce process mismatch effect. The bipolar transistors in this chip are the parasitic vertical p-n-p BJTs and n-p-n BJTs. The ratio between the emitter areas of $Q_{1\_{\rm pnp}}$ and $Q_{2\_{\rm pnp}}$ ($Q_{1\_{\rm npn}}$ and $Q_{2\_{\rm npn}}$) is 8. The total emitter area of $Q_{1\_{\rm pnp}}$ ($Q_{1\_{\rm npn}}$) is 200 μm^2 and that of $Q_{2\_{\rm pnp}}$ ($Q_{2\_{\rm npn}}$) is 25 μm^2 in the layout. The resistors in this chip are formed by unsalicided P+ poly resistances, which have minimum process variation and temperature coefficient in the given foundry's CMOS process, to improve the accuracy of resistance

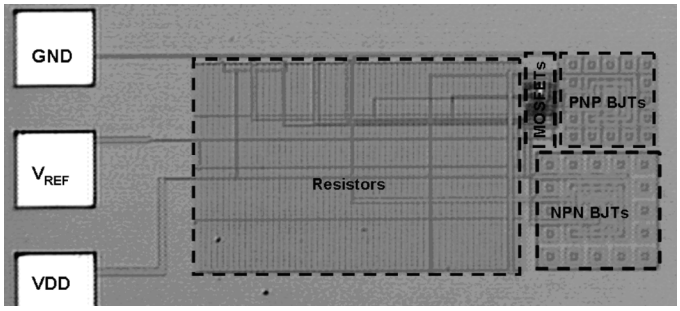

Fig. 7. Die microphotograph of the new proposed curvature-compensated bandgap voltage reference fabricated in a 0.25-μm CMOS process.

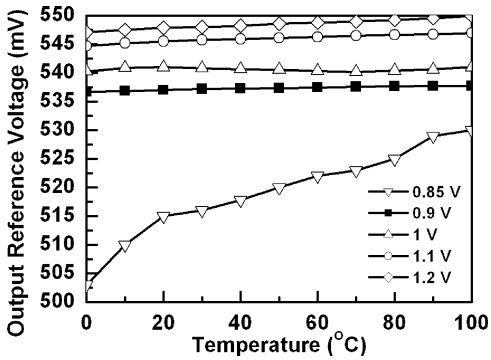

Fig. 8. Measured dependence of output reference voltage on the operating temperature under different supply voltage levels.

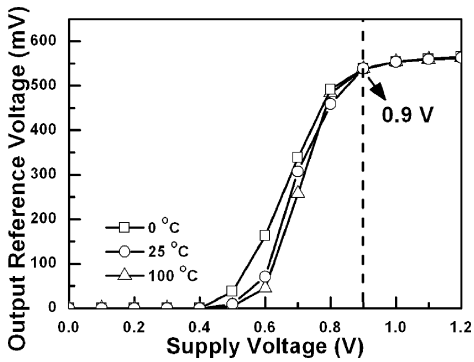

Fig. 9. Measured dependence of output reference voltage on the supply voltage under different operating temperatures.

ratio. The bandgap voltage reference has been measured with the operating temperature varying from 0 °C to 100 °C. The power-supply voltage was set from 0.85 to 1.2 V. The measured results are shown in Fig. 8. The temperature coefficient is around 13.4 ppm/°C with a supply voltage at 1 V. The experimental results in Fig. 9 have confirmed that the minimum supply voltage for the new proposed sub-1-V curvature-compensated bandgap voltage reference is 0.9 V with a temperature coefficient of 19.5 ppm/°C.

About the measurement setup for power-supply rejection ratio (PSRR), a signal with sinusoidal ripple is added onto the power supply to measure the small-signal gain between the supply voltage and output reference voltage. The ac input signal at the power-supply pin must include a dc offset of the normal power-supply voltage, so that the bandgap voltage reference circuit remains powered up [18]. The averaged measured PSRR is -25.5 dB at 10 kHz, whereas the reference output

TABLE I
COMPARISON AMONG THE CURVATURE-COMPENSATED BANDGAP VOLTAGE REFERENCES

	This work	Ref. [10]	Ref. [11]	Ref. [12]	Ref. [14]
Technology	0.25-μm CMOS	1.5-μm BiCMOS	2-μm BiCMOS	BJT	0.6-μm CMOS
$VDD_{(min)}$	0.9 V (1 V)	1.2 V	1.1 V	1 V	2 V
Temperature Range	0 ~ 100 °C	-55 ~ 125 °C	-15 ~ 90 °C	0 ~ 125 °C	0 ~ 100 °C
Temperature Coefficient	Without Trimming 19.5 ppm/°C (13.4 ppm/°C)	After Trimming 6.7 ppm/°C	After Trimming ≅ 20 ppm/°C	After Trimming 4 ppm/°C	After Trimming 5.3 ppm/°C

voltage is 536 mV at 25 °C under the supply voltage of 0.9 V. The comparison among the proposed sub-1-V curvature-compensation bandgap voltage reference of this work with other prior-art curvature- compensation bandgap voltage references is summarized in Table I. From this table, the exponential temperature compensation [10] and piecewise-linear curvature correction [11], [12] are realized by BiCMOS and BJT processes, respectively. The resistor temperature compensation [14] in CMOS process requires a higher supply voltage to realize it. Those prior arts [10]–[12], [14] shown with very low temperature coefficients were achieved by trimming after silicon fabrication. In this brief, the new proposed sub-1-V curvature-compensated bandgap voltage reference can achieve a sufficiently low temperature coefficient without trimming in the general CMOS technology.

V. CONCLUSION

A new proposed sub-1-V curvature-compensated bandgap voltage reference with V_{REF} of 536 mV and temperature coefficient of 19.5 ppm/°C under a supply voltage of 0.9 V was presented, which consumes a maximum current of 50 μA at 0.9 V. The sub-1-V operation of the curvature-compensated bandgap voltage reference has been successfully verified in silicon. The new proposed curvature-compensated technique used to improve the temperature coefficient of sub-1-V bandgap voltage reference can be implemented in general CMOS technology.

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