

5.2-GHz GaInP/GaAs HBT CASCODE LNA WITH 5.5 dB GAIN ENHANCEMENT USING INTER-STAGE LC MATCHING

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ABSTRACT: A gain boosting method without noise-figure degradation by optimizing interstage matching in a cascode low-noise amplifier (LNA) with emitter-degeneration inductor is demonstrated at 5.2 GHz using 2- μm GaInP/GaAs HBT technology. A low-pass LC matching network is inserted in the interstage of a conventional cascode LNA with emitter-degeneration inductor to enhance the gain with the same current consumption. The 2- μm GaInP/GaAs HBT LNA without interstage matching has 14-dB power gain and 2.37-dB noise figure at 5.2 GHz while the 2- μm GaInP/GaAs HBT LNA with interstage matching has 19.5-dB power gain and 2.22-dB noise figure at 5.2 GHz. The current consumption is 2.3 mA and voltage supply is 3.6 V. © 2006 Wiley Periodicals, Inc. *Microwave Opt Technol Lett* 48: 1499–1501, 2006; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.21742

Key words: GaInP/GaAs HBT; LNA; cascode; emitter inductive degeneration; noise

INTRODUCTION

A low-noise amplifier (LNA) is the key element in a wireless receiver. The emitter-inductively-degenerated cascode amplifier topology has been widely used as an LNA. The emitter-degeneration inductor can bring the constant noise-figure circles and constant available-gain circles closer at the expense of lower gain while the cascode configuration can provide better isolation [1–4]. A cascode configuration can be treated as the direct series connection of a common emitter amplifier and a common base amplifier. However, there is no attempt to optimize the power transfer between the output of the common emitter amplifier and the input of the common base amplifier in a cascode configuration. As illustrated in Figure 1, the impedance looking into the input of the cascode device equals to $1/g_m$ while the impedance looking into the output of the common emitter amplifier equals to a resistor of $(C_\pi/C_\mu + 1)/g_m$ in parallel with a capacitor of $C_\pi C_\mu / (C_\pi + C_\mu)$ at frequencies interested. Apparently, the output resistance of the common emitter amplifier is $C_\pi/C_\mu + 1$ times larger than the input resistance of the common base amplifier. It is possible to perform the impedance transformation in the inter-stage of a cascode amplifier for higher transducer gain. In this paper, an LC low-pass inter-stage matching network is inserted between the output of the common emitter amplifier and the input of the common base amplifier to form a matched emitter-inductively-degenerated cascode amplifier, as illustrated in Figure 1. An L-type matching with a series-connected inductor and a shunt capacitor at the collector of the common emitter stage is sufficient for the interstage impedance matching. The series-connected inductor also maintains the current reuse topology [5]. Therefore, an emitter-inductively-degenerated cascode GaInP/GaAs HBT LNA without the interstage matching network and an emitter-inductively-degenerated cascode GaInP/GaAs HBT LNA with the interstage matching network, as shown in Figure 1, are implemented in adjacent areas of the same wafer for comparison purposes.

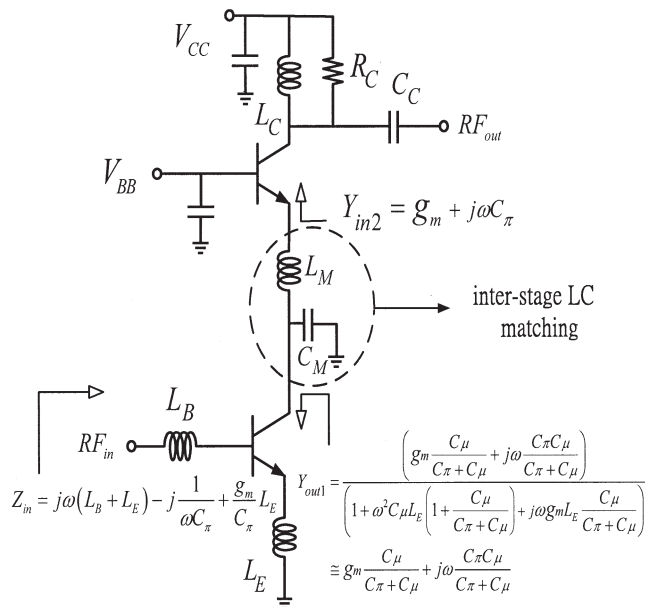


Figure 1 Schematic of a matched emitter-inductively-degenerated cascode LNA with an LC low-pass interstage matching network

CIRCUIT DESIGN

The chip micrograph for both LNAs is shown in Figure 2. The 2- μm GaInP/GaAs HBT technology has a peak f_T around 40 GHz. The L_E shown in Figure 1 is the emitter-degeneration inductor while L_B and L_C are the input-matching inductor and the output-matching inductor, respectively. For a simple common emitter stage, the optimum impedance for noise figure matching is a complex impedance while the optimum impedance for power gain matching is close to a pure imaginary impedance [6–9]. It is not possible to achieve simultaneous power gain and noise matching for a simple common emitter stage.

An emitter-degeneration inductor can alleviate the problem. The emitter-degeneration inductor results in a resistance, $(g_m L_E)/C_\pi$, and maintains the same reactance when looking into the base, as shown in Figure 1. At the same time, the emitter-degeneration inductor only changes $-j\omega L_E$ to the optimum noise-matching impedance and keeps the real part unchanged. In other words, the optimum gain matching moves along a constant reactance curve and the optimum noise impedance moves along a constant resistance curve in the Smith Chart when the emitter-degeneration inductor is introduced. The emitter inductive degeneration can bring the constant noise-figure circles and constant available gain circles closer at the expense of lower gain. The design approach for this GaInP/GaAs HBT LNA is a measurement-based design. The measurement-based design is very accurate, but requires a test run to generate circuit element database. High-frequency noise-parameter and scattering-parameter measurements were performed on different device sizes at various bias points after the test run was made [10]. An optimum L_E inductor in terms of simultaneous noise and gain matching is chosen for a given device at a certain biased point. L_E also shows in the reactance part of the input impedance, as shown in Figure 1, and normally is not enough to cancel the reactance part caused by the C_π . Then, the series L_B is designed to achieve the impedance matching. A cascode configuration has high output impedance when looking into the output of the cascode device. The bandwidth of a cascode amplifier is usually limited by the output-matching bandwidth. The output-matching bandwidth is very limited especially if a pure reactive

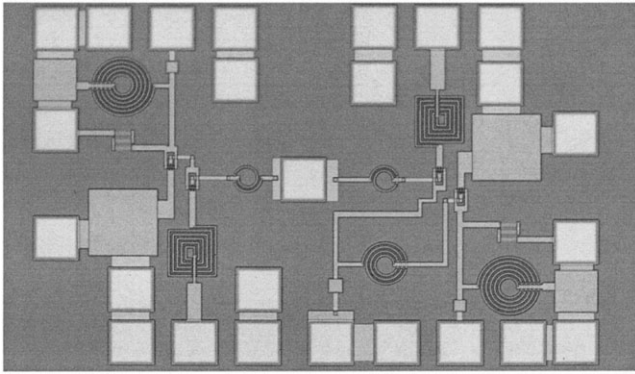


Figure 2 Chip micrograph of LNAs. The emitter-inductively-degenerated cascode LNA without the interstage matching network is shown on the left-hand side and the emitter-inductively-degenerated cascode LNA with the interstage matching is shown on the right-hand side

matching is used at the output stage. Here, a resistor R_C is used in the output stage to increase the output matching bandwidth and helps to stabilize the circuit at the cost of lower gain. The amplifier demonstrated in this paper can actually be used in the range of 5.2 to 5.8 GHz for an output return loss of at least 10 dB. An L-type LC matching network is used to match the output impedance. The L_C inductor also alleviates the dc voltage drop in the resistor. The matching emitter-inductively-degenerated cascode LNA has all the identical design parameters as the conventional emitter-inductively-degenerated cascode LNA except for the interstage matching. An LC low-pass interstage matching network is inserted between the output of the common emitter amplifier and the input of the common base amplifier for the matched emitter-inductively-degenerated cascode amplifier, as illustrated in Figure 1. An L-type matching network with a series-connected inductor L_M and a shunt capacitor C_M at the collector of the common emitter stage is sufficient for the interstage impedance matching. The series-connected inductor also maintains the current reuse topology. The inductors used in the HBT LNA design are 1.5 circular turns for L_E , 5.5 square turns for L_B , 5.5 circular turns for L_C , and 3.5 circular turns for L_M , respectively. A two-finger HBT device is used for the common emitter stage and the cascode device. The $2.4 \times 3 \times 2$ HBT device used here has a $2.4\text{-}\mu\text{m}$ emitter width, $3\text{-}\mu\text{m}$ unit emitter length, and two emitter fingers.

EXPERIMENTAL RESULTS

The measurement results for gain and noise figure of the $2\text{-}\mu\text{m}$ GaInP/GaAs LNAs with/without interstage matching are shown in

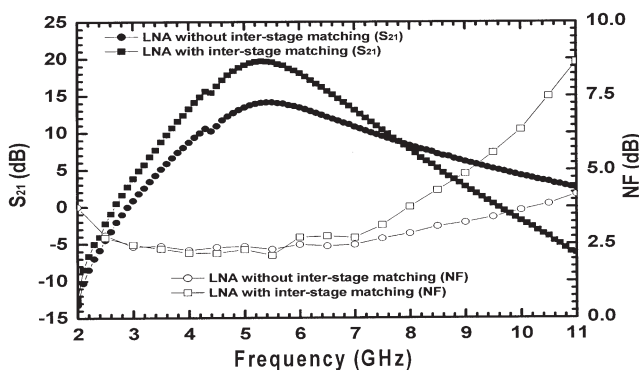


Figure 3 Measured power gain and noise figure for emitter-inductively-degenerated cascode LNAs with/without the interstage matching network

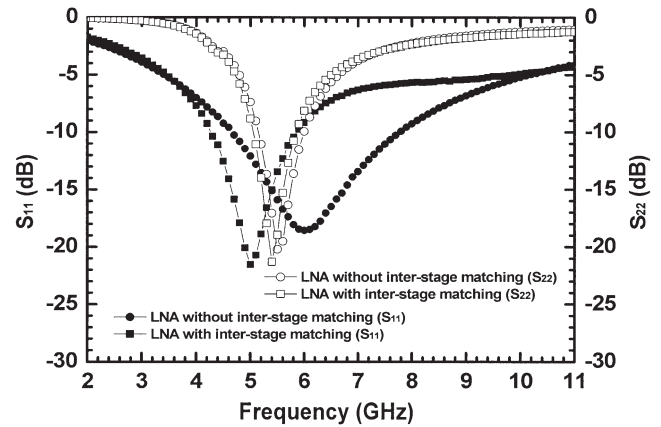


Figure 4 Measured input/output return loss for emitter-inductively-degenerated cascode LNAs with/without the interstage matching network

Figure 3. The LNA with interstage matching has 19.5-dB power gain and 2.22-dB noise figure at 5.2 GHz, while the conventional LNA without interstage matching has 14-dB power gain and 2.37-dB noise figure at 5.2 GHz. Both circuits are biased at 3.6 V with a current consumption of 2.3 mA. The matched LNA has a narrower gain bandwidth than the conventional LNA, and the power gain is the same for the low-frequency range because of the low-pass characteristics of the interstage matching network.

The input and output return losses of both LNAs are shown in Figure 4. The input return losses of both LNAs are almost the same for frequencies below 4 GHz, and the optimum input return loss point shifts slightly toward lower frequency for the matched LNA. The input return losses of both LNAs deviate for frequencies above 4 GHz due to the effect of low-pass interstage matching. The input return loss at 5.2 GHz is 13.5 dB for the LNA without interstage matching and 19 dB for the LNA with interstage matching. The output return losses of both LNAs are almost the same for frequencies up to 10 GHz because of the high isolation property of the cascode device. The optimum output return loss point also shifts slightly toward lower frequency for the matched LNA. The output return loss at 5.2 GHz is 11 dB for the LNA without interstage matching and 14 dB for the LNA with interstage matching. Power performance for two-tone intermodulation at 5.2 GHz is also illustrated in Figure 5. OIP_3 is 9 dBm for the conventional LNA and is 7 dBm for the matched LNA. The $2\text{-}\mu\text{m}$ GaInP/GaAs HBT LNA with interstage matching has 5.5-dB gain enhancement at 5.2

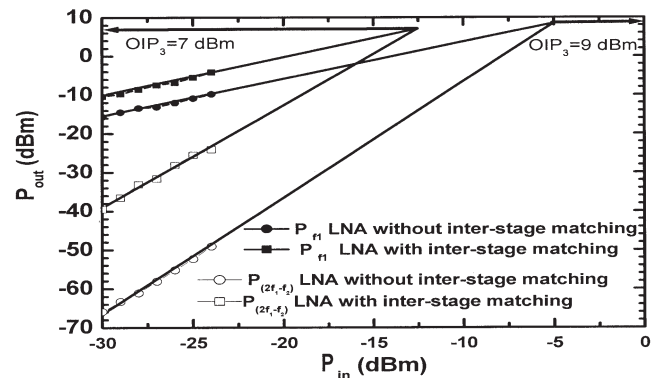


Figure 5 Measured two-tone power performances for emitter-inductively-degenerated cascode LNAs with/without the interstage matching network

GHz and almost no changes in the rest of properties such as noise figure, current consumption, input return loss, and output return loss when compared with the 2- μm GaInP/GaAs HBT LNA without interstage matching. The bandwidth of a cascode amplifier is usually limited by the output matching bandwidth. A resistor R_C is used in the output stage to increase the output matching bandwidth and helps to stabilize the circuit. The amplifier demonstrated in this paper can be actually used in the range of 5.2 to 5.8 GHz for output return loss of at least 10 dB. The 2- μm GaInP/GaAs HBT LNA without interstage matching has 13.5-dB power gain and 2.4-dB noise figure at 5.8 GHz while the 2- μm GaInP/GaAs HBT LNA with interstage matching has 18.5-dB power gain and 2.43-dB noise figure at 5.8 GHz. The input return loss at 5.8 GHz is 18 dB for LNA without interstage matching and 10.5 dB for LNA with interstage matching. The output return loss at 5.8 GHz is 13.5 dB for LNA without interstage matching and 11 dB for LNA with interstage matching. There is still 5 dB power gain enhancement at 5.8 GHz with almost no changes in the rest of properties.

DISCUSSION AND CONCLUSION

A means to enhance power gain by inserting an interstage matching in a cascode LNA has been demonstrated. The matched LNA maintains the current reuse topology and has 5.5-dB power gain enhancement at 5.2 GHz without degradation in any other property. The method demonstrated here can be directly applied to any other technology. The 2- μm GaInP/GaAs HBT LNA without interstage matching has 14-dB power gain and 2.37-dB noise figure at 5.2 GHz, while the 2- μm GaInP/GaAs HBT LNA with interstage matching has 19.5-dB power gain and 2.22-dB noise figure at 5.2 GHz. The current consumption is 2.3 mA and voltage supply is 3.6 V.

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INTERNAL FOLDED LOOP ANTENNA WITH TUNING NOTCHES FOR GSM/GPS/DCS/PCS MOBILE HANDSET APPLICATIONS

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ABSTRACT: A novel compact quad-band internal antenna for mobile handsets operating the GSM (880–960 MHz), GPS (1575 \pm 10 MHz), DCS (1710–1880 MHz), and PCS (1850–1990 MHz) bands is proposed and implemented. The proposed antenna consists of a feeding strip, shorting strip, and folded loop radiating element with embedded tuning notches. Embedding the notches changes the current flow on the surface of the loop radiator so that the resonant frequencies can be controlled independently by their size and position. The measured impedance bandwidth (VSWR < 2) of the proposed antenna is 11.3% at GSM band and 27.4% at higher bands including GPS/DCS/PCS. The measured peak gains are 0.51, 2.06, 0.52, and 1.34 dBi, at the GSM, GPS, DCS, and PCS bands, respectively. © 2006 Wiley Periodicals, Inc. *Microwave Opt Technol Lett* 48: 1501–1504, 2006; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.21743

Key words: quad-band; internal antenna; folded loop; tuning notches

1. INTRODUCTION

In conjunction with the rapid growth of mobile communications, there is a great demand in developing an internal antenna that is capable of achieving multiband performance. Compared with conventional antennas, it is somewhat complicated for an internal antenna to control the typical parameters such as bandwidth, efficiency, and radiation pattern within the limited antenna volume. Designing an internal antenna for a mobile handset is even more critical, especially when a multiband system is required. To find a solution, the planar inverted-F antenna (PIFA) has been chosen as the main candidate. Many new studies on a multiband internal antenna based on PIFA concepts have been presented [1–3]. The most typical method is to obtain multiple resonances from a quarter wavelength PIFA by inserting various types of slits or slots [4, 5]. Though this technique is very convenient and

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