Geometrical Effect of Bump Resistance for Flip-Chip Solder Joints: Finite-Element Modeling and Experimental Results

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The bump resistance of flip-chip solder joints was measured experimentally and analyzed by the finite-element method. Kelvin structures for flip-chip solder joints were designed and fabricated to measure the bump resistance. The measured value was only about 0.9 mΩ at room temperature, which was much lower than that expected. Three-dimensional (3-D) modeling was performed to examine the current and voltage distribution in the joint. The simulated value was 7.7 mΩ, which was about 9 times larger than the experimental value. The current crowding effect was found to be responsible for the difference in bump resistance. Therefore, the measured bump resistance strongly depended on the layout of the Kelvin structure. Various layouts were simulated to investigate the geometrical effect of bump resistance, and a significant geometrical effect was found. A proper layout was proposed to measure the bump resistance correctly. The Kelvin structure would play an important role in monitoring void formation and microstructure changes during the electromigration of flip-chip solder joints.

Key words: Electromigration, solder, bump resistance, flip chip

INTRODUCTION

Flip-chip technology has become the most important packaging method for fine-pitch devices.[1,2] One of its advantages is that a large number of tiny solder bumps can be fabricated into an area array on a chip as input/output (I/O) interconnections. The diameter of the bumps is 100 μm or less, and it continues to shrink. As the dimension of the bumps decreases, the resistance of the solder bumps may continue to increase accordingly. Typically, the resistance of a solder bump was estimated to be of the order of few milli-ohms, whereas the resistance of the metallization trace ranges from few hundreds to few thousands of milli-ohms, depending on its dimension. The resistance is quite small compared with the resistance of the metallization traces.[3] Therefore, daisy-chain structures cannot detect the slight resistance changes due to void formation or microstructure changes in solder joints.

The Kelvin structure has been used to measure via or contact resistance in Al and Cu interconnect for over 20 years, in which four electrical terminals are employed to measure the contact resistance.[4,5] The geometrical effect of the contact resistance has been investigated by Natan et al.[6] Liu et al. investigated the electrical resistance of the solder joints, but the current crowding effect was not considered.[7] Electromigration has become an important reliability issue for flip-chip packages due to the continuous shrinking of the solder joints.[1,8] Although the bump resistance may not be a critical issue for signal delay consideration, it can be used to monitor the failure of the electromigration test. Recently, many researchers have been using bump resistance changes to monitor electromigration behavior.[9–11] Gee et al. has designed this structure to measure bump resistance in the ball grid array during electromigration.[9] Ebersberger et al. used it to monitor the failure of electromigration in flip-chip solder joints.[11] However, no literature has been found on measuring the bump resistance.

In addition, from a scientific point of view, the bump resistance may be of interest, since serious current crowding occurs in the solder joints, and the joint comprises several materials. Compared with the Al and Cu interconnects, the dimension of the solder joints is quite large. Therefore, there

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are several ways to design the Kelvin bump structure. However, no significant effort has been made on the measurement and modeling of the bump resistance. The effect of the crowding effect on bump resistance has not been studied. In this paper, we measured the bump resistance by Kelvin structure and employed three-dimensional (3-D) finite-element modeling to investigate the geometrical effect of bump resistance. This study provides a deeper understanding of the bump resistance in flip-chip solder joints.

EXPERIMENTAL AND SIMULATION

We have designed and fabricated the Kelvin structure for flip-chip eutectic SnPb solder joints. Figure 1a shows the plan-view schematic for the structure. The test structure consisted of four bumps, in which the Al trace connected them together. The Al trace was 1.5-μm thick and 100-μm wide. The pitch for the solder joints was 1 mm. Six Cu lines in the FR5 substrate connected to the four bumps, and they were labeled as nodes 1 through 6, as shown in the figure. The dimensions of the Cu lines were 30-μm thickness and 100-μm width. The bump connected to node 3, and node 6 was used to investigate the geometrical effect of bump resistance. Through these six Cu lines, various experimental setups can be performed to measure the bump resistance for bump 2. In this study, four approaches were adopted to measure the bump resistance. The experimental setup for the first approach was shown in Fig. 1b. The current was applied through nodes 1 and 2, and the voltage drop was monitored through nodes 4 and 5. This approach measures the voltage drop on the left-hand side of the bump. The second experimental setup is illustrated in Fig. 1c, in which the current was applied through nodes 1 and 4, and the voltage change was examined using nodes 2 and 5. For this approach, the voltage drop across the diagonal of the bump was measured. The third approach is shown in Fig. 1d; current was applied through nodes 1 and 2, and the voltage difference was measured through nodes 3 and 5. The fourth approach measured the voltage drop across nodes 5 and 6 when current was applied through nodes 1 and 2, as depicted in Fig. 1e.

The schematic of the flip-chip bumps used in this study is shown in Fig. 2a. The under bump metallization (UBM) was Ti/Cu/Cu. The titanium layer of 0.1 μm was sputtered on the oxidized Si wafer and acted as an adhesion layer. Copper (0.5 μm) was then sputtered on the Ti layer and served as a seed layer for the subsequent electroplating process. Then, a 5-μm Cu was electroplated on the Ti/Cu layers. Photolithography was applied to define the UBM opening. Afterward, the UBM opening was formed by the wet etching process. Due to fast etching of Cu, the diameter of Cu UBM was smaller than that of Ni UBM, as shown in Fig. 2a. The passivation and UBM openings are 110 μm and 125 μm in diameter, respectively. Eutectic SnPb solder was electroplated onto UBM, followed by reflowing in an infrared oven at 220°C for about 1 min. The solder bumps were jointed to the FR5 substrates. The pad metallization consisted of 1-μm Au and 5-μm electroless Ni layers. The dimension of the pad opening was 115 μm in diameter. Figure 2b shows a fabricated solder bump. The bump height was approximately 75 μm. The electroplated Cu on the chip side reacted with the solder to form Cu_6Sn_5 intermetallic

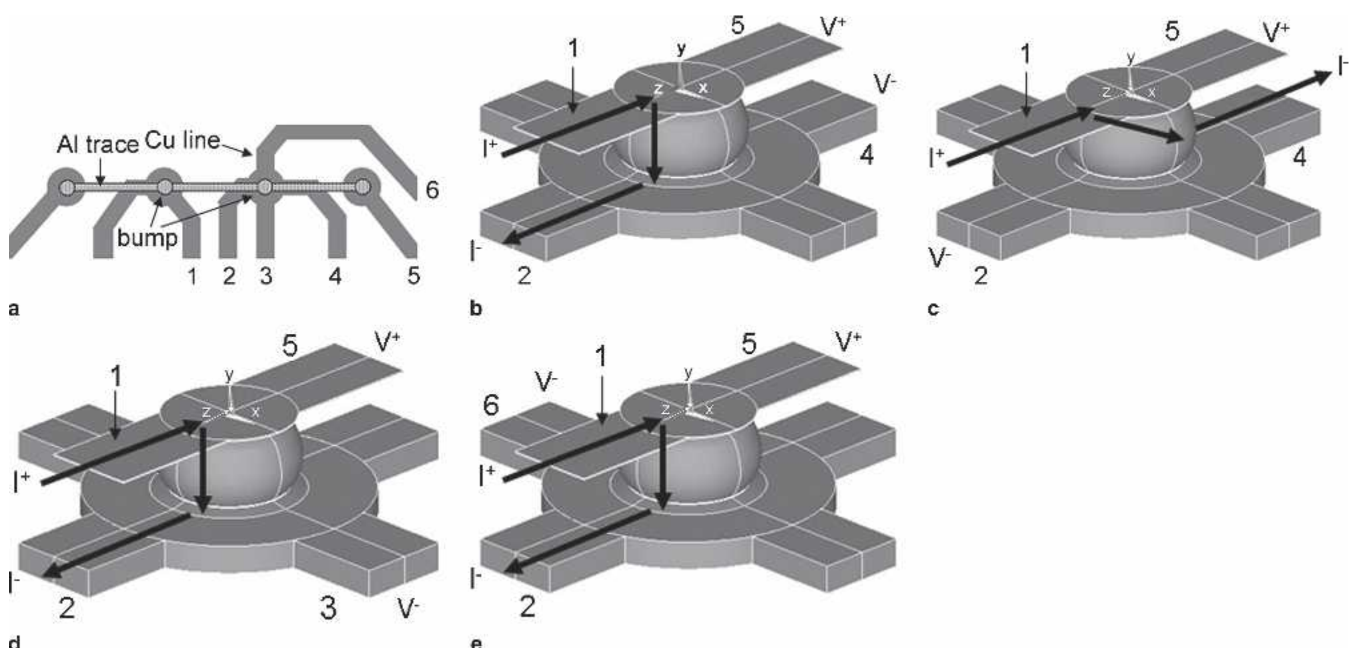
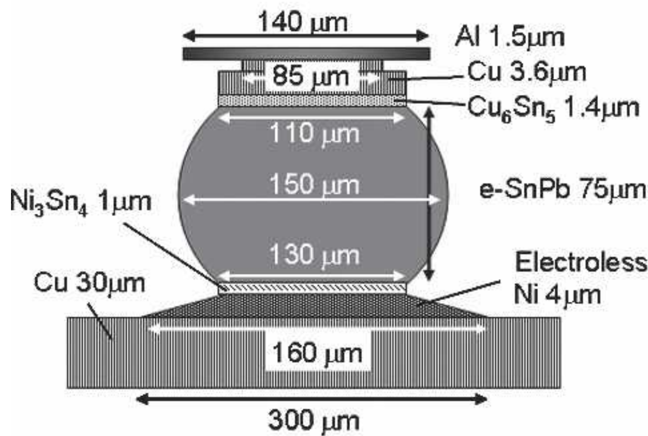


Fig. 1. (a) Plan-view schematic of the layout design. The Al trace connected all four solder bumps together. Six nodes in the substrate side are labeled. A cross-sectional diagram showing the experimental setup for (b) approach 1, (c) approach 2, (d) approach 3, and (e) approach 4.



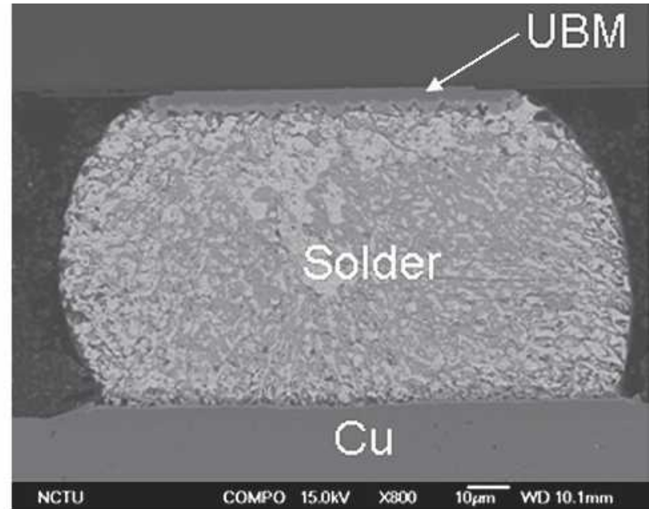


Fig. 2. (a) Schematic structure for the solder bump used in this study. (b) Cross-sectional SEM image for a SnPb solder bump with a bump height of 75 μm.

compounds (IMCs), and the average thickness of the IMC was 1.4 μm. Ni_3Sn_4 IMCs were formed on the substrate side in the interface of the electroless Ni and the solder, and the average thickness of the IMCs was 1 μm.

The 3-D simulation model with meshization used in this study is shown in Fig. 3. The dimension of the solder joint matched the real joints, except for the Ti and IMC layers. Since the Ti layer was quite thin compared with the bump height, it was ignored in the simulation model to avoid difficulty in meshization. In addition, we assumed both the Cu_6Sn_5 and Ni_3Sn_4 IMCs to be layered type. The resistivity values of the materials used in this simulation are listed in Table I. Ansys simulation software was employed to do the simulation, and the model used was a SOLID69 eight-node hexahedral coupled field element. The dimension of the mesh was 3.8 μm. A current of 0.2 A was applied in the modeling.

The measurement of bump resistance was carried out by applying 0.2 A in the desired solder bump. The temperature increase due to Joule heating effect was less than 1°C, as detected by an infrared microscope.[3] Therefore, the amount of current can provide an adequate voltage drop across the solder bump for resistance measurement, but has a negligible Joule heating effect. The power supply used in this measurement was Keithley (Keithley Instruments, Cleveland, OH) 2,400 with a 0.1-μV resolution.

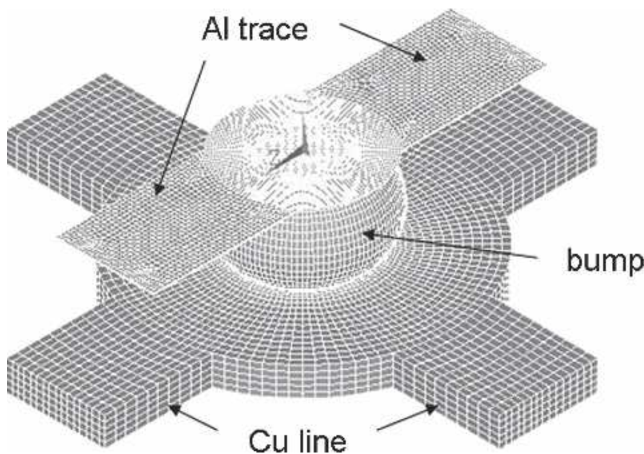


Fig. 3. The simulation model with meshization in this study.

RESULTS AND DISCUSSION

Surprisingly, the measured bump resistance was much lower than that expected for the four approaches shown in Fig. 1b and e. Figure 4 shows the typical bump resistances as a function of temperature up to 150°C for the four approaches. For bump resistance measured by approach 1, the value was only 0.89 mΩ at room temperature. The resistance increased with the increase in temperature, and it was attributed to the temperature coefficient of resistivity (TCR). If we assume the TCR to be linear, the estimated TCR for the solder joint was $5.1 \times 10^{-3}\ K^{-1}$. The measured bump resistance comprised the contribution from Al, Cu, Ni, Sn, and Pb materials. Therefore, the TCR may be a combination of the above materials. The TCR values for the bulk Al, Cu, Ni, Sn, and Pb are 4.2, 4.3, 6.8,

Table I. The Properties of Materials Used in the Simulation Models

Materials	Resistivity (μΩ · cm at 20°C)
Al	3.2
Cu	1.7
IMC Cu_6Sn_5	17.5
IMC Ni_3Sn_4	28.5
Sn63Pb37	14.6
Electroless Ni	70

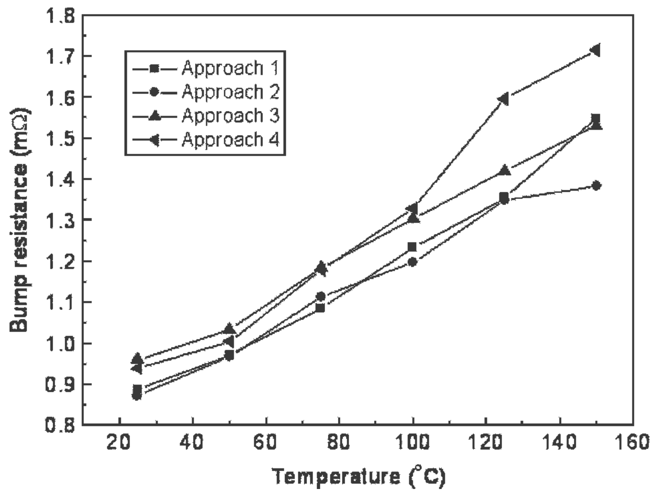


Fig. 4. The measured bump resistance as a function of temperature up to 150°C for the four approaches.

4.6, and 4.2×10^{-3} K^{-1}, respectively. Hence, the measured TCR seems to be quite reasonable. The measured bump resistance for the same bump was 0.87 mΩ, 0.96 mΩ, and 0.94 mΩ at room temperature for the second, third, and fourth approaches, respectively. The bump resistances measured by approaches 3 and 4 are slightly larger than those by approaches 1 and 2. The temperature dependence of bump resistance was quite close to that measured by the first approach. The estimated TCR values are 4.4, 4.3, and 4.9 for the three approaches, respectively.

To examine the current and voltage distribution in the solder joints, 3-D simulation was performed to provide more understanding of the effect of current crowding on the bump resistance measurement. Figure 5a shows the current density distribution in the solder joint upon applying 0.2 A current. The current crowded into the solder bump

Fig. 5. (a) Simulation results showing the current density distribution across the solder joint upon applying 0.2 A. (b) The voltage distribution in the solder joint. Voltage drop mainly occurred in the Al trace. (c) Cross-sectional view along the YZ plane in (b) showing that voltage drop inside the solder bump mainly occurred at the high current density region. (d) Voltage distribution in the solder joint, excluding the Al trace and the Cu line. Six positions were labeled for measuring the voltage drop.

in the vicinity of the entrance of the Al trace, and only a small amount of current flows in the opposite side of the joint. Figure 5b illustrates the voltage distribution in the solder joint. Since the resistance of the Al trace was much larger than that of the solder joint due to its smaller cross section, most of the voltage dropped in the Al trace. Figure 5c depicts the cross-sectional view along the YZ plane in Fig. 5b. Apparently, voltage drop mainly occurred at the left-hand side of the bump, which was the current crowding region. The voltage drop on the left-hand side was approximately 9 times larger than that on the right-hand side. This may cause large variation in the measurement of bump resistance. Hence, the measured voltage strongly depends on the layout of the Kelvin structure.

To investigate the geometry effect of the bump resistance, voltage at various positions was examined in the solder joint. Figure 5d shows the voltage distribution in the solder joint, excluding the Al trace and the Cu line. Two positions, 1 and 5, in the chip side were labeled. On the substrate side, positions 2, 3, 4, and 6 were labeled. The definition of the positions matched the six nodes in Fig. 1a. When the current was applied through nodes 1 and 2, the voltages in the six positions were examined. The results are listed in Table II. The voltages in the chip side were obtained by averaging the voltages in the junction of the Al trace and the Al pad. The junction area was approximately 110 μm × 1.5 μm. Voltages in the substrate side were estimated by averaging the voltages in the junction of the Cu line and the Cu pad. The junction area was approximately 110 μm × 30 μm. It was found that the voltage drop across positions 1 and 2 was 1.54 mV, whereas it was only 0.15 mV across positions 4 and 5 (first approach), and it was 0.17 mV across positions 3 and 5 (third approach) as well as positions across 5 and 6 (fourth approach). Therefore, the simulated bump resistance was 0.77 mΩ, 0.83 mΩ, and 0.83 mΩ for the first, third, and fourth approaches, respectively. Similarly, the theoretic bump resistance for the second approach can be obtained by simulation, and the value was 0.76 mΩ. Table III summarizes the experimental and simulation results on bump resistances for the four approaches. The measured bump resistance was 0.89 mΩ, 0.87 mΩ, 0.96 mΩ, and 0.94 mΩ, whereas the simulated value was 0.77 mΩ, 0.76 mΩ, 0.83 mΩ, and 0.83 mΩ for the four approaches, respectively. The experimental results were approximately 12–14% higher than the simulated values. The difference may be attributed to the variation in bump height and the temperature differences between the simulation and the measurement. In the simulation, the resistivity values adopted were at 20°C, but the measurement was done in the temperature range 25–30°C. Although the experimental values were higher than the simulated ones, the geometrical effect shows the same trend for both results. Therefore, the simulation results supported the experimental data. These results indicate that a serious current crowding effect occurs in flip-chip solder joints.

Table II. The Simulation Voltages at the Six Positions in Figure 5(b)

	Positions for Voltage Measurement					
	1	**2**	**3**	**4**	**5**	**6**
Voltage (mV)	1.66	0.12	0.19	0.21	0.36	0.19

Table III. Experimental and Simulation Results on Bump Resistances for the Four Approaches

Node Approach	Experimental (mΩ)	Simulation (mΩ)
First	0.89	0.77
Second	0.87	0.76
Third	0.96	0.83
Fourth	0.94	0.83

On the basis of the simulation results, the real bump resistance should be equal to the voltage difference between the current entrance point and the leaving points divided by the current. In the case of the first approach, as shown in Fig. 5, the real bump resistance should be 7.7 mΩ. However, the measured bump resistances for the four approaches were less than 0.9 mΩ. The low measured values for bump resistance may be attributed to the serious crowding effect in the solder joints. Our previous 3-D simulation shows that the current did not spread uniformly in the UBM opening. Instead, the current crowded into the solder bump in a small volume near the entrance point of the Al trace.[12] Little current passed through the opposite end of the entrance point of the current. Therefore, the voltage drops measured by the first approaches were much lower. For the third and fourth approaches, the Kelvin probes for measuring voltage drops were closer to the current crowding region than those in the first and second approaches. Consequently, the measured values by the third and fourth approaches were larger than those by the first and second approaches.

Three components, the Al pad (disc), UBM/solder, and Cu pad (disc), as shown in Figs. 6a through c, may contribute to the bump resistance. From the simulation results, the bump resistance was 7.7 milli-ohm. In this paper, we denoted the bump resistance as the voltage drop across positions 1 and 2, divided by the applied current. Therefore, the bump resistance included the above three components. Among them, the Al disc contributed most to the bump resistance. This is because the cross section of the Al disc was quite small, approximately 1.5 μm × 100 μm. The current needs to flow through part of the Al disc adjacent to the Al trace in order to enter the solder joint through the passivation opening, as shown in Fig. 6a. The resistance of the partial Al disc was estimated to be

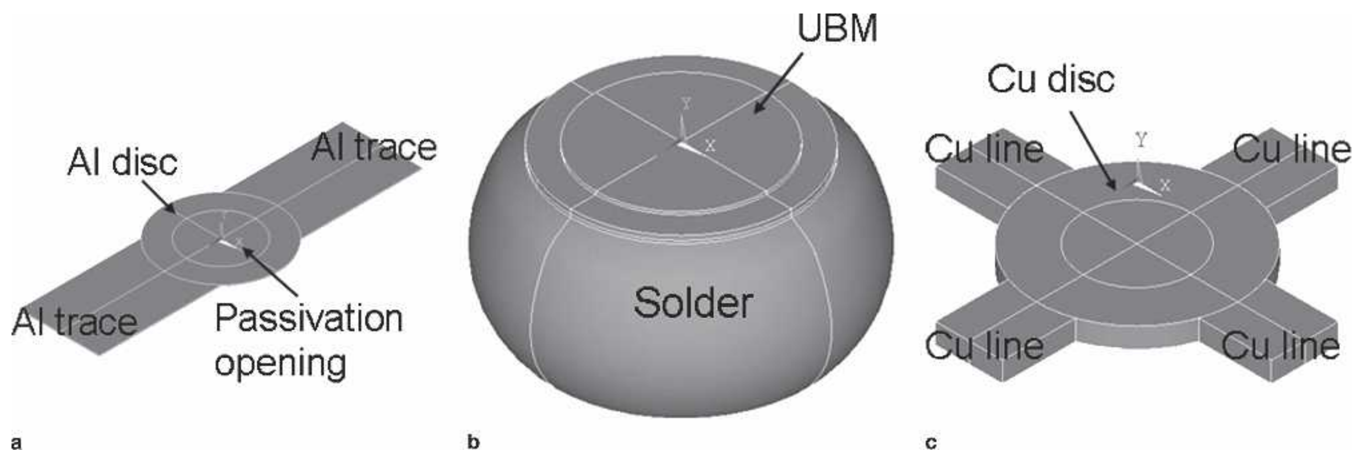


Fig. 6. Three components contributing to the bump resistance, including (a) the Al disc, (b) the UBM/solder, and (c) the Cu disc. The resistance of the Al disc contributed about 79% of the total bump resistance.

5.5 milli-ohms, which was about 72% of the bump resistance. In addition, since the cross sections for UBM/solder and part of the Cu disc were much larger than that of the Al disc, they contributed only the rest of 21% resistance.

This bump resistance of 7.7 mΩ was larger than expected. We assume that the current flows through the joint uniformly, as illustrated schematically in Fig. 7a. The resistance based on this assumption was estimated to be only 1.0 mΩ for our solder joints. In fact, the current path was not uniform, as depicted schematically in Fig. 7b. The current entered the solder joint from the Al trace, drifting in the left-hand side of the Al disc, crowding into the solder joint from the passivation opening, spreading out gradually as well as drifting toward the substrate side, and leaving the joint from the Cu disc. Due to this current path, the bump resistance was about 7.7 times larger than that for uniformly distributed current.

The thermal-electrical effect might affect the measurement of bump resistance. When two materials are joined together and a temperature difference ΔT is applied between two junctions, an open circuit voltage ΔV is established in the circuit when the electric current I approaches zero. The Seebeck coefficient, α, is defined as[13,14]

$$\alpha = \left(\frac{\Delta V}{\Delta T}\right)_{I=0}$$

Therefore, if there is a temperature difference across the solder bump, there would be a voltage drop there. To estimate the magnitude of the voltage drop due to the thermal-electrical effect in this measurement, we assume that the temperature difference across the solder bump is 1°C, which is reasonable since the Joule heating effect in this study was less than 1°C. The Seebeck coefficients at 300 K for Al, Cu, and Sn are −1.66 μV/K, 1.83 μV/K, and −1 μV/K. Therefore, the voltage drop due to the thermal-electrical effect is approximately 1.5 μV, which is about 1–2% of the voltage drop in the solder bump with applied 0.2 A. As a result, the influence of the thermal-electric effect could be neglected in this study.

Based on the above results and discussion, a layout for Kelvin structure is proposed to measure the

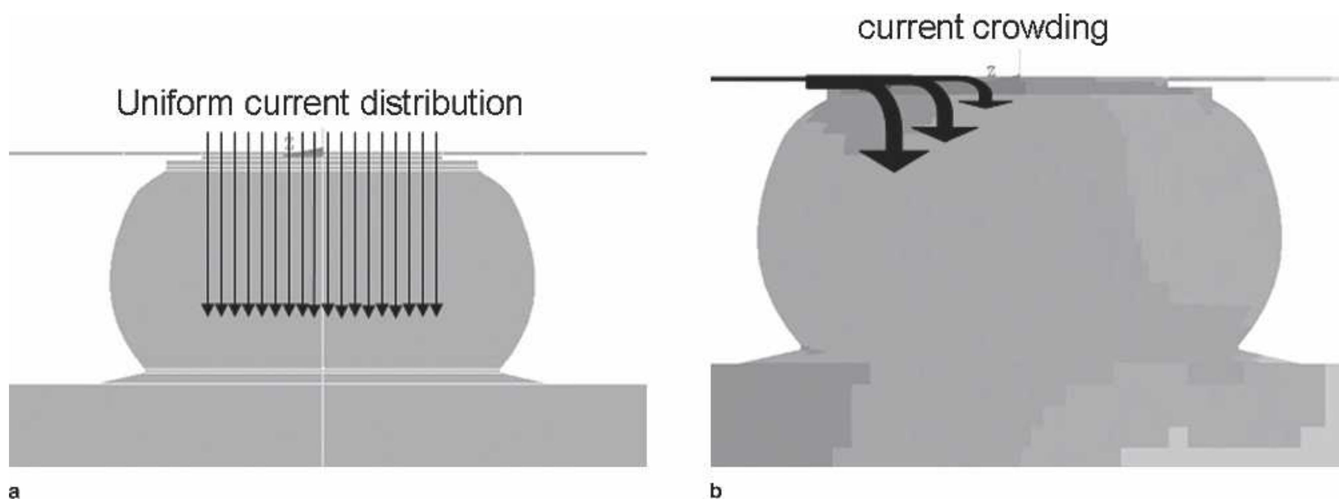


Fig. 7. Schematic drawings showing (a) the uniform current distribution and (b) the current crowding effect in the solder joints.

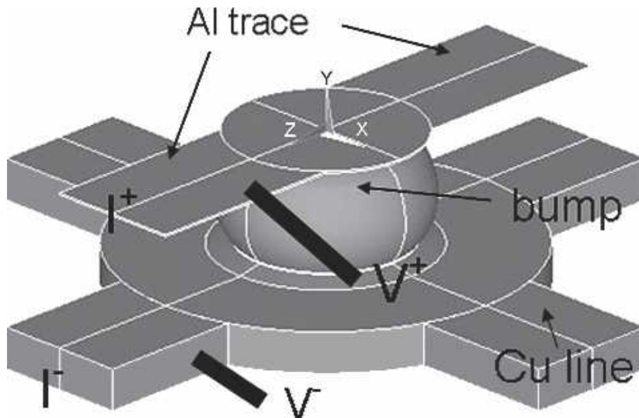


Fig. 8. Proposed layout of Kelvin structure for measuring the bump resistance of the flip-chip solder joint.

bump resistance, as shown in Fig. 8. It is denoted as approach 5 in this paper. One voltage terminal is connected near the entrance of the Al trace, and the other voltage terminal could be at any position on the substrate side, since the voltage at the substrate was almost constant. However, the measured value is the combination of part of the Al trace and the bump resistance. The bump resistance can be obtained by excluding the resistance of the Al trace. When the terminal is very close to the bump, the measured value will be near the bump resistance. Gee et al. has used this structure to monitor the bump resistance changes during electromigration.[9] The resistance they measured was as high as 26 mΩ. This high value may be mainly attributed to the larger bump height of about 250 μm and to the resistance comprised part of the resistance of the Al trace.

Although the bump resistance may not be a critical issue for signal delay consideration, it has been used to monitor the resistance change due to void formation during reliability tests.[14,15] Zhang and Baldwin fabricated the Kelvin bump structure to monitor the bump resistance changes during power cycling, and the resistances they measured were about 2–4 mΩ at room temperature for eutectic solder bumps with 125-μm diameter.[14] Amagai et al. defined the failure of the solder joint during the drop test by an increase in bump resistance by 1.2 times.[16] To examine the resistance change due to void formation, a void was inserted in the simulation model, as shown in Fig. 9. The void depleted approximately 18% of the UBM opening. As the void formed near the entrance of the left Al trace, more current was forced to drift farther in the Al pad and entered the right-hand side of the solder bump, causing the increase in the bump resistance. The resistance increases due to the void formation measured by the four approaches are listed in Table IV. It is found that the resistance increase was only 0.12 mΩ, which is an approximately 15% increase in bump resistance. However, if approach 5 in Fig. 8 were adopted to monitor the bump resistance, the change was only 6.5%.

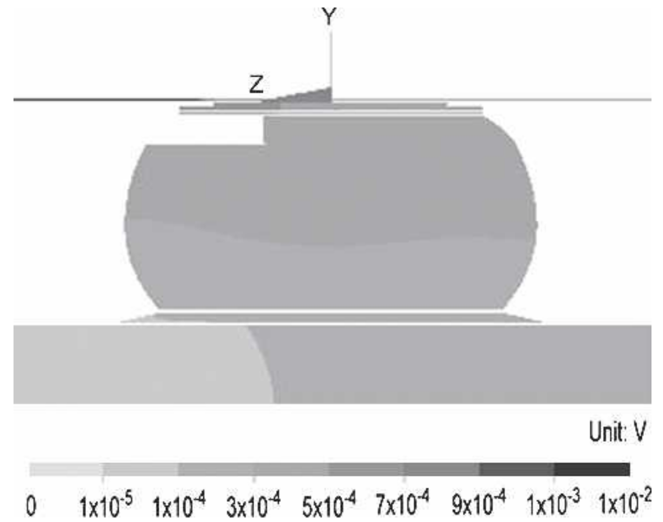


Fig. 9. The voltage distribution in the solder bump when a void depleted approximately 18% of the UBM opening.

Table IV. The Resistance Increases Due to the Void Formation Measured by the Different Approaches in this Study

Approach	R0 (mΩ)	R1 (mΩ)	R/R0 (%)
1	0.77	0.89	15.6
2	0.76	0.88	15.7
3	0.83	0.95	14.5
4	0.83	0.95	14.5
5	7.7	8.2	6.5

Therefore, approaches 1 though 4 are more sensitive to void formation.

CONCLUSION

Kelvin structures for flip-chip solder joints were designed and fabricated to measure bump resistance. The measured bump resistance strongly depended on the layout of the Kelvin bump structures. The simulation results indicated that the difference in bump resistance could be as large as 9 times when the voltage drop was measured at different positions. It is found that the serious crowding effect may be responsible for the significant geometrical effect of bump resistance in flip-chip solder joints. The simulation results indicated that approaches 1 though 4 are quite sensitive to detect the void formation, and thus, they are quite suitable for monitoring the resistance change due to void formation.

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