A Wafer-Level Hermetic Encapsulation for MEMS Manufacture Application

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Abstract—In order to simplify the processing complexity and cut down the manufacturing cost, a new wafer bonding technique using ultraviolet (UV) curable adhesive is introduced here for microelectromechanical systems (MEMS) device packaging and manufacturing applications. UV curable adhesive is cured through UV light exposure without any heating process that is suitable for the packaging of temperature-sensitive materials or devices. A Pyrex 7740 glass is chemically wet etched to form microcavities and utilized as the protection cap substrate. After a UV-curable adhesive is spin-coated onto the glass substrate, the substrate is then aligned and bonded through UV light exposure with a device substrate below. Electrical contact pad opening and die separation are done simultaneously by dicing. Two different testing devices, a dew point sensor and capacitive accelerometer, are built to evaluate the package strength and hermeticity. After the dicing process, no structural damage or stiction phenomenon is found in the packaged parallel capacitor. The acceleration test results also indicate that the package using the Loctite 3491 UV adhesive with 150 μ m bond width can survive more than 300 days at a 25 °C and 100% relative humidity working environment.

Index Terms—Acceleration tests, driven-out spin method, hermetic encapsulation, low-temperature wafer bonding, microelectromechanical systems (MEMS) manufacturing, post-process, ultraviolet (UV) adhesive, wafer-level packaging.

I. INTRODUCTION

HE characteristics of miniaturization, low power consumption, and cheap manufacturing cost have enabled microelectromechanical systems (MEMS) technology to be a manifest choice in the fabrication of next-generation sensing and actuating devices [1]–[3]. Nevertheless, it has still encountered great technical challenges while being commercialized. Most of MEMS devices usually consist of two major components which are mechanical microstructures and solid-state integrated circuits (ICs), respectively. Unlike the ICs, the micromechanical structures usually contain freestanding moving

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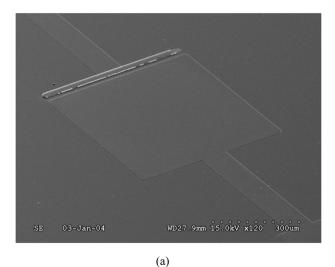
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parts which are formed after sacrificial layer removal of its underneath layer[4] and need to interact with surrounding physical environments for sensing or actuating purposes. One of the challenges is how to protect these delicate micromechanical structures well with a reasonable cost and provide windows for nonelectric signal input/outputs at the same time. The packaging development has become the most crucial issue for MEMS commercialization [4]–[10].

Meanwhile, in MEMS fabrication, the present dicing operation should be performed prior to structural release since the dicing is a wet process which could result in a stiction problem to the freestanding microstructures. The cooling water jet and particle contamination during the dicing operation could also fail the devices. For instance, a parallel capacitor is damaged after dicing, either the overhanging electrode is washed out [see Fig. 1(a)] or the electrode sticks to the bottom one [see Fig. 1(b)]. In order to prevent damages occurring during the dicing, MEMS devices are, in general, fabricated and diced on a silicon wafer first. After that, the freestanding micromechanical structures of the devices are released die by die for following die-level testing and packaging procedures. Although such a manufacturing flow can ensure every MEMS device free from the possible damages caused by the wet dicing process, high manufacturing cost is inevitable. On the other hand, these damage issues could be resolved using laser ablaze [7] instead of abrasive cutting. Time-consuming, debris redeposition, and expensive dicing equipment are still inevitable drawbacks for this solution. In this paper, a novel wafer-level hermetic encapsulation is proposed for MEMS manufacture. Through wafer-level processing, all devices on a wafer can be simultaneously fabricated, released, tested, and then packaged so the cost can be reduced. The approach can also effectively eliminate any possible damages since every device is packaged and protected prior to the final dicing operation.

Previously, several approaches have been proposed for the fabrication of a hermetic seal [11]–[14]. In these approaches, a common scheme, called post-process packaging, is also adopted in our new packaging process. The post-process packaging (see Fig. 2) means the packaging step is done after device fabrication processes, including the release of micromechanical structures, which can provide high process flexibility for various MEMS fabrications. The proposed packaging method in this paper is a combination of wafer bonding technique and microshell encapsulation. MEMS devices and protection shells are fabricated at the same time on two different wafers, silicon and glass substrates, respectively. Then these two substrates are assembled together using an appropriate "wafer bonding technique" [15] to achieve the final encapsulation of the devices. The microshell



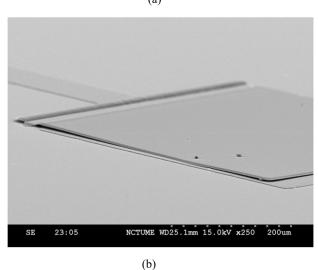


Fig. 1. Scanning electron microscopy (SEM) of the overhanging electrode of a capacitive accelerometer after dicing operation. (a) Wash-out damage by cooling water jet. (b) Structural stiction by surface tension force.

provides mechanical support, thermal path, and electrical contact for the MEMS devices.

Although several wafer bonding techniques, such as anodic, fusion, solder, epoxy glue, etc., had been developed for the packaging purpose, most of them are not suitable for packaging the devices with temperature-sensitive materials. Thus, in this paper, a wafer bonding technique using an ultraviolet (UV)-curable adhesive is introduced and characterized for the proposed hermetic encapsulation fabrication. UV-curable adhesives have been extensively used for many applications. To meet different packaging needs, numerous UV-curable adhesives have been developed in the past few years [16], [17]. For the wafer-level packaging application, Loctite product 3491 is chosen due to high bonding strength between glass and metal and low viscosity characteristic which makes it suitable for spin-coating purposes. In addition, it shows good resistance to humidity and water immersion. The key features of the UV-curable adhesive wafer bonding include low process temperature, less roughness dependence of the bonding interface, and good hermeticity to moisture. Unlike most adhesives cured by heating [14], [18]–[20], UV-curable adhesive can provide good bonding

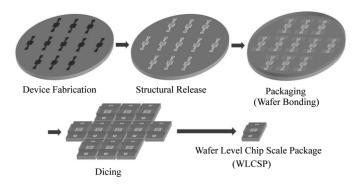


Fig. 2. Schematic diagram of wafer-level post-process packaging.

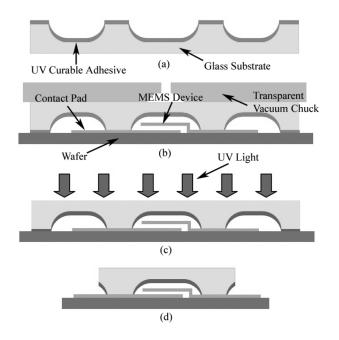
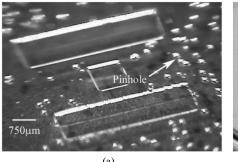


Fig. 3. Process flow of wafer-level package by using UV-curable adhesive. (a) Adhesive coating of glass. (b) Wafer alignment and contact of glass-to-silicon. (c) UV adhesive curing and bonding. (d) Die separation.

strength for the assembly of silicon and glass substrates under UV light exposure with correct wavelength and dosage at room temperature. Since the curing process can be shortened by increasing UV light intensity, low packaging cost with high throughput can be expected.

II. PACKAGING DESIGN AND FABRICATION

Our packaging scheme is to employ UV-curable adhesive bond for hermetic encapsulation of on-wafer MEMS devices. Via the adhesive, a micromachined glass substrate can be tightly bonded with the device substrate at room temperature. Fig. 3 shows the process flow of the packaging. It begins with UV-curable adhesive coating onto a glass substrate which has been chemically etched to form 55-µm-deep concave microcavities for the accommodation of as-fabricated devices and related electrical contacts. Then, the glass substrate is placed and fixed on a homemade bonding tool for following optical alignment and mechanical contact with device substrate of its underside. A flood exposure of UV light is subsequently performed onto the two tentatively adhered substrates for adhesive curing. Finally,



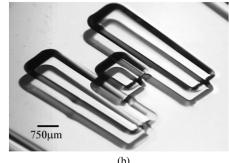


Fig. 4. Optical micrographs of on-glass micromachined cavities. (a) Without photoresist protection. (b) With photoresist protection.

a hermetically sealed MEMS device with accessible electrical contacts is completed after the dicing operation.

A. Micromachined Glass Substrate With Protection Caps

A Corning Pyrex 7740 glass wafer is chosen and micromachined to form protection caps of MEMS devices because it is mechanically robust, transparent to UV light, and shows good resistance to most chemicals. In addition, the 7740 glass has similar coefficient of thermal expansion (CTE) to silicon wafer so that it has better thermal reliability in the bonding interface due to minute thermal stress formation induced by environmental temperature variation. The concave structures inside the protection caps are chemically wet etched using hydrofluoric acid with a hard mask and backside protection which are 40/150-nm-thick Cr/Au film and waterproof tape, respectively. Additional photoresist is then spin-coated on top of the Cr/Au and photo-defined through backside exposure. The optical micrographs of the micromachined glass caps with and without PR protection after being etched are juxtaposed in Fig. 4. Because, in the hard mask deposition, the impurities in a sputter chamber will cause defects on the sputtered film, serious pinhole phenomenon occurs in the HF etching process as shown in Fig. 4(a). The defects will result in local bonding failure and make the package unreliable. Hence, a 12- μ m-thick AZ4620 photoresist patterned using backside exposure is utilized to fully cover the hard mask in the experiment. It has been found that the pinhole can be effectively diminished during HF wet etching, as shown in Fig. 4(b).

In order to expose the area of electric contact pads for later wire bonding and device testing, the glass over the pads is removed in terms of double cuts which are called separation and die cuts, respectively, as shown in Fig. 5. The concave design in the area of the contact pads is to provide a relative height difference between the contact pad and the inner surface of the glass. After two different cuts designed with different height of the dicing blade, glass removal can be achieved. It is noted that the bonding strength in the package design must be strong enough to sustain the abrasive force between the substrates and the dicing blade.

B. Packaging Monitoring Devices

In the experiment, two different kinds of testing devices, a one-axial capacitive accelerometer and a dew point sensor,

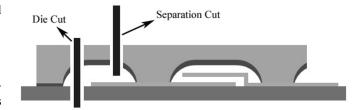


Fig. 5. Two-step dicing strategy.

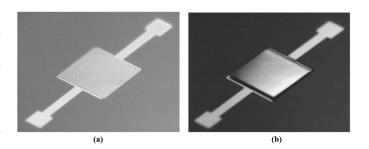


Fig. 6. Optical micrographs of two testing devices. (a) Dew point sensor. (b) Capacitive accelerometer.

are fabricated for packaging hermeticity and strength evaluations, respectively. The accelerometer is utilized to mimic a freestanding MEMS device. Via the observation of mechanical damage or stiction phenomenon, the package can be examined whether it can provide desirable protection to MEMS devices during dicing operation. Regarding the hermeticity test of the package, the dew point sensor is utilized to monitor capacitance change due to the effective dielectric constant increase from $\varepsilon_r = 1$ at air to $\varepsilon_r = 80$ at water once the moisture penetrates through the bonding width and condenses within the sensing electrodes. Fig. 6 shows the optical micrographs of two fabricated monitoring devices. The interdigited finger design of the dew point sensor shown in Fig. 6(a) is aimed for high moisture sensitivity in terms of having larger sensing area. 2- μ m thick, 560- μ m long, and 5- μ m spacing of aluminum electrode design makes the sensor have 5.7-pF capacitance. The capacitive accelerometer is deigned with two overlapping aluminum electrodes, which are a 3- μ m-thick upper electrode and a 1- μ m-thick lower electrode, as shown in Fig. 6(b). The upper electrode is over hanged on top of the other electrode with 5- μ m spacing.

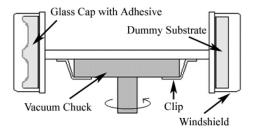


Fig. 7. Setup diagram of "driven-out spin."

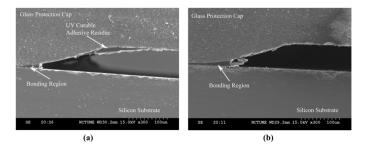


Fig. 8. Cross-sectional views of two bonded glass cap/MEMS substrates. (a) Without using "driven-out spin" technique. (b) Using "driven-out spin" technique.

C. UV-Curable Adhesive Coating and Driven-Out Spin Method

During the experiment, an UV-curable adhesive is spin-coated on the protection cap substrate. Spin coating is chosen instead of stamping mainly due to the consideration of uniformity control. However, it occurs that there is residual adhesive inside the cavities after the coating, which may fail interior devices. Thus, a "driven-out spin" method is developed to minimize the adhesive residue in the cavities after spin coating. By taking the advantage of centrifugal force during spin coating, the adhesive will reflow toward the bonding region, which can effectively reduce the amount of the adhesive residue originally trapped inside the cavities. Fig. 7 shows the setup of "driven-out spin." An additional windshield is used to avoid wind perturbation during high-speed rotation.

Fig. 8 shows the cross-sectional SEM views of the coated microcavities using two different spin coating strategies. Without the additional "driven-out spin," adhesive residue remains in the cap corner, as shown in Fig. 8(a), that may affect the working space designed for the devices. Additional concave depth or size is needed. In contrast, with additional "driven- out spin," the adhesive residue will leave the corner site and reflow toward the bonding region, as shown in Fig. 8(b). The possible damage to freestanding devices during the following bonding processes can be prevented.

D. Wafer-Level Bonding

In the bonding experiment, soft baking cannot be performed onto the employed UV-curable adhesive before UV light exposure, since it is still in a sticky status after spin-coated on the glass cap substrate, which is not suitable for the following alignment process. A conventional wafer-bonding tool based on the contact/separation/alignment three-steps operation is therefore not applicable to our packaging approach. A bonding tool using two-step alignment with alignment pins is then designed and

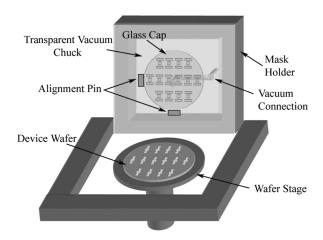


Fig. 9. Schematic diagram of the wafer bonding setup.

developed for our bonding purpose, as shown in Fig. 9. This design concept is adaptable to any conventional contact aligner. A transparent vacuum chuck is built and fixed on the mask holder of the UV lithography system. The glass cap substrate is first vacuum fixed on the chuck, positioned by the alignment pins, then aligned with device substrate of its underside by proximity contact. After UV-curable adhesive is spin-coated, the glass cap is fixed again at the same position and another finer alignment is performed. The wafer holder stage is then raised up to bond with the glass cap substrate together temporarily. Finally, the glass cap bonded with the device wafer is transferred under a mercury lamp for flood exposure to cure the adhesive. The suggested curing conditions are 365-nm UV light with the intensity of 36–38 mw/cm² or 425-nm UV light with the intensity of 45-m mw/cm². Total exposure time is about 3 h for the bonding process, which can be further reduced via the increase of light intensity.

III. RESULTS AND PACKAGING RELIABILITY

The glass/silicon wafer level bonding results are shown in Fig. 10. Fig. 10(a) shows a 4-in MEMS device substrate bonded with a micromachined glass wafer. As shown in the figure, there is an area with different contrast which indicates the occurrence of incomplete bond. The local bonding failure around the center region of the wafer is mainly due to air entrapment caused by the rim region contact of the two substrates prior to the center region one. Fig. 10(b) shows an enlarged view of the defect area in which protection caps were washed out by cooling water jet during wafer dicing. However, the problem can be solved using a vacuum environment for the bonding. Fig. 11 shows a packaged capacitive accelerometer after the dicing operation. The glasses over electrical contact pads are successfully removed by the double cuts method. No damage is found in these pads. In order to further verify that there is no stiction or structural damage happening after the dicing operation, the glass protection cap is removed carefully by cutting nipper and examining under SEM. None of the phenomena are observed in the device as shown in Fig. 12. The results show the package strength is strong enough to withstand the dicing operation. Moreover, none of mechanical damages is found on the bonding surface of the silicon substrate after the glass protection cap removal.

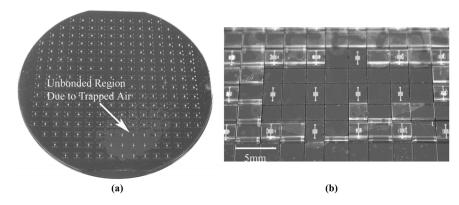


Fig. 10. Wafer bonding results. (a) 4-in glass/silicon bonded wafer. (b) Enlarged view of air trapping area after dicing operation.

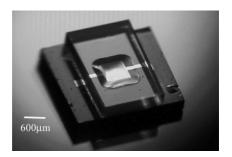


Fig. 11. Packaged capacitive accelerometer.

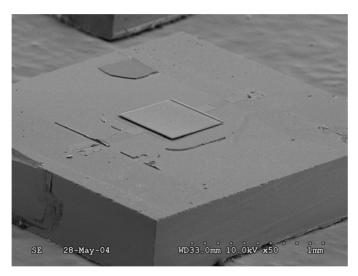


Fig. 12. No stiction or structural damage is observed after decaping.

It indicates that the bonding strength is less than the fracture strength of silicon.

Package lifetime is characterized by measuring capacitance change of the encapsulated dew point sensor while it is immersed in a hot water bath, the so-called acceleration test. Because the electrical contacts of the sensor are seriously oxidized during the testing as shown in Fig. 13, capacitance measurement cannot proceede even though no moisture penetration is observed. Thus, package failure is then determined based on the observation under optical microscope instead of capacitance measurement, as shown in Fig. 14. When dew is found in the sensing electrodes of the packaged sensor, the lifetime of package can be determined. Ten dies with the bonding

widths, $149 \pm 5 \mu m$, are first prescreened with no detectable

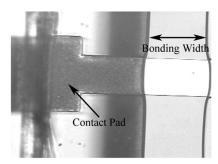


Fig. 13. Optical micrograph of tested device after acceleration test; the contact pad has been oxidized during the test.

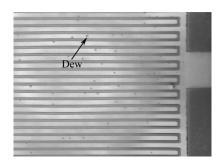


Fig. 14. Optical micrograph of the interdigited dew point sensor with moisture condensation while the package is failed.

defects and then divided into two different testing conditions. One group is put into 70 °C water and the other is at 60 °C. The packages are examined under a microscope for the observation of water vapor condensation. Since no observable damages, such as the interface detachment and strength decrease of the bonding, are found in the failed packages except the moisture condensation phenomenon, the failure mechanism of the packages can be attributed to the vapor diffusion. The package lifetime at room temperature and 100%RH environment is roughly estimated based on the diffusion mechanism using the following Arhennius equation [21]:

$$t = C \exp\left(\frac{Q}{RT}\right) \tag{1}$$

where t is the time to failure, T is temperature, Q is activation energy, and R is gas constant. The estimated lifetime is about 305 days under 25 °C, and 100% R.H. working conditions, as shown in Fig. 15.

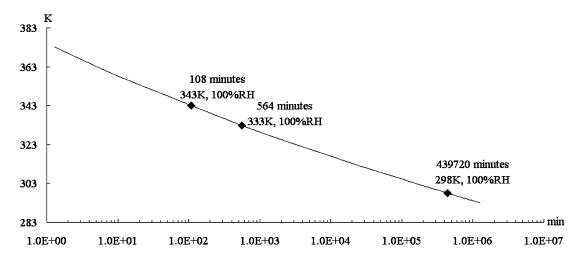


Fig. 15. Package lifetime versus testing temperature.

This paper is the first to present a wafer-level hermetic encapsulation using UV adhesive. Although the technique can provide a zero level protection to a MEMS device and its electrical contacts to outside environment simultaneously, the technique could also block the ways of MEMS structures to the outside for sensing and actuating purposes. Since the contact windows must be opened later, it will lessen the advantages using the wafer-level processing. The problem has been solved recently via the creation of tiny channel structures which can effectively prevent the water jet penetration [22]. In addition, the bonding width is controlled by the contact pressure and the thickness of spin-coated UV adhesive, the bonding strength depends on the choice of adhesive, and the accuracy of package lifetime requires more dies to test. Further characterizations are required since these parameters are very important for future applications of the packaging technique.

IV. CONCLUSION

A low-temperature wafer-level MEMS hermetic encapsulation is achieved using UV-curable adhesive. The bonding strength is adequate to sustain following wet dicing operation and protect freestanding MEMS devices from stiction and damages. To reduce the adhesive residue inside the glass cap, a "drive out spin" technique is developed to increase packaging reliability. The acceleration test shows that the hermetic package with 150-µm-wide adhesive bond width can withstand moisture penetration for 305 days while it is operated at 25 °C and 100% RH environment. Such a low-cost and post-process packaging method provides an alternative choice for MEMS and microelectronics device manufacture applications.

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REFERENCES

- R. R. Minor and D. W. Rowe, "Utilization of GPS/MEMS-IMU for measurement of dynamics for range testing of missiles and rockets," in *Proc. IEEE Position Location Navigation Symp.*, Apr. 20–23, 1998, pp. 602–607.
- [2] S. Kamisuki, T. Hagata, C. Tezuka, Y. Nose, M. Fujii, and M. Atobe, "A low power small, electrostatically-driven commercial ink jet head," in *Proc. IEEE 11th Microelectromech. Syst.*, Jan. 1998, pp. 63–68.
- [3] K. Ikuta, S. Maruo, Y. Fukaya, and T. Fujisawa, "Biochemical IC chip toward cell free DNA protein synthesis," in *Proc. IEEE 11th Microelec-tromechanical Syst.*, Jan. 1998, pp. 131–136.
- [4] C. B. O'Neal, A. P. Malshe, S. B. Singh, W. D. Brown, and W. P. Eaton, "Challenges in the packaging of mems," in *Proc. Int. Symp. Adv. Packag. Mater.: Processes, Properties, Interfaces*, Mar. 14–17, 1999, pp. 41–47.
- [5] T. R. Hsu, "Packaging design of microsystems and meso-scale devices," IEEE Trans. Adv. Packag., vol. 23, no. 4, pp. 596–601, Dec. 2000.
- [6] C. Linder, C. L. Paratte, M.-a. Grétillat, V. P. Jaecklin, and N. F. de Rooji, "Surface micromachining," *J. Micromech. Microeng.*, vol. 2, no. 3, pp. 122–132, 1992.
- [7] T. Lizotte, "Laser dicing of chip scale and silicon wafer scale packages," in *IEEE/CPMT/SEMI 28th Int. Electron. Manuf. Technol. Symp.*, Jul. 16–18, 2003, pp. 1–5.
- [8] S. A. Audet and K. M. Edenfeld, "Integrated sensor wafer-level pack-aging," in *Proc. IEEE Int. Conf. Solid State Sens. Actuators*, vol. 1, Chicago, IL, Jun. 16–19, 1997, pp. 287–289.
- [9] D. Ando, K. Oishi, K. T. Nakamura, and S. Umeda, "Glass direct bonding technology for hermetic seal package," in *IEEE Proc. 10th Microelectromech. Syst.*, Jan. 1997, pp. 186–190.
- [10] Y. T. Cheng, W.-T. Hsu, K. Najafi, C. T.-C. Nguyen, and L. Lin, "Vacuum packaging technology using localized aluminum/silicon-to-glass bonding," in *Proc. IEEE/ASME J. Microelectromech.* Syst., vol. 11, 2002, pp. 556–565.
- [11] H. A. C. Tilmans, D. J. van de Peer, and E. Beyne, "The indent reflow sealing (IRS) technique-a method for the fabrication of sealed cavities for mems devices," *IEEE/ASME J. Microelectromech. Syst.*, vol. 9, no. 2, pp. 206–217, Jun. 2000.
- [12] A. V. Chavan and K. D. Wise, "A monolithic fully-integrated vacuum-sealed CMOS pressure sensor," *IEEE Trans. Electron Devices*, vol. 49, no. 1, pp. 164–169, Jan. 2002.
- [13] Y. T. Cheng, L. Lin, and K. Najafi, "Localized silicon fusion and eutectic bonding for MEMS fabrication and packaging," in *Proc. IEEE/ASME J. Microelectromech. Syst.*, vol. 9, 2000, pp. 3–8.
- [14] Y. Awatani, Y. Matsumoto, and K. Kato, "Damage free dicing method for mems devices," in *Proc. IEEE/LEOS Int. Conf. Opt. MEMs*, Aug. 2002, pp. 137–138.
- [15] A. Hanneborg, "Silicon wafer bonding techniques for assembly of micromechanical elements," in *IEEE Proc. 4th Microelectromech. Syst.*, Jan.–Feb. 1991, pp. 92–98.
- [16] M. A. Uddin, H. P. Chan, K. W. Lam, Y. C. Chan, P. L. Chu, K. C. Hung, and T. O. Tsun, "Delamination problems of UV-cured adhesive bonded optical fiber in V-groove for photonic packaging," *IEEE Photon. Technol. Lett.*, vol. 16, no. 4, pp. 1113–1115, Apr. 2004.

- [17] H. Murray and T. Ledwidge, "UV cationic systems for smart card/tag applications," in *Proc. IEEE 1st Int. Conf. Polymers Adhesives Microelectron. Photon.*, Oct. 2001, pp. 309–313.
- [18] J. Oberhammer, F. Niklaus, and G. Stemme, "Selective wafer-level adhesive bonding with benzocyclobutene for fabrication of cavitites," Sens. Actuators A, vol. 105, pp. 297–304, 2003.
- [19] A. Jourdain, P. De Moor, S. Pamidighantam, and H. A. C. Tilmans, "Investigation of the hermeticity of BCB-sealed cavities for housing RF-MEMS devices," in *IEEE Proc. 15th Microelectromech. Syst.*, Jan. 2002, pp. 677–680.
- [20] A. Han, K. W. Oh, S. Bhansali, H. Thurman, and C. H. Ahn, "A low-temperature biochemically compatible bonding technique using fluoropolymers for biochemical microfluidic systems," in *IEEE Proc. 13th Microelectromech. Syst.*, Jan. 2000, pp. 414–418.
- [21] R. R. Tummala, E. J. Rymaszewski, and A. G. Kolpfenstein, Microelectronics Packaging Handbook. New York: Chapman & Hall, 1997.
- [22] P. Chang-Chien and K. D. Wise, "A barometric pressure sensor with integrated vacuum reference control using localized CVD," in *North Amer. Solid-State Sens.*, *Actuators, Microsyst. Workshop*, Hilton Head, SC, Jun. 2002, pp. 90–93.



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