Hafnium Silicate Nanocrystal Memory Using Sol–Gel-Spin-Coating Method

Hsin-Chiang You, Tze-Hsiang Hsu, Fu-Hsiang Ko, Jiang-Wen Huang, and Tan-Fu Lei

***Abstract*—The authors fabricate the hafnium silicate nanocrystal memory for the first time using a very simple sol–gel-spin-coating method and 900 °C 1-min rapid thermal annealing (RTA). From the TEM identification, the nanocrystals are formed as the charge trapping layer after 900 °C 1-min RTA and the size is about 5 nm. They demonstrate the composition of nanocrystal is hafnium silicate from the X-ray-photoelectron-spectroscopy analysis. They verify the electric properties in terms of program/erase (P/E) speed, charge retention, and endurance. The sol–gel device exhibits the long charge retention time of 10^4 s with only 6% charge loss, and good endurance performance for P/E cycles up to 10^5.**

***Index Terms*—Charge retention, endurance, hafnium silicate, nanocrystal memory, sol–gel spin coating.**

I. Introduction

THE DEMAND for high-density low-cost low-power consumption and fast program/erase (P/E) speed semiconductor memory will lead the current baseline memory technologies to several revolutionary and evolutionary approaches such as silicon–oxide–nitride–oxide-silicon (SONOS) high-κ memory and nanocrystal memory. But SONOS high-κ memory has the electron migration problem in the charge trapping layer [1], which will cause the charge loss and degrade the charge retention performance. The nanocrystal memory can keep the trapped charge tightly to avoid the charge loss problem of SONOS memory and also achieve the advantages like: fast P/E speed, low programming voltage, and good endurance as SONOS memory [2]–[4]. In this letter, we propose a novel technique for the first time to form the hafnium silicate $(HfSiO_x)$ nanocrystals in the charge trapping layer of the memory. We use a sol–gel-spin-coating method [5] to deposit the high-κ charge trapping layer on the tunneling oxide of the memory device followed by 900 °C 1-min rapid thermal annealing (RTA) to form nanocrystals in the charge trapping layer. The film formation with the sol–gel spin coating is a simple method in comparison with atomic layer deposition, physical vapor deposition (PVD), or chemical vapor deposition (CVD). Our proposed technique features the cheaper sol–gel materials and very simple fabrication tool than PVD technique [6], [7]. In addition, the film can be fabricated in the normal pressure system instead of high-vacuum system [8].

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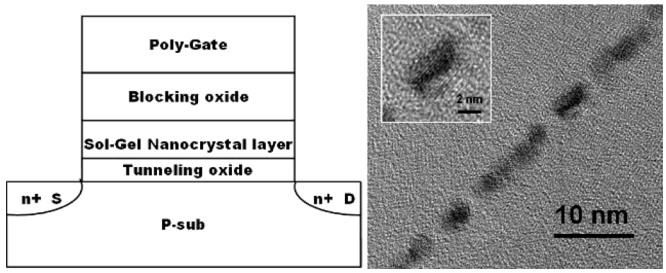

Fig. 1. Device structure for the sol–gel hafnium silicate nanocrystal memory and cross-sectional HRTEM of the nanocrystals.

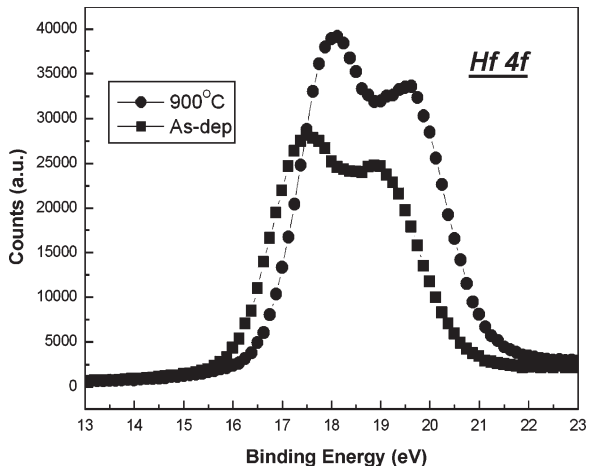

Fig. 2. XPS spectra of as-deposited and 900 °C RTA hafnium silicate films.

II. Experimental

The fabrication of the sol–gel-spin-coating nanocrystal memory is started with local-oxidation of silicon (LOCOS) isolation process on p-type (100) 150-mm silicon substrate. At the beginning, a 4-nm tunneling oxide was thermally grown at 925 °C by furnace. The charge trapping layer was prepared using the sol–gel-spin-coating method. $HfCl_4$ (99.5%, Aldrich, USA) and $SiCl_4$ (99.5%, Aldrich) were used as the precursors. The donation of hafnium and silicon can form the hafnium silicate after a suitable RTA. Initially, we prepared a solution which the molar ratio of $HfCl_4$:$SiCl_4$:isopropanol is 1:1:1000. The charge trapping layer was deposited by spin coating at 3000 r/min for 60 s at ambient temperature (25 °C). The spin-coater used was TEL Clean Track Model-MK8 (Japan). After spin coating, the wafer was under RTA at 900 °C for 60 s in O_2 ambient to form hafnium silicate $(HfSiO_x)$ nanocrystals. The blocking oxide 30 nm was deposited by HDPCVD TEOS followed by poly-Si gate 200-nm deposition. Finally,

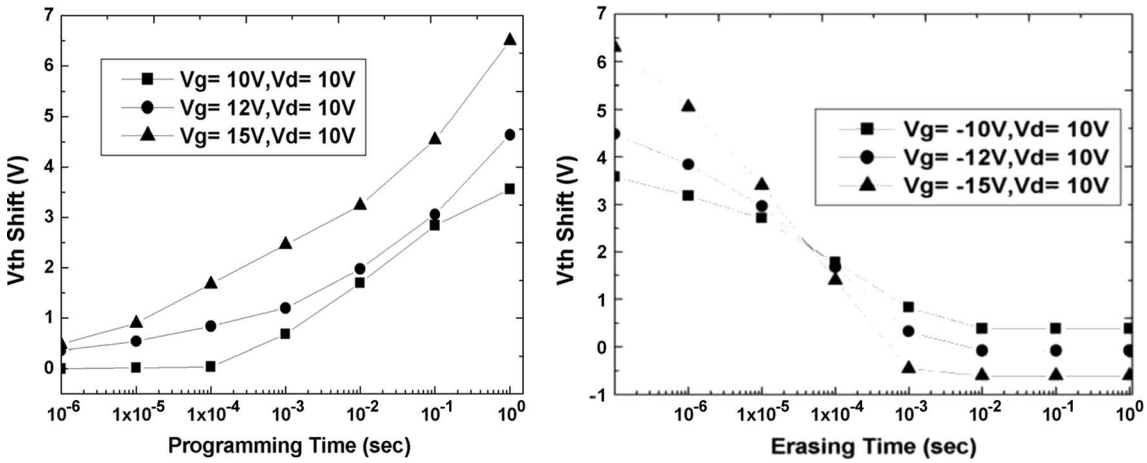

Fig. 3. P/E speed curve of the sol–gel hafnium silicate nanocrystal memory.

gate patterning, source/drain (S/D) implant, and the rest of the subsequent CMOS processes were used to fabricate this nanocrystal memory. Fig. 1 shows the structure of the fabricated nanocrystal device.

III. Results and Discussion

The high-resolution transmission electron microscopy (HRTEM) image in Fig. 1 depicts the nanocrystal on SiO_2 film after annealing at 900 °C for 60 s. The average nanocrystal size is around 5 nm. The clearly visible lattice fringes denote crystallization into a well-ordered nanostructure. Chemical characterization of the $HfSi_xO_y$ film was accomplished by X-ray photoelectron spectroscopy (XPS) in Fig. 2. The literature [9] also suggests the similar Hf 4f peaks for the hafnium silicate film. Specifically, as the film is heated, the shift from 17.4 eV (as-dep) to 18.0 eV (900 °C annealing) and the enlargement of peak height are observed. Cho *et al.* [10] reports the peak shift to higher binding energy for $HfSi_xO_y$ and can be caused by the formation of Hf–O bonding in the vicinity of Si. Thus, these relationships of bonding between Hf–O and Hf–Si suggest that Hf and Si atoms are bonded to O atoms as nearest neighbors. Wilk *et al.* [11] and Kirsch *et al.* [12] also observe a similar behavior and they attribute to the increased hafnium silicate formation.

Fig. 3 shows the program speed of the hafnium silicate nanocrystal memory. We use channel hot electron (CHE) to program, and the program conditions are 1) $V_g = 10$ V, $V_d = 10$ V; 2) $V_g = 12$ V, $V_d = 10$ V; and 3) $V_g = 15$ V, $V_d = 10$ V, respectively. The Vth shift increases as increasing the applied gate voltage, and the program speed can be as fast as 10 μs with 1-V memory window for program condition $V_g = 15$ V, $V_d = 10$ V. The erase speed of the hafnium silicate nanocrystal memory is also demonstrated in Fig. 3. We use band-to-band hot hole (BTBHH) to erase, and the erase conditions are 1) $V_g = -10$ V, $V_d = 10$ V; 2) $V_g = -12$ V, $V_d = 10$ V; and 3) $V_g = -15$ V, $V_d = 10$ V, respectively. As the gate voltage becomes more negative, the erase effect becomes much fast. The three curves with various erase conditions intercross within the region of 10^{-5} and 10^{-4} s. This observation is attributed to the property of better erase ability at the much more negative gate voltage.

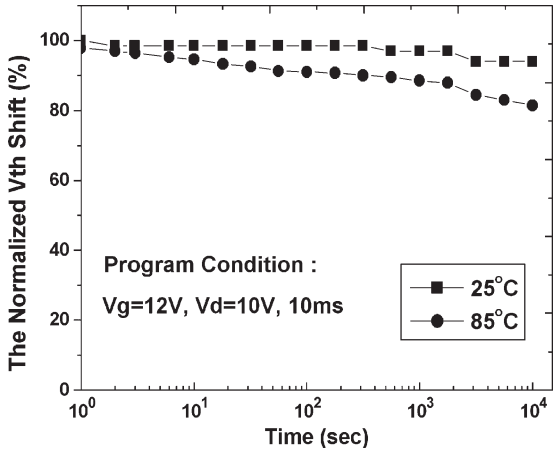

Fig. 4. Charge retention curve of sol–gel hafnium silicate nanocrystal memory at room temperature and 85 °C, respectively.

We also observed somewhat overerase (< 0.5 V) occurred at $V_g = -15$ V. Muralidhar *et al.* [13] has been observed the overerase effect for CVD silicon nanocrystal memory. However, the overerase less than 0.5 V is acceptable for our sol–gel hafnium silicate nanocrystal memory. Our device has better speed at 10 μs for program condition of $V_g = 15$ V, $V_d = 10$ V and at 1 ms for erase condition of $V_g = -12$ V, $V_d = 10$ V.

The charge retention characteristic of the sol–gel hafnium silicate nanocrystal memory is demonstrated in Fig. 4. The normalized Vth shift is defined as the ratio of Vth shift at the time of interest and at the beginning. Using this as an indicator, we can see the charge loss for the nanocrystal memory. The curve is obtained in program condition of $V_g = 12$ V and $V_d = 10$ V with 10 ms under the room temperature and 85 °C, respectively. The room temperature retention curve shows only 6% charge loss as measure time up to 10^4 s. The 85 °C curve exhibits $\sim$ 20% charge loss. This result indicates the hafnium silicate nanocrystals in the charge trapping layer can tightly catch the tunneling electrons. Hence, the trapped electrons by the sol–gel-derived nanocrystal devices are not easily to escape, and the exhibited charge loss percentage is quite low. Fig. 5 shows the endurance characteristics of the nanocrystal memory. The measurement condition is program $V_g = 15$ V and

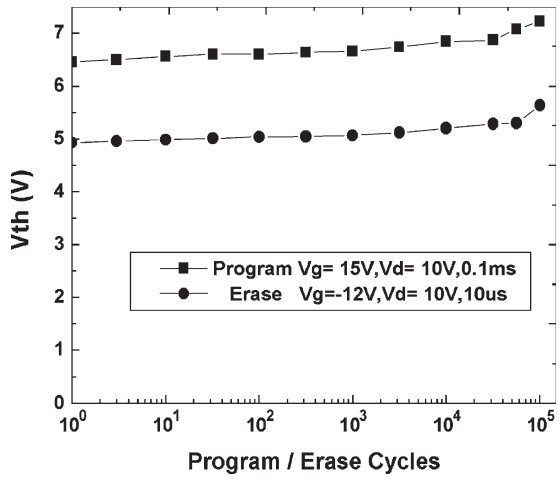

Fig. 5. Endurance characteristic of sol–gel hafnium silicate nanocrystal memory.

$V_d = 10$ V under 0.1 ms, and erase $V_g = -12$ V and $V_d = 10$ V under 10 μs. As the figure shows, the memory window is about 1.3–1.5 V after 10^5 P/E cycles. No significant window narrowing is observed. The Vth increase in the later stage of endurance is due to some electrons left in the hafnium silicate nanocrystals after erasing. This can be explained by the electrons are trapped in the nanocrystals tightly and hard to escape by BTBHH erase. This observation suggests the retention characteristics of our devices still behave well. Although the Vth shift varies more than 0.5 V, the Vth shift is still less than 0.7 V and the memory can still operate in normal condition. This observation verifies the reliability of our hafnium silicate nanocrystal memory. The proposed simple the sol–gel-spin-coating process exhibits the potential to be incorporated into the future nanocrystal memory fabrication processes.

IV. Conclusion

In this letter, we propose a new the sol–gel-spin-coating method to form nanocrystals as the charge trapping layer of SONOS memory. The TEM and XPS analysis indicates the formation of $\sim$ 5-nm hafnium silicate nanocrystals. We have verified the device performance with the P/E speed, charge retention, and endurance. The quality of the nanocrystals formed by the sol–gel-spin-coating method and RTA treatment exhibits better properties in terms of fast P/E speed (10 μs/1 ms), long charge retention time (6% loss at 10^4 s), and good endurance (up to 10^5 P/E cycles) with no memory window narrowing.

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