Correlating Drain–Current With Strain-Induced Mobility in Nanoscale Strained CMOSFETs

Hong-Nien Lin, Hung-Wei Chen, Chih-Hsin Ko, Chung-Hu Ge, Horng-Chih Lin, *Senior Member, IEEE*, Tiao-Yuan Huang, *Fellow, IEEE*, and Wen-Chin Lee, *Member, IEEE*

***Abstract*—The correlation between channel mobility gain ($\Delta\mu$), linear drain–current gain ($\Delta I_{\rm dlin}$), and saturation drain–current gain ($\Delta I_{\rm dsat}$) of nanoscale strained CMOSFETs are reported. From the plots of $\Delta I_{\rm dlin}$ versus $\Delta I_{\rm dsat}$ and ballistic efficiency ($B_{\rm sat,PSS}$), the ratio of source/drain parasitic resistance ($R_{\rm SD,PSS}$) to channel resistance ($R_{\rm CH,PSS}$) of strained CMOSFETs can be extracted. By plotting $\Delta\mu$ versus $\Delta I_{\rm dlin}$, the efficiency of $\Delta\mu$ translated to $\Delta I_{\rm dlin}$ is higher for strained pMOSFETs than strained nMOSFETs due to smaller $R_{\rm SD,PSS}$-to-$R_{\rm CH,PSS}$ ratio of strained pMOSFETs. It suggests that to exploit strain benefits fully, the $R_{\rm SD,PSS}$ reduction for strained nMOSFETs is vital, while for strained pMOSFETs the $\Delta I_{\rm dlin}$-to-$\Delta\mu$ sensitivity is maintained until $R_{\rm SD,PSS}$ becomes comparable to/or higher than $R_{\rm CH,PSS}$.**

***Index Terms*—CMOSFETs, current, mobility, strain.**

I. Introduction

PRESENTLY, uniaxial strain engineering has become one of mainstream techniques to enhance the performance of nanoscale CMOSFETs. Strain-enhanced channel mobility and drain–current are considered as important performance indexes for evaluating the feasibility of a strain technique. However, as the gate length dramatically shrinks into nanoscale regime, strain-induced enhancement becomes more complicated to predict as the carrier ballistic transport, and source/drain (S/D) parasitic resistance effects start to prevail for state-of-the-art CMOS technologies [1]–[3]. It has been reported that, as compared with saturation drain–current ($I_{\rm dsat}$), linear drain–current ($I_{\rm dlin}$) is more sensitive to channel mobility (μ) [1]. With the S/D parasitic resistance ($R_{\rm SD}$) playing a more and more important role in the total resistance due to the drastic reduction of strain-induced channel resistance [2], the strain-induced performance enhancement will be ultimately limited. In addition, the drain–current gain is found to be affected by ballistic efficiency ($B_{\rm sat,PSS}$), which becomes more evident in sub-100-nm regime [3]. Therefore, in order to take full advantage of strain engineering in nanoscale strained CMOSFETs, it is essential to clarify the correlation between the μ, $I_{\rm dlin}$, $I_{\rm dsat}$, and the significance of $R_{\rm SD}$ and $B_{\rm sat,PSS}$.

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H.-N Lin, H.-C. Lin, and T.-Y. Huang are with the Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: hnlin.ee89g@nctu.edu.tw).

H.-W. Chen, C.-H. Ko, C.-H. Ge, and W.-C. Lee are with the Taiwan Semiconductor Manufacturing Company Ltd., Hsinchu 300, Taiwan, R.O.C.

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TABLE I
SUMMARY OF DEDUCED EQUATIONS CORRELATING THE CHANNEL MOBILITY GAIN ($\Delta\mu$), LINEAR DRAIN–CURRENT GAIN ($\Delta I_{\rm dlin}$), AND SATURATION DRAIN–CURRENT GAIN ($\Delta I_{\rm dsat}$) FOR STRAINED MOSFETS

$R_{\rm TOTAL}$ & $I_{\rm dlin}$ [2]

$$R_{\rm TOTAL} = V_{\rm D}/I_{\rm dlin} = R_{\rm CH} + R_{\rm SD} \quad \cdots (1a)$$

$$I_{\rm dlin} = W\mu Q_{\rm inv}(V_{\rm D} - I_{\rm dlin}R_{\rm SD})/L = (V_{\rm D} - I_{\rm dlin}R_{\rm SD})/R_{\rm CH} \quad \cdots (1b)$$

$\Delta I_{\rm dlin}$ vs. $\Delta\mu$, from (1a) & (1b)

$$\Delta I_{\rm dlin} = \frac{\Delta\mu}{1 + R_{\rm SD,PSS}/R_{\rm CH,PSS}}\left(1 + \frac{R_{\rm SD} - R_{\rm SD,PSS}}{R_{\rm CH} - R_{\rm CH,PSS}}\right)$$

$$= \frac{\Delta\mu}{1 + R_{\rm SD,PSS}/R_{\rm CH,PSS}} + \frac{(R_{\rm SD,PSS}/R_{\rm CH,PSS})\Delta R_{\rm SD}}{1 + R_{\rm SD,PSS}/R_{\rm CH,PSS}} \quad \cdots (2a)$$

$$= \frac{R_{\rm CH,PSS}}{R_{\rm TOTAL,PSS}}\Delta\mu + \frac{R_{\rm SD,PSS}}{R_{\rm TOTAL,PSS}}\Delta R_{\rm SD} \quad \cdots (2a')$$

where $\Delta R_{\rm SD} = (R_{\rm SD} - R_{\rm SD,PSS})/R_{\rm SD,PSS}$

$\Delta I_{\rm dsat}$ vs. $\Delta\mu$, adapted from [5]

$$\Delta I_{\rm dsat} = (1 - B_{\rm sat,PSS})\Delta\mu + k\Delta R_{\rm SD} \quad \cdots (2b)$$

k : constant, ≤ 1

$\Delta I_{\rm dlin}$ vs. $\Delta I_{\rm dsat}$, from (2a) & (2b)

$$\Delta I_{\rm dlin} = \frac{\Delta I_{\rm dsat}}{\left(1 + \frac{R_{\rm SD,PSS}}{R_{\rm CH,PSS}}\right)(1 - B_{\rm sat,PSS})} + \frac{\frac{R_{\rm SD,PSS}}{R_{\rm CH,PSS}}(1 - B_{\rm sat,PSS}) - k}{\left(1 + \frac{R_{\rm SD,PSS}}{R_{\rm CH,PSS}}\right)(1 - B_{\rm sat,PSS})}\Delta R_{\rm SD} \quad \cdots (3)$$

W, L & $Q_{\rm inv}$: gate width, gate length, and inversion charge density
$R_{\rm TOTAL}$, $R_{\rm CH}$ & $R_{\rm SD}$: total, channel, and source/drain parasitic resistance
$B_{\rm sat}$: ballistic efficiency
The subscript "PSS" denotes strained MOSFETs.

In this letter, we propose the correlation between channel mobility gain ($\Delta\mu$), linear drain–current gain ($\Delta I_{\rm dlin}$), and saturation drain–current gain ($\Delta I_{\rm dsat}$) in terms of the ratio of S/D parasitic resistance to channel resistance and ballistic efficiency, and examine the validity of this correlation with experimental results of state-of-the-art strained CMOSFETs.

II. Methodology

Process-strained Si (PSS) CMOSFETs [4] were employed to study the correlation between $\Delta\mu$, $\Delta I_{\rm dlin}$, and $\Delta I_{\rm dsat}$. In Table I, (1a) and (1b) express the total resistance ($R_{\rm TOTAL}$) composed of the channel resistance ($R_{\rm CH}$) and the S/D parasitic resistance ($R_{\rm SD}$, extrinsic to the channel), and $I_{\rm dlin}$ with $R_{\rm SD}$ correction [2], whereas $\Delta I_{\rm dlin}$ and $\Delta I_{\rm dsat}$ of

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PSS CMOSFETs are expressed in (2a) and (2b) as a function of $\Delta\mu$, the ballistic efficiency ($B_{\rm sat,PSS}$), $R_{\rm CH,PSS}$, $R_{\rm SD,PSS}$, and $\Delta R_{\rm SD}$, where $\Delta I_{\rm dlin}$, $\Delta I_{\rm dsat}$, $\Delta\mu$, and $\Delta R_{\rm SD}$ are defined as $\Delta I_{\rm dlin} = (I_{\rm dlin,PSS} - I_{\rm dlin})/I_{\rm dlin}$, $\Delta I_{\rm dsat} = (I_{\rm dsat,PSS} - I_{\rm dsat})/I_{\rm dsat}$, $\Delta\mu = (\mu_{\rm PSS} - \mu)/\mu$, and $\Delta R_{\rm SD} = (R_{\rm SD} - R_{\rm SD,PSS})/R_{\rm SD,PSS}$, respectively. Then, assuming the same gate length (L), gate width (W), and inversion charge density ($Q_{\rm inv}$) for the control and PSS MOSFETs, it is deduced that $\Delta\mu = (R_{\rm CH} - R_{\rm CH,PSS})/R_{\rm CH,PSS}$ and $\Delta I_{\rm dlin} = (R_{\rm TOTAL} - R_{\rm TOTAL,PSS})/R_{\rm TOTAL,PSS}$. From the above deductions, $\Delta I_{\rm dlin}$ can be expressed as a linear function of $\Delta\mu$ with an offset of $\Delta R_{\rm SD}$, as shown in (2a). According to (2a), the $R_{\rm SD,PSS}$-to-$R_{\rm CH,PSS}$ ratio of PSS MOSFETs is crucial in evaluating the dependence of $\Delta I_{\rm dlin}$ on the efficiency of $\Delta\mu$ and $\Delta R_{\rm SD}$ [2]. That is, at small $R_{\rm SD,PSS}$-to-$R_{\rm CH,PSS}$ ratio, $\Delta I_{\rm dlin}$ mainly stems from $\Delta\mu$ with an offset determined by $\Delta R_{\rm SD}$, which increases with the $R_{\rm SD,PSS}$-to-$R_{\rm CH,PSS}$ ratio, as shown in (2a'). Similarly, $\Delta I_{\rm dsat}$ can also be expressed as a linear function of $\Delta\mu$ with an offset of $\Delta R_{\rm SD}$, as shown in (2b). In (2b), the efficiency of $\Delta\mu$ translated into $\Delta I_{\rm dsat}$ is determined by the ballistic efficiency $B_{\rm sat,PSS}$ [5], where $B_{\rm sat,PSS}$ can be extracted by the temperature-dependent analytic model described in [3]. In addition to the contribution from $\Delta\mu$, $\Delta I_{\rm dsat}$ also benefits from $\Delta R_{\rm SD}$ with a factor k, where k may depend on device dimensions and process conditions [6], [7]. When substituting (2b) into (2a), the dependence of $\Delta I_{\rm dlin}$ on $\Delta I_{\rm dsat}$ is derived as (3). It is demonstrated that the correlation between $\Delta I_{\rm dlin}$ and $\Delta I_{\rm dsat}$ of nanoscale strained MOSFETs depends on both $R_{\rm SD,PSS}$-to-$R_{\rm CH,PSS}$ ratio and $B_{\rm sat,PSS}$.

The control and PSS MOSFETs with nominally identical drain-induced barrier lowering (DIBL), subthreshold swing, and inversion current–voltage (C–V) characteristic (not shown here [3]) were then characterized. $I_{\rm dlin}$ and $I_{\rm dsat}$ of both nMOSFETs ($L_{\rm physical} = 55-85$ nm) and pMOSFETs ($L_{\rm physical} = 75-125$ nm) were measured at $|V_G - V_T| = 1$ V. The $R_{\rm SD,PSS}$-to-$R_{\rm CH,PSS}$ ratio can be evaluated by the best fitting slope in the plot of $\Delta I_{\rm dlin}$ versus $\Delta I_{\rm dsat}$ and $B_{\rm sat,PSS}$ according to (3). The mobility of short channel device can then be extracted from (1b) [8].

III. Results and Discussion

Fig. 1 plots $\Delta I_{\rm dlin}$ versus $\Delta I_{\rm dsat}$ of PSS CMOSFETs at various gate lengths. At a given physical gate length, the fitting slope of PSS pMOSFETs is roughly two times larger than that of PSS nMOSFETs. It indicates that, with the same strain-induced mobility change, $\Delta I_{\rm dlin}$ of PSS pMOSFETs can be improved more than $\Delta I_{\rm dsat}$ while $\Delta I_{\rm dlin}$ and $\Delta I_{\rm dsat}$ of PSS nMOSFETs are similar, which is consistent with the results of [1]. In Fig. 2(a), as $L_{\rm physical}$ decreases, $B_{\rm sat,PSS}$ increases, which indicates carrier transport is closer to the ballistic transport regime, so that $\Delta I_{\rm dsat}$ will become less dependent on $\Delta\mu$ [9]. As mentioned above, the $R_{\rm SD,PSS}$-to-$R_{\rm CH,PSS}$ ratio [shown in Fig. 2(b)] can be obtained from the slope of $\Delta I_{\rm dlin}$ versus $\Delta I_{\rm dsat}$ as long as $B_{\rm sat,PSS}$ is known. It is found that the smaller the $L_{\rm physical}$ is, the higher the $R_{\rm SD,PSS}$-to-$R_{\rm CH,PSS}$ ratio is. In addition, the $R_{\rm SD,PSS}$-to-$R_{\rm CH,PSS}$ ratio of PSS nMOSFETs is higher than that of PSS pMOSFETs. Thus, the rising $R_{\rm SD,PSS}$-to-$R_{\rm CH,PSS}$ ratio will hurt strain-induced drain–current improvement, especially for PSS nMOSFETs in sub-100-nm regime.

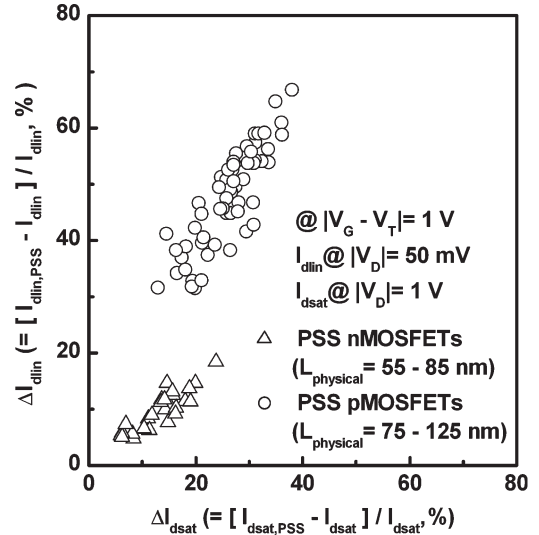

Fig. 1. $\Delta I_{\rm dlin}$ versus $\Delta I_{\rm dsat}$ of PSS CMOSFETs at various gate lengths ($L_{\rm physical} = 55-85$ nm for nMOSFETs, and $L_{\rm physical} = 75-125$ nm for pMOSFETs). The strain techniques employed in this letter are the contact etch stop layer (CESL) and the embedded SiGe S/D stressors for PSS nMOSFETs and PSS pMOSFETs, respectively.

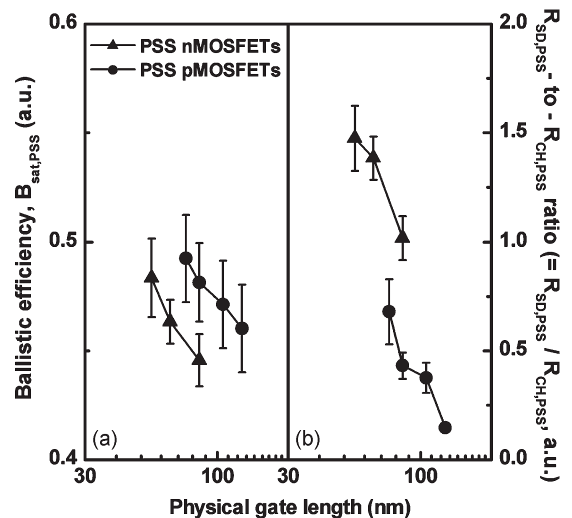

Fig. 2. (a) Ballistic efficiency ($B_{\rm sat,PSS}$) and (b) the ratio of S/D parasitic resistance ($R_{\rm SD,PSS}$) to channel resistance ($R_{\rm CH,PSS}$) of PSS CMOSFETs at various gate lengths ($L_{\rm physical} = 55-85$ nm for nMOSFETs, and $L_{\rm physical} = 75-125$ nm for pMOSFETs). From extracted $B_{\rm sat,PSS}$ [3] and the fitting slope of $\Delta I_{\rm dlin}$ versus $\Delta I_{\rm dsat}$ (Fig. 1), the $R_{\rm SD,PSS}$-to-$R_{\rm CH,PSS}$ ratio of PSS CMOSFETs at a given gate length can be calculated. The slope of $\Delta I_{\rm dlin}$ versus $\Delta I_{\rm dsat}$ at a given gate length is obtained by fitting a group of devices. It is noted that the $R_{\rm SD,PSS}$-to-$R_{\rm CH,PSS}$ ratio of PSS nMOSFETs is higher than that of PSS pMOSFETs.

Fig. 3 plots $\Delta\mu$ versus $\Delta I_{\rm dsat}$ of PSS CMOSFETs. At $L_{\rm physical} = 85$ nm, the fitting slopes (1.73 for nMOSFETs and 2.12 for pMOSFETs) are very close to the calculated $1/(1 - B_{\rm sat,PSS})$ (1.80 for nMOSFETs and 1.93 for pMOSFETs), which shows the validity of (2b). In addition, $\Delta I_{\rm dsat}$ of PSS

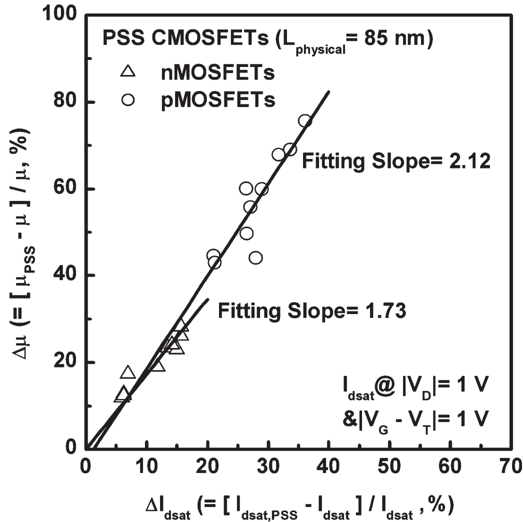

Fig. 3. $\Delta\mu$ versus ΔI_{dsat} of PSS CMOSFETs ($L_{\text{physical}} = 85$ nm). The solid lines represent the best fitting lines with the slopes of 1.73 and 2.12 for nMOSFETs and pMOSFETs, respectively. The fitting slopes are close to the calculated $1/(1 - B_{\text{sat,PSS}})$ values from Fig. 2(a) (1.80 for nMOSFETs and 1.93 for pMOSFETs). It validates the $\Delta\mu$-to-ΔI_{dsat} correlation by (2b).

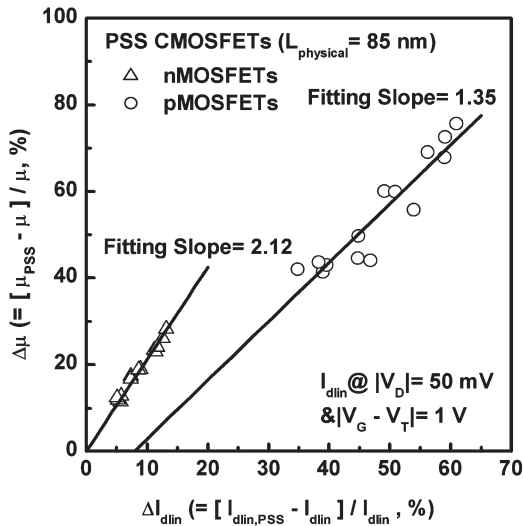

Fig. 4. $\Delta\mu$ versus ΔI_{dlin} of PSS CMOSFETs ($L_{\text{physical}} = 85$ nm). The solid lines represent the best fitting lines with the slopes of 2.12 and 1.35 for nMOSFETs and pMOSFETs, respectively. The fitting slopes are close to the $1 + R_{\text{SD,PSS}}/R_{\text{CH,PSS}}$ values from Fig. 2(b) (2.02 for nMOSFETs, 1.43 for pMOSFETs). It indicates the correlation between $\Delta\mu$ and ΔI_{dlin} can be predicted by (2a). The nonzero intercept of ΔI_{dlin} of PSS pMOSFETs stems from the reduced parasitic resistance of SiGe S/D.

CMOSFETs are roughly half of $\Delta\mu$ because the $B_{\text{sat,PSS}}$ values are 0.45 and 0.48 for nMOSFETs and pMOSFETs, respectively.

Fig. 4 plots $\Delta\mu$ versus ΔI_{dlin} of PSS CMOSFETs. At $L_{\text{physical}} = 85$ nm, for PSS nMOSFETs, $\Delta\mu$ is about two times of ΔI_{dlin} due to the $R_{\text{SD,PSS}}$-to-$R_{\text{CH,PSS}}$ ratio being larger than one. However, for PSS pMOSFETs, the $R_{\text{SD,PSS}}$-to-$R_{\text{CH,PSS}}$ ratio is less than one, which results in $\Delta\mu$ being close to ΔI_{dlin}. The fitting slopes (2.12 for nMOSFETs and 1.35 for pMOSFETs) are very close to the $1 + R_{\text{SD,PSS}}/R_{\text{CH,PSS}}$ (2.02 for nMOSFETs and 1.43 for pMOSFETs), which indicates that the correlation between $\Delta\mu$ and ΔI_{dlin} can be predicted by (2a). Therefore, the efficiency of $\Delta\mu$ translated into ΔI_{dlin} is dominated by the $R_{\text{SD,PSS}}$-to-$R_{\text{CH,PSS}}$ ratio. For PSS nMOSFETs, the $R_{\text{SD,PSS}}$-to-$R_{\text{CH,PSS}}$ ratio would be the bottleneck for further performance improvement by strain techniques. It is also worthy to note that the nonzero intercept of ΔI_{dlin} of PSS pMOSFETs, which stems from significant $R_{\text{SD,PSS}}$ reduction while SiGe S/D is adopted. However, for PSS nMOSFETs, insignificant ΔR_{SD} is observed.

IV. Conclusion

In this letter, the correlation between $\Delta\mu$, ΔI_{dlin}, and ΔI_{dsat} of nanoscale strained CMOSFETs is investigated. By virtue of the correlation between ΔI_{dlin} and ΔI_{dsat} and the ballistic efficiency, the ratio of S/D parasitic resistance to the channel resistance can be extracted easily. The efficiency of $\Delta\mu$ translated into ΔI_{dlin} and ΔI_{dsat} is dominated by the $R_{\text{SD,PSS}}$-to-$R_{\text{CH,PSS}}$ ratio and ballistic efficiency $B_{\text{sat,PSS}}$, respectively. For PSS nMOSFETs, the S/D parasitic resistance would be the bottleneck for translating $\Delta\mu$ into ΔI_{dlin} while for PSS pMOSFETs, $\Delta\mu$ can be translated into ΔI_{dlin} efficiently until the S/D parasitic resistance becomes comparable to/or higher than the channel resistance.

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