Low-K/Cu CMOS-Based SoC Technology With 115-GHz f_T, 100-GHz $f_{\max}$, Low Noise 80-nm RF CMOS, High-Q MiM Capacitor, and Spiral Cu Inductor

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***Abstract*—Logic CMOS-based RF technology is introduced for a 10-Gb transceiver in which active and passive RF devices have been realized in a single chip. RF nMOS of 115-GHz f_T, 100-GHz $f_{\max}$, and sub-1.0-dB $NF_{\min}$ at 10 GHz have been fabricated by aggressive device scaling and layout optimization. High-Q MiM capacitor and spiral Cu inductors have been successfully implemented in the same chip by 0.13-μm low-K/Cu back end of integration line technology. Core 1.0 V MOS and/or junction varactors for VCO at 10 GHz are offerings free of extra cost and realized by the elaborated layout.**

***Index Terms*— $f_{\max}$, f_T, inductor, MiM capacitor, $NF_{\min}$, RF CMOS, varactor.**

I. Introduction

THE REGULAR delivery of smaller and faster CMOS devices driven by Moore's law facilitates a fully CMOS solution for RF IC with the carrier frequency pushed upward to 10 GHz and beyond [1], [2]. Besides the regular transistor speed increase [3]–[8], the growing number of interconnect layers allows the realization of on-chip inductors and capacitors with higher Q [2]–[11]. In this paper, we will report a promising practice targeted on a 10-Gb transceiver, which is supported by 0.13-μm low-K/Cu $(K = 2.9)$ logic CMOS-based RF technology with 80-nm RF NMOS of 115-GHz f_T and sub-1.0-dB $NF_{\min}$ at 10 GHz integrated with a high Q metal–insulator–metal (MiM) capacitor $(Q@10\text{ GHz} > 30)$ and spiral Cu inductor $(Q@10\text{ GHz} \sim 20)$ in the same chip. It is noted that a fully CMOS voltage control oscillator (VCO) is one of the most challenging parts of RF transceiver design and fabrication due to the most demanding parameters of VCO such as large frequency tuning range, low phase noise, and low power [12]–[14]. In this paper, MOS or junction varactors are offerings free of extra masks and cost in which an elaborated layout was employed to suppress series resistance and to achieve enough Q. Triple well is introduced by deep n-well implant and proven more effective than a p^+ guard ring in terms of substrate noise isolation.

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TABLE I
MS/RF CMOS—Baseline "Vanilla" Technology Nodes 0.25, 0.18, 0.13 G and 0.13 LV. Time Frame From 1998 to 2002

Technology node	0.25μm	0.18μm	0.13μm	
			G	LV
Year	1998	2000	2002	2002
V_{DD}(V)	2.5	1.8	1.2	1
L_g (μm)	0.24	0.16	0.105	0.08
I_{on} (μA/μm)	600	600	525	590
I_{off} (nA/μm)	0.01	0.1	1	10
Gate delay, τ_{PD} (ps)	45	30	16	13.5
$1/\tau_{PD}$ Ratio	1	1.50	2.81	3.33
f_T (GHz)	30	60	85	115
f_T Ratio	1	2	2.83	3.83
Metal	5 Al	6 Al	7-8 Cu	7-8 Cu
IMD	Oxide	FSG	FSG	LK(BD)
K	3.9	3.7	3.7	2.9

II. RF CMOS—Enabler for SoC

The aggressive advancement of Si CMOS technology in the past decade has driven the microelectronics progress from a digitally oriented scheme to one well suited for RF and microwave applications. The commercialization of CMOS wireless transceivers was driven by the new market for cost sensitive products such as Bluetooth and IEEE 802.11 WLANs. The attribute of a commodity for the mentioned products brings the pressure of continuous cost down by increasing the levels of integration. The features of high integration, lower cost, lower power, and high performance associated with the logic CMOS process make it a critical enabler to the communication system-on-chip (SoC).

In this paper, we will demonstrate a good example through our Si in which CMOS-based RF gets good standing points in three aspects as follows. The first one is the higher integration. Process wise, it is exactly feasible to put RF active and passive devices together on the same chip and also RF elements together with mixed-signal (MS) and digital circuits. The second one is the lower cost, which is due to smaller chip size by higher integration, the adoption of an RF element as a portable module in logic baseline, the reduction of assembly and test cost by elimination of off-chip discrete components, and the extended usage of the logic design kits for the digital part. The last one is the lower power. For active devices, lower supply voltage facilitated

TABLE II
RF CMOS TECHNOLOGY OFFERINGS—10-Gb TRANSCEIVER

Elements	Devices		Layout	Parameter definition	Circuits	Performance Parameters
Active	RF CMOS		L_g, W_F	gate length, width	MUX/DMUX	f_T
			N_F	gate finger number	LNA, Mixer, VCOs	f_T, f_{MAX}, NF_{min}
Passive	MiM capacitor		L	unit cell length	LNA, Mixer	Q, C, ω_{SR} VCC1, TCC1
			W	unit cell width		
			N	unit cell number		
	Spiral Inductor		R	coil inner radius	LNA, Mixer, VCOs	Q, L, ω_{SR}
			W	coil width		
			S	inter coil space		
			N	coil number		
	Varactor	MOS	L_g, W_F	poly gate length, width	VCOs	Q, C, ω_{SR} C_{max}/C_{min} (tuning ratio)
			N_F	gate finger number		
		Junc	L	P^+ finger length		
			W	P^+ finger width		
			N	P^+ finger number		

by logic CMOS scaling is an effective way to reduce the active power. As for passive elements, high Q assisted by low-k intermetal dielectric (IMD) and thick Cu can reduce power dissipation and make better use of the energy.

A. MS/RF CMOS — Derivative of Logic Baseline

Table I provides an overview of the advantages provided by the standard logic CMOS scaling to RF active and passive devices. The time frame spanned from 1998 for the 0.25-μm to 2002 for 0.13-μm technology node, that is roughly two years per generation, and it brings gate length scaling of around 70% for every generation advancement and the corresponding supply voltage scaling of around 70% before the 0.13-μm low voltage (LV) technology. The improvement in the gate speed is impressive, i.e., more than double has been achieved by the 0.13-μm general purpose (G) technology compared to the 0.25-μm technology node, and more than triple by 0.13-μm LV with gate length scaling down to 80 nm. It is quite interesting to note that the f_T of RF CMOS just follows an even better rate of enhancement for each technology node. For 0.13-μm LV with gate length of 80 nm, f_T is nearly four times that of the 0.25-μm node with a gate length of 0.24 μm. The benefit in terms of logic gate speed and RF CMOS f_T matches our expectation. f_T is simply controlled by the transconductance G_m and gate capacitances but logic gate speed is complicated by the junction capacitances. Regarding the advancement of the back end of integration line (BEOL), the increased metal layers and the lower dielectric constant will benefit the MiM capacitor and spiral inductor by reduced substrate coupling and substrate loss. For 0.13-μm technology, eight metal layers are available for general logic and MS products, and low-K IMD with a dielectric constant below 3.0 to support high-speed applications. Due to the easy and cost-effective adoption of RF devices in the logic baseline, logic-based RF CMOS becomes a reality.

B. RF CMOS Technology Offerings—10-Gb Transceiver

Table II is an overview of 0.13-μm RF CMOS technology offerings for tens of gigahertz single-chip communication. A 10-Gb transceiver is one of the examples. Basically, one active and three passive elements are supported. "Active" represents RF CMOS transistors implemented by exactly the same process for general logic but with elaborated layout to achieve good RF performance like f_T, $f_{\max}$, and $\mathrm{NF}_{\min}$. Three passive elements to be offered are MiM capacitor, spiral inductor, and varactors. The major circuits to adopt these active and passive devices are low noise amplifier (LNA), mixer, VCO, and some switching circuits like MUX or DMUX. For RF CMOS use in MUX or DMUX, f_T representing the ideal gate speed (free from influence of junction capacitances) is the key but the applications in LNA, mixer, or VCO entail the real concern of all three parameters, f_T, $f_{\max}$, and $\mathrm{NF}_{\min}$. Regarding the passive elements, the general requirement is the higher Q. For example, a high-Q inductor is needed for VCO and LNA. Another example is that the MiM capacitor is a good choice for high linearity but a varactor to offer higher tuning ratio is needed by VCO, and the tradeoff between the tuning ratio and Q becomes a reality.

III. RF CMOS PERFORMANCE

Following the introduction of logic-based RF CMOS technology offerings and device portfolios, the exact performance measured from our RF CMOS transistors and passive elements will be presented to justify the system-level integration scenario that RF CMOS is an enabler for communication SoC.

A. RF nMOS f_T, $f_{\max}$, and $NF_{\min}$

RF CMOS transistors of multiple gate fingers with an appropriate selection of finger width $(\mathrm{W_F})$ and finger number $(\mathrm{N_F})$ are used in this paper to improve RF CMOS performance. We would like to emphasize more the RF power and noise measured by maximum power gain $(G_{\max})$, unit power gain cutoff frequency $(f_{\max})$, and minimum noise figure $(\mathrm{NF}_{\min})$ than the current gain (H_{21}) measured by f_T. The focus comes from the need to deliver a reasonable amount of RF power for communication. The RF noise and associated gain are critically important for front-end LNA, which sets the ultimate minimum noise floor for the whole communication system. Fig. 1 shows f_T, $f_{\max}$, and G_m (transconductance) and their correlation with the drain current density $(I_{D0} = I_D/\mathrm{W_F} \times \mathrm{N_F})$ under drain voltage at 1.0 V $(V_{\mathrm{DS}} = 1.0\ \mathrm{V})$. Both f_T and $f_{\max}$ increase with increasing I_{D0} and their peak values happen at a certain I_{D0} near the maximum

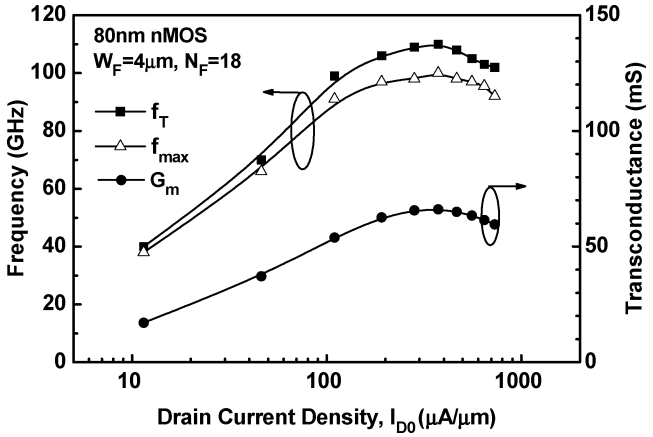

Fig. 1. Dependence of f_T, $f_{\max}$, and G_m (transconductance) on normalized drain current density ($I_{D0} = I_D/\mathrm{W_F} \times \mathrm{N_F}$) under drain voltage at 1.0 V, for 80-nm RF nMOS, $\mathrm{W_F} = 4\ \mu\mathrm{m}$, $\mathrm{N_F} = 18$.

G_m. Note that the $f_{\max}$ is extracted corresponding to the maximum available gain (MAG), which should be identical with that extrapolated from unilateral (U) power gain, provided that S_{12} (reverse gain) can approach zero by means of a lossless feedback network to validate the U method [15], [16]. Theoretically, U can be calculated from a set of two-port S parameters as given by (1). In practice, however, the measurement must be truly precise to achieve an accurate U due to the fact that the calculation of U generally involves the subtraction of two quantities, which may lead to a pretty small difference for some devices and result in excessive error [15]–[17]. In this paper, simulation with extensive calibration was employed to calculate MSG, MAG, and U to a frequency beyond 100 GHz for an accurate extraction of $f_{\max}$. The calibration was done on BSIM3 I-V and C-V models and the accuracy has been extensively verified and proven by good fit in terms of I_D, G_m, Y parameters, and f_T under a wide range of bias conditions and operating frequencies [18]. MSG and MAG can be calculated by (2) and (3) based on S parameters. Fig. 2 shows the simulated power-gain bandwidth characteristics in terms of MAG/MSG and U versus frequency beyond 100 GHz and a good match with measurement in terms of MAG/MSG up to 40 GHz. $f_{\max}$ was extracted by different methods for 80-nm nMOS with $\mathrm{W_F} = 4\ \mu\mathrm{m}$ and $\mathrm{N_F} = 18$. We see a dramatic difference in the extracted $f_{\max}$ by using the conventionally used U method (extrapolation along the line of U assuming slope fixed at -20 dB/dec for full frequency range) and that by the MAG method (unit gain of MAG and U occur at an identical frequency). As shown in Fig. 2(a), $f_{\max}$ extracted by the U method can achieve as high as 210 GHz, which is obviously higher than the 100 GHz extracted by the MAG method. Besides the extraction method, de-embedding also imposes a significant effect on the extracted $f_{\max}$ that is manifested by comparison between Fig. 2(a) and (b). $f_{\max}$ drops from 100/210 GHz extracted by the MAG/U method from S parameters going through both open and short de-embedding to 83/175 GHz from S parameters just going through open de-embedding but without short de-embedding. The apparent degradation of $f_{\max}$ corresponding to S parameters without short de-embedding accounts for the impact from parasitic resistances (R_G, R_D, R_S, and R_b) and inductances (L_G, L_D, and L_S), which should be extracted

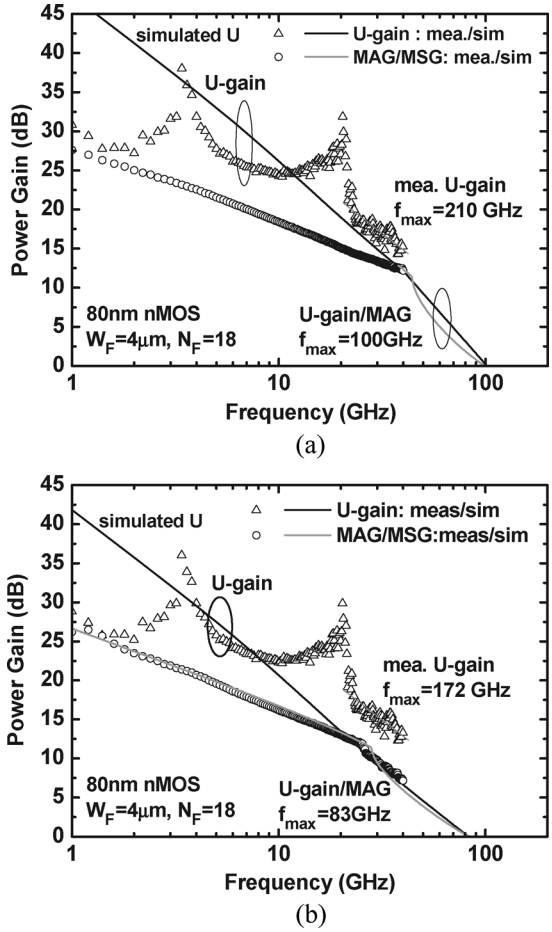

Fig. 2. Frequency response of power gain, maximum stable gain (MSG), maximum available gain (MAG), and unilateral gain (U) for $f_{\max}$ extraction (a) open and short de-embedding, $f_{\max} = 100/210$ GHz extracted by MAG/U method. (b) Open de-embedding only, $f_{\max} = 83/175$ GHz extracted by MAG/U method. 80-nm RF nMOS, $\mathrm{W_F} = 4\ \mu\mathrm{m}$, $\mathrm{N_F} = 18$.

through short de-embedding and removed from measured S parameters to achieve the truly intrinsic characteristics at high frequency

$$U = \frac{\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{2K\left|\frac{S_{21}}{S_{12}}\right| - 2\mathrm{Re}\left[\frac{S_{21}}{S_{12}}\right]} = \frac{|Y_{21} - Y_{12}|^2}{4\left[\mathrm{Re}(Y_{11})\mathrm{Re}(Y_{22}) - \mathrm{Re}(Y_{12})\mathrm{Re}(Y_{21})\right]} \quad (1)$$

$$\mathrm{MSG} = \left|\frac{S_{21}}{S_{12}}\right| \quad (2)$$

$$\mathrm{MAG} = \left|\frac{S_{21}}{S_{12}}\right|(K - \sqrt{K^2 - 1}) = \mathrm{MSG} * (K - \sqrt{K^2 - 1}) \quad (3)$$

where

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}.$$

The study done by Brodersen's group [19] highlighted the problem with accurate $f_{\max}$ extraction by using the U method

TABLE III
0.13-μm LOGIC CMOS-BASED RF nMOS $f_{\max}$ BENCHMARK—DEPENDENCE OF FINGER WIDTH, DRAIN CURRENT DENSITY, AND EXTRACTION METHOD

This work					Ref [19]		
W_F (μm)	4				W_F (μm)	4/1	
de-embedding	Open		Open/Short		de-embedding	Open/Short	
f_{max} extraction	MAG/U-gain Calibrated U	U-gain, -20 dB/dec	MAG/U-gain Calibrated U	U-gain, -20 dB/dec	f_{max} extraction	MAG/U-gain Calibrated U	U-gain, -20 dB/dec
$I_{DS}/(W_F x N_F)$ (μA/μm)	f_{max}(GHz)	f_{max}(GHz)	f_{max}(GHz)	f_{max} (GHz)	$I_{DS}/(W_F x N_F)$ (μA/μm)	f_{max}(GHz)	f_{max}(GHz)
110	79	-----	94	-----	90	75/115	-----
192	81	-----	97	-----	140	80/ 125	-----
282	83	172	100	210	245/300	85/ 135	NA/200

TABLE IV
STATE-OF-THE-ART RF nMOS PERFORMANCE BENCHMARK FOR 0.13-μm AND 90-nm TECHNOLOGIES

Publications	This work		Ref. [6]	Ref. [7]	Ref. [8]			Ref. [19]	
Technology node	0.13μm		90nm	90nm	0.13μm		90nm	0.13μm	
Gate length, L_g (nm)	80		70	65	92		63	NA	
V_{DD} (V)	1.0		1.2	1.0	1.5		1.2	1.2	
peak f_T (GHz)	115		150	150	92		140	90	
I_{DO}@peak f_T (μA/μm)	280		400	NA	NA		NA	300	
f_{max} extraction method	MAG/U-gain	U-method	U-method	U-method	NA		NA	MAG/U-gain	U-method
peak f_{max} (GHz)	100	210	200	206/280	90/109	**78/78	**108/120	85/135	NA/200
gate finger width,W_F(μm	4	4	5	4/2	5/1	5/1	5/1	4/1	4/1
I_{DO}@peak f_{max}(μA/μm)	282	282	250	NA	NA	NA	NA	300	300
Remark	MAG & Calibrated U	U-gain -20 dB/dec.	U-gain -20 dB/dec.	U-gain -20 dB/dec.	** : Calculated			MAG & Calibrated U	U-gain -20 dB/dec.

and got the same conclusion that the U method sometimes overestimated $f_{\max}$ as compared with that extracted by the MAG method. They reported an important observation that U actually drops at a rate much faster than the generally assumed 20 dB/dec slope, which is not valid in a high-frequency regime. Table III indicates $f_{\max}$ extracted by the calibrated U method incorporating the finger width and biasing current effect. The comparison between this paper and the published results [19] in terms of $f_{\max}$ under varying drain current density (I_{D0}) indicates better performance of higher $f_{\max}$ achieved by this work for finger width fixed the same $(\mathrm{W_F} = 4\ \mu\mathrm{m})$ and adopting the same de-embedding method, i.e., open and short. Table IV provides the RF nMOS performance benchmark with the state-of-art-technology at 90-nm nodes published by IMEC and Philips [6], [7], 0.13-μm and 90-nm nodes by IBM [8], and the 0.13-μm node by Brodersen's group [19]. We see a very consistent trend in f_T versus L_G scaling wherein 115 GHz achieved by 80-nm nMOS indicates 25% improvement over 92 GHz offered by 92-nm nMOS, both at the 0.13-μm node. However, $f_{\max}$ revealed a strong dependence on the gate finger width, biasing current, and extraction method. It makes the comparison much more complicated. The extraction by U method assumes a -20 dB/dec slope and generally predicts much higher $f_{\max}$. For our 80-nm nMOS with $\mathrm{W_F} = 4\ \mu$m,the U method suggests an $f_{\max}$ as high as 210 GHz, which happened to be nearly the same as the referred state-of-the-art $90 \sim 130$-nm technologies [6], [7], [19] adopting $\mathrm{W_F}$ at $4 \sim 5\ \mu$m. Our paper suggests that finger width is a dominant factor determining the peak $f_{\max}$ and a fair comparison of $f_{\max}$ should be based on the same extraction method.

Noise figure is an even more important parameter to be verified due to the general concern for the surface channel conduction nature by CMOS devices. Fig. 3(a)–(c) shows the intrinsic $\mathrm{NF_{min}}$ versus I_{D0} extracted for 80-nm nMOS of different $\mathrm{N_F}$, which operates under $V_{\mathrm{DS}} = 1.0\ V$ and various frequencies (2.4, 5.8, 10 GHz). We see that $\mathrm{NF_{min}}$ decreases with increasing I_{D0}, reaches a minimum point, and then turns up with a continuous increase of I_{D0}. An inverse relation with f_T can explain the observed dependence on drain current and it matches the theory that the higher the f_T, the smaller noise figure, as given by Fukui's formulas in (4) [20]. The intrinsic $\mathrm{NF_{min}}$ was extracted by a new lossy substrate de-embedding method to eliminate the lossy substrate and lossy pad effect [18]. Some improvement has been done to our previous work [18] to get nearly symmetric RLC networks for two ports, port-1 for gate and port-2 for drain, respectively. Fig. 4 presents our proposed equivalent circuit of the full structure with intrinsic MOSFET adopting two sets of RLC networks for extrinsic noise simulation and intrinsic noise extraction. RLC networks were used to model the lossy pad and lossy substrate effect. The accuracy has been verified by comparison with the measured S parameters for a full structure before de-embedding as well as those of open pads at port-1 and port-2. Fig. 5(a) and (b) proves the accuracy of our new lossy substrate model by a good match with the measured S_{11} and S_{22} of the full structure (a good fit to open pads' S parameters is also proven but not shown here). The intrinsic noise can be easily extracted through circuit simulation by removing the RLC networks from the original full structure shown in Fig. 4. The accuracy of the extracted intrinsic $\mathrm{NF_{min}}$ was supported by the calibrated intrinsic MOSFET model proven by a good fit in terms of $I_D - V_{\mathrm{gs}}$, $G_m - V_{\mathrm{gs}}$, Y parameters, and f_T [18]. The accuracy was further verified by a comparison with the well-known Fukui's model [20]. Fig. 6 shows a match within

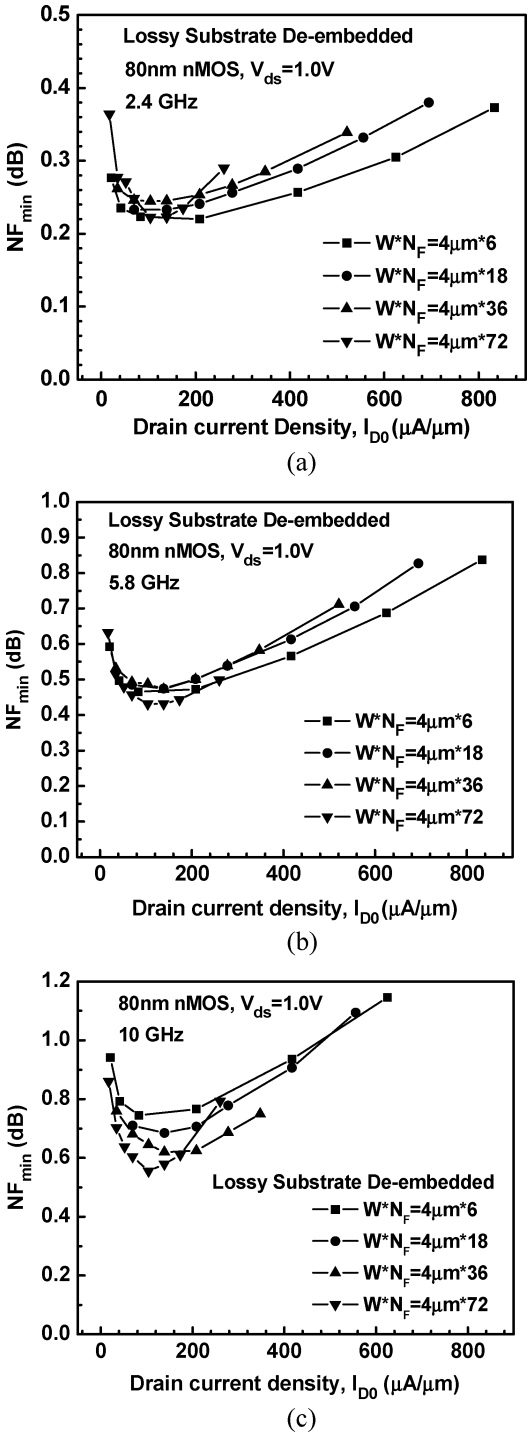

Fig. 3. Intrinsic $\mathrm{NF_{min}}$ extracted by lossy substrate de-embedding method for 80-nm nMOS with $\mathrm{W_F} = 4\ \mu\mathrm{m}$ and various finger numbers $\mathrm{N_F} = 6, 18, 36,$ and 72 operating under $V_{\mathrm{DS}} = 1.0\ V$ and various frequencies (a) 2.4 GHz, (b) 5.8 GHz, and (c) 10 GHz.

0.05 dB between the lossy substrate de-embedding method and Fukui's model in terms of frequency dependence for the minimum of $\mathrm{NF_{min}}$ under specific gate bias corresponding to the maximum G_m, i.e., maximum f_T. For various $\mathrm{N_F}$

$$F_{\min} = 1 + K\sqrt{G_m(R_g + R_s)}\frac{f}{f_T}$$
$$NF_{\min} = 10 \times \log(F_{\min}). \tag{4}$$

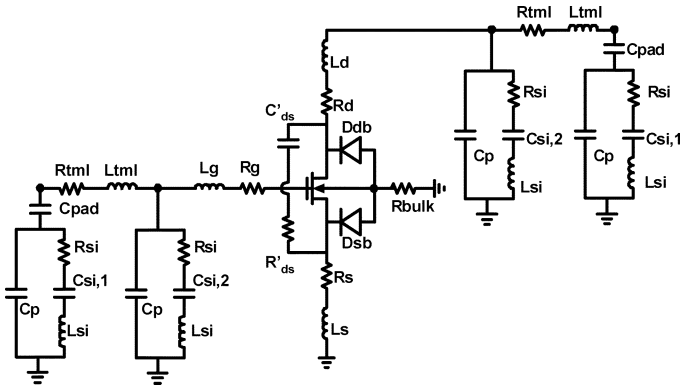

Fig. 4. Full circuit model with intrinsic MOSFET integrated with RLC network in which R, L, and C parasitics account for lossy pad (C_{pad}), lossy substrate (R_{Si}, L_{Si}, C_{Si}, and C_p), and transmission line (R_{tml}, L_{tml}) connected to gate and drain of MOSFET.

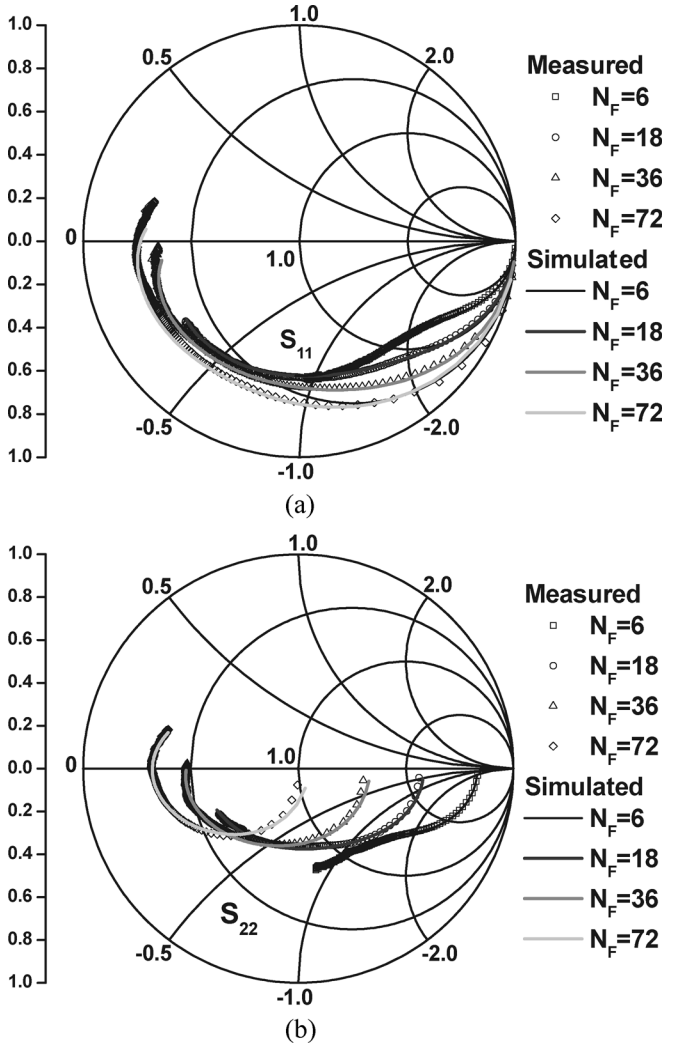

Fig. 5. Smith chart of measured S_{11} and S_{22} for full circuit with MOSFET and pads and good match by simulation using proposed RLC network (a) S_{11} and (b) S_{22}. nMOS with $\mathrm{N_F} = 6, 18, 36,$ and 72 and operating frequencies of 0.2∼40 GHz. Symbol is measured data and line is simulation.

For 2.4 GHz in Fig. 3(a), the minimum of $\mathrm{NF_{min}}$ corresponding to the optimized I_{D0} is obviously below 0.3 dB for all $\mathrm{N_F}$. Regarding 5.8 GHz in Fig. 3(b), the minimum of

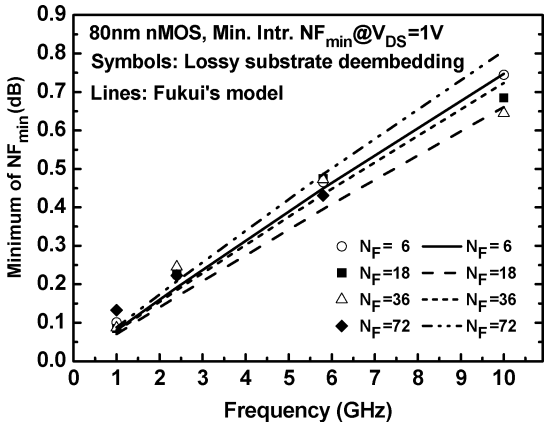

Fig. 6. Minimum of $\mathrm{NF_{min}}$ extracted by lossy substrate de-embedding method and compared with $V_{\mathrm{DS}} = 1.0$, V_{GS}, corresponding to maximum G_m. Operating frequencies are 2.4, 5.8, and 10 GHz.

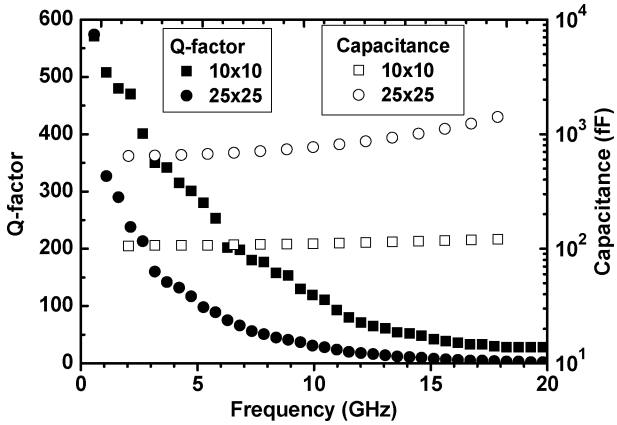

Fig. 8. Frequency dependence of Q and capacitance for MiM capacitors with different unit cell sizes, $10 \times 10\ \mu\mathrm{m}^2$ and $25 \times 25\ \mu\mathrm{m}^2$.

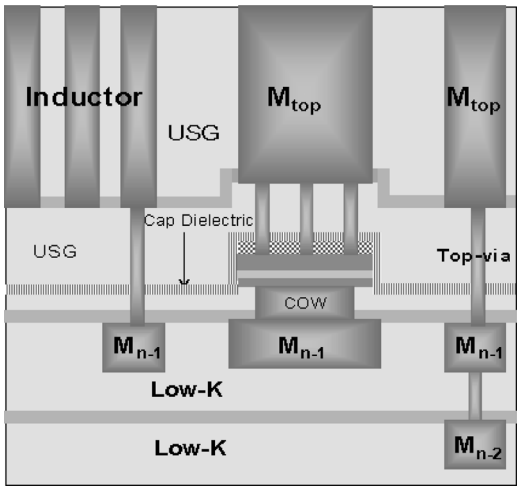

Fig. 7. Structure of MiM capacitor by M8/V7/M7 and inductor by top thick metal, M8. COW serves as bottom electrode of MiM capacitor.

$\mathrm{NF_{min}}$ is maintained no higher than 0.5 dB. As for 10 GHz in Fig. 3(c), the minimum of $\mathrm{NF_{min}}$ is kept below 0.8 dB for all $\mathrm{N_F}$, in which the best one is 0.55 dB for $\mathrm{N_F} = 72$ and the worst one is near 0.8 dB for $\mathrm{N_F} = 6$. Basically, the Fukui's model predicted that spread associated with different $\mathrm{N_F}$ will increase with increasing frequency and may explain our results with a larger spread at 10 GHz among various $\mathrm{N_F}$. However, the assumption of a fixed K in Fukui's formulas for various $\mathrm{N_F}$ and frequencies tends to overestimate the spread as compared with our results.

B. RF Passive Device Performance—MiM Capacitor, Spiral Inductor, and Varactors

1) MiM Capacitor Structure and Performance: In this paper, the on-chip inductor and MiM capacitor have been realized by 0.13-μm low-K/Cu technology. As shown by Fig. 7, the MiM capacitor was built by M7/V7/M8 (Metal 7/Via 7/Metal 8) and the spiral inductor was composed of M8, i.e., a thick top metal of 3-μm Cu. A perfectly clean microstructure was inspected by transmission electron microscopy (TEM) for the MiM capacitor in which a chemical–vapor deposition (CVD) oxide of around 38 nm was used as the intermetal dielectric. Regarding the linearity of major concern for applications in MS/RF circuits, promisingly good linearity with respect to voltage (VCC1) and temperature (TCC1) has been achieved by our MiM capacitor. VCC1 as low as 11.7 ppm/V is much better than the general specification of 30 ppm/V, and the TCC1 of around 42 ppm/°C is also better than the specification of 60 ppm/°C. Fig. 8 exhibits the excellent Q characteristics measured from our MiM capacitor with two different unit cell sizes. For a smaller cell with unit cell size of $10 \times 10\ \mu\mathrm{m}^2$, a Q as high as 435 can be achieved at 2.4 GHz and a Q higher than 100 can be maintained at 10 GHz. As for a larger cell with a unit cell size of $25 \times 25\ \mu\mathrm{m}^2$, Q drops to around 220 at 2.4 GHz but Q of 100/30 can be maintained at 5.2/10 GHz, which is sufficiently good for most of RF circuits. So far, a Q of 100 at 5 GHz is two times better than the specification $(Q@5\ \mathrm{GHz} > 50)$ defined by the 2004 International Technology Roadmap for Semiconductor (ITRS) [21] and also is better than that achieved by the state-of-the-art 90-nm CMOS MS/RF technology $(Q@5\ \mathrm{GHz} = 59)$ [4]. The excellently high Q accounts for the advantage realized by the novel structure of our MiM capacitor in which the series resistance has been greatly reduced by using a capacitor's open window (COW) as the bottom electrode. Another point worthy of mention is the cell size effect on the self-resonance frequency ω_{SR}, wherein the smaller cell size contributes the obviously higher ω_{SR}.

2) RF Passive Device Technology and Performance Benchmark: To verify the RF CMOS technology advancement effect on passive device performance, a benchmark was done by comparison of key performance parameters associated with each passive device, respectively. Table V indicates the benchmark done between this work using 0.13-μm LV technology [3] and others adopting 90-nm technologies [4]–[7]. All technologies deploy a Cu process in the BEOL to achieve the desired logic speed and improve RF passive performance simultaneously. As shown in Table V, the MiM capacitors fabricated reveal superior performance in terms of high Q over a wide and useful frequency range (2.4, 5, and 10 GHz). The Q enhancement of around 36%/71% in comparison with the conventional MiM structure implemented by 90-nm technology, corresponding to 2.4/5 GHz operation is a good indicator to justify the advantage

TABLE V
RF PASSIVE DEVICE TECHNOLOGY AND PERFORMANCE BENCHMARK

Publications	**This work**		**Ref. [4]**			**Ref. [5]**		**Ref. [7]**	
Technology	**0.13um**		**90nm**			**90nm**		**90nm**	
BEOL Metal Layers	**8 Cu layers**		**9 Cu layers**			**6 Cu layers**		**9 Cu layers**	
MiM capacitor	M7/M6		M8/M7			NA		NA	
Cap. Density, C_0(fF/um^2)	1.0		1.0	1.5	2.0	0.8		0.8	
VCC1 (ppm/V)	11.7		NA	NA	NA	NA		NA	
TCC1 (ppm/^{o}C)	-42		-49	38	37.5	NA		NA	
Unit Cell Area (um^2)	10x10	25x25	25x25			NA		NA	
Q@2.4 GHz	435	225	166	135	107	NA		NA	
Q@5 GHz	290	108	63	59	146	NA		NA	
Q@10 GHz	115	30	NA	NA	NA	NA		NA	
Spiral Inductor	M8/M7 (Cu)		M9/M8 (Cu)			M1-M6 (Cu)		M9/M8 (Cu)	
Coil Metal Thickness (um)	3		0.9	3	6	NA	6	0.9	
Layout/Ground-shield	single-end		single-end			single-end		differential	
Ground-shielding	x		x			v		v	
Inductance (nH)	0.93	3.5	~1			1.5	3.5	1.1	4
Peak Q@ω	24.9@5 GHz	16@2.4 GHz	12@~5G	23@~5G	26@~5G	12@4G	18@5G	24@15G	15@4~5G
Q@2.4 GHz	19.9	16	NA	NA	NA	9.5	14	~10	~13
Q@5 GHz	24.9	8.8	NA	NA	NA	11	18	~15	~15
Q@10 GHz	19.5	0.17	NA	NA	NA	NA	NA	20	< 2
MOS Varactor	Core 1.0V MOS		IO MOS			Core 1.2V MOS		GP(1.0V)/LP(1.2V)	
Structure	N+ Gate/N-well		N+ Gate/N-well			N+ G/NW	P+ G/PW	N+ Gate/N-well	
EOT/$T_{OX(INV)}$(nm)	1.7/2.4		NA			2.0/--	2.0/--	GP(1.6)/LP(2.1)	
C_{max}/C_{min} (Bias range)	6.2 (-1~+1V)		1.8			3.4	2.7	5.2	4.5
Q@2.4 GHz	45.5		60~120			>40	>30	NA	NA
Q@5 GHz	22.5		28~56			NA	NA	NA	NA
Q@10 GHz	7.7		NA			NA	NA	7.5	10

of the novel structure illustrated in Fig. 7. As for MOS varactors, the tuning ratio as high as 6.2 realized in this paper, using core 1.0-V gate oxide ($\mathrm{EOT/T_{OX(INV)}} = 1.7/2.4$ nm), is another advantage in comparison with the 1.8 achieved by the IO MOS varactor embedded in 90-nm technology [4] or 2.7~3.4 provided by core 1.2 V MOS varactor ($\mathrm{EOT} = 2.0$ nm) [5] and is somewhat better than the 5.2 attained by 1.0-V 1.6-nm nMOS varactor [7], all adopting 90-nm technologies. Q is maintained sufficiently high by layout optimization in this paper. Q under 2.4/5 GHz is maintained at 45.5/22.5, which is comparable with those achieved by 90-nm technology [5]. Q at 10 GHz dropped to around 7.7, which is nearly the same as that achieved by a differential varactor using 90-nm technology but with a lower tuning ratio at 5.2 [7]. In general, this kind of varactor can be used as a low cost solution (free of extra costs like masks or implant, etc.) and the lower Q can be compensated, e.g., by parallel with MiM capacitors of excellent Q. Besides, study on CMOS optical communication transceivers reported that the measurement on a 40-GHz LC MOS VCO suggests that the tank Q is dominated by that of an inductor rather than an MOS varactor [22]. Regarding the spiral inductor performance, use of a thick coil metal will obviously improve the Q attributed to the effectively reduced coil metal resistance [4], [5]. Peak $Q@5$ GHz $= 24.9$ ($N = 1.5$, $L = 0.93$ nH), achieved in this paper by using 3-μm Cu without any grounding shielding is somewhat better than the peak Q of 23 at 5 GHz ($L \sim 1$ nH) reported in [4], where nine Cu layers were adopted by 90-nm technology. Regarding larger inductor with L reaching 3.5 nH, the peak $Q@2.4$ GHz $= 16$ can be maintained by 3-μm Cu without any ground shielding. However, the use of ultra-thick Cu at 6 μm combined with ground shielding [5] can further improve Q to peak $Q@5$ GHz $= 18$. The comparison suggests that an ultra-thick coil metal and elaborated ground shielding or semi-insulating substrate [23] will help to improve Q for the on-chip inductors. A differential-type inductor can achieve superior Q even without using ultra-thick metal. Peak Q of 24 at 15 GHz was presented by using 0.9-μm Cu combined with ground shielding [7].

IV. CONCLUSION

In this paper, we have implemented RF active and passive devices on the same chip. All the RF devices are portable. We present it as a low-cost solution for communication SoCs in the tens of gigahertz era. The RF CMOS with 80-nm gate can achieve a satisfyingly good performance of 115 GHz f_T, 100 GHz $f_{\max}$, and sub-1.0 dB $\mathrm{NF_{min}}$ at 10 GHz without using ground shielding. Regarding the benefit from low-K/Cu BEOL, the eight layers of Cu can support an MiM capacitor and spiral inductor. MiM capacitor's Q is excellent, higher than 30, and a spiral inductor Q higher than 19, both at 10 GHz. In addition, two more advantages we believe are realized are the lower cost by smaller chip size and reusable logic core, as well as lower power by low-voltage CMOS and high-Q RF passive elements.

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REFERENCES

[1] P. H. Woerlee, M. J. Knitel, R. V. Langevelde, D. B. M. Klaassen, L. F. Tiemeijer, A. J. Scholten, and A. T. A. Z. Duijnhoven, "RF CMOS performance trends," *IEEE Trans. Electron Devices*, vol. 48, no. 10, pp. 1776–1782, Oct. 2001.

[2] T. H. Lee and S. S. Wong, "CMOS RF integrated circuits at 5 GHz and beyond," *Proc. IEEE*, vol. 88, no. 10, pp. 1560–1571, Oct. 2000.

[3] J. C. Guo, W. Y. Lien, M. C. Hung, C. C. Liu, C. W. Chen, C. M. Wu, Y. C. Sun, and P. Yang, "Low-K/Cu CMOS logic based SoC technology for 10 Gb transceiver with 115 GHz fT, 80 GHz fmax RF CMOS, high-Q MiM capacitor, and spiral Cu inductor," in *Symp. VLSI Tech. Dig.*, Japan, Jun. 2003, pp. 39–40.

[4] C. H. Chen, C. S. Chang, C. P. Chao, J. F. Kuan, C. L. Chang, S. H. Wang, H. M. Hsu, W. Y. Lien, Y. C. Tsai, H. C. Lin, C. C. Wu, C. F. Huang, S. M. Chen, P. M. Tseng, Y. T. Lin, C. F. Chang, H. J. Lin, J. C. Guo, G. J. Chern, D. Tang, and J. Y. C. Sun, "A 90 nm CMOS MS/RF based foundry SoC technology comprising superb 185 GHz f_T RFMOS and versatile, high-Q passive components for cost/performance optimization," in *2003 IEDM Tech. Dig.*, pp. 39–42.

[5] G. Baldwin, J. Ai, K. Benaissa, F. Chen, P. R. Chidambaram, S. Ekbote, S. Ghneim, S. Liu, C. Machala, F. Mehrad, D. Mosher, G. Pollack, T. Tran, B. Williams, J. Yang, S. Yang, and F. S. Johnson, "90 nm CMOS RF technology with 9.0 V I/O capability for single-chip radio," in *2003 VLSI Tech. Dig.*, pp. 87–88.

[6] W. Jeamsaksiri, A. Mercha, J. Ramos, D. Linten, S. Thijs, S. Jenei, C. Detcheverry, P. Wambacq, R. Velghe, and S. Decoutere, "Integration of a 90 nm RF CMOS technology (200 GHz $f_{\max}$ − 150 GHz f_T NMOS) demonstrated on a 5 GHz LNA," in *2004 VLSI Tech. Dig.*, pp. 100–101.

[7] L. F. Tiemeijer, R. J. Havens, R. de Kort, A. J. Scholten, R. van Langevelde, D. B. M. Klaassen, G. T. Sasse, Y. Bouttement, C. Petot, S. Bardy, D. Gloria, P. Scheer, B. Van Haaren, C. Clement, J.-F. Larchanche, I.-S. Lim, A. Zlotnicka, and A. Duvallet, "Record RF performance of standard 90 nm CMOS technology," in *2004 IEDM Tech. Dig.*, pp. 441–444.

[8] J. Pekarik, D. Greenberg, B. Jagannathan, R. Groves, J. R. Jones, R. Singh, A. Chinthakindi, X. Wang, M. Breitwisch, D. Coolbaugh, P. Cottrell, J. Florkey, G. Freeman, and R. Krishnasamy, "RFCMOS technology from 0.25 μm to 65 nm: The state of the art," in *Proc. 2004 CiCC Conf.*, pp. 217–224.

[9] J. N. Burghartz, "Progress in RF inductors on silicon—Understanding substrate losses," in *IEDM Dig.*, 1998, pp. 523–526.

[10] D.-W. Kim, I.-H. Jeong, H.-S. Sung, T.-O. Kong, J.-S. Lee, C.-M. Man, and Y.-S. Kwon, "High performance RF passive integration on Si smart substrate," in *Proc. IEEE MTT*, 2002, pp. 1561–1564.

[11] S. Jenei, S. Decoutere, K. Maex, and B. Nauwelaers, "Add-on Cu/SiLK module for high Q inductors," in *IEEE EDL*, 2002, vol. 23, pp. 173–175.

[12] J. Maget, M. Tiebout, and R. Kraus, "Influence of novel MOS varactor on the performance of a fully integrated UMTS VCO in standard 0.25 um CMOS technology," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 953–958, Aug. 2002.

[13] A.-S. Porret, T. Melly, C. C. Enz, and E. A. Vittoz, "Design of high-Q varactors for low power wireless applications using a standard CMOS process," *IEEE J.l Solid-State Circuits*, vol. 35, no. 2, pp. 337–345, Feb. 2000.

[14] M. A. Do, R. Zhao, K. S. Yeo, and G.-J. Ma, "Fully integrated 10 GHz CMOS VCO," *Electron. Lett.*, vol. 37, pp. 1021–1023, 2001.

[15] S. J. Mason, "Power gain in feedback amplifiers," *IRE Trans. Circuit Theory*, vol. CT-1, no. 2, pp. 20–25, 1954.

[16] J. M. Rollett, "The measurement of transistor unilateral gain," *IEEE Trans. Circuit Theory*, pp. 91–97, 1965.

[17] J. Lange, "A much improved apparatus for measuring the unilateral gain of transistors at GHz frequencies," *IEEE Trans. Circuit Theory*, vol. CT-13, no. 4, pp. 461–463, 1966.

[18] J. C. Guo and Y. M. Lin, "A lossy substrate model for sub-100 nm, super-100 GHz f_T RF CMOS noise extraction and modeling," in *2005 RFIC Tech. Dig.*, pp. 145–148.

[19] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Millimeter-wave CMOS design," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144–155, 2005.

[20] H. Fukui, "Optimal noise figure of microwave GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. ED-26, no. 7, pp. 643–650, Jul. 1979.

[21] International Technology Roadmap for Semiconductor 2004 Update: RF and Analog/Mixed-Signal Technologies for Wireless Communication.

[22] B. Razavi, "Prospects of CMOS technology for high-speed optical communication circuits," *IEEE J. Solid-State Circuits*, vol. 37, no. 10, pp. 1135–1145, Oct. 2002.

[23] D. D. Tang, W. C. Lin, L. S. Lai, C. H. Wang, L. P. Lee, H. M. Hsu, C. M. Wu, C. W. Chang, W. Y. Lien, C. P. Chao, C. Y. Lee, G. J. Chern, J. C. Guo, C. S. Chang, Y. C. Sun, D. S. Du, K. C. Lan, and L. F. Lin, "The integration of proton bombardment process into the manufacturing of mixed-signal/RF chips," in *2003 IEDM Tech. Dig.*, pp. 673–676.

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