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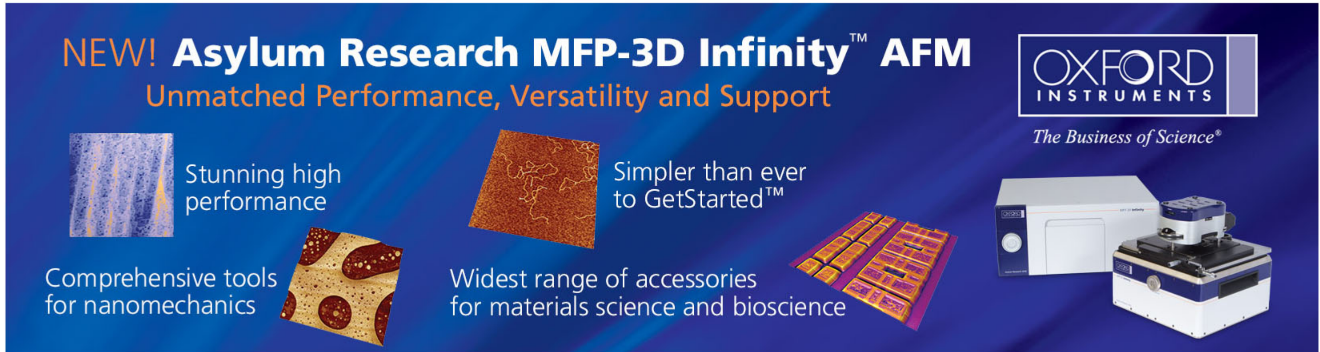

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Study of void formation due to electromigration in flip-chip solder joints using Kelvin bump probes

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Kelvin bump probes were fabricated in flip-chip solder joints, and they were employed to monitor the void formation during electromigration. We found that voids started to form at approximately 5% of the failure time under 0.8 A at 150 °C, and the bump resistance increased only 0.02 mΩ in the initial stage of void formation. Three-dimensional simulation was performed to examine the increase in bump resistance at different stages of void formation, and it fitted the experimental results quite well. This technique provides a systematic way for investigating the void formation during electromigration. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2226989]

Electromigration in flip-chip solder joints has become an important reliability issue due to the high-density and high-performance requirements,[1,2] and it has been studied extensively in recent years.[3–7] The current-crowding-induced voiding on the cathode/chip side was proposed to be responsible for the failure at the cathode/chip side of the solder joints.[2,4,5] For Al and Cu interconnects, void nucleation and propagation during electromigration are monitored by the change in resistance.[8–10] In addition, Kelvin probes have long been employed to measure via or contact resistance in the interconnects.[11–13] With the aid of Kelvin probes, via or contact resistance can be monitored to investigate the initial stage of void formation or microstructure change in the via or in the contact. In previous electromigration studies of flip-chip solder joints, daisy-chain structures were used to monitor the change in resistance. Nevertheless, the resistance of a solder bump was estimated in the order of a few milliohms, whereas the resistance of the metallization trace ranges from a few hundred to a few ohms, depending on its dimension. Thus, the bump resistance is quite small compared with the resistance of the metallization traces,[14] and the daisy-chain structure cannot detect the slight changes in resistance due to void formation in the solder joint. Kelvin probes have recently been implemented in flip-chip solder joints for electromigration study.[15,16] However, void nucleation and propagation as well as the change in bump resistance due to void formation remain unclear.

In this study, we used Kelvin bump probes to monitor the change in bump resistance during electromigration. It was found that a change in bump resistance as small as 0.01 mΩ could be detected. The increase in bump resistance due to void formation can be examined at different stages. Three-dimensional (3D) finite element modeling was also performed to simulate the increase in bump resistance due to void formation. This approach facilitates the systematic study of void formation due to electromigration in flip-chip solder joints.

We have designed and fabricated Kelvin probes for flip-chip eutectic SnPb solder joints. Figure 1(a) shows the cross-sectional schematic for the structure. The test structure consisted of four bumps, which were connected by an Al trace. The four bumps were labeled bump 1–bump 4. The Al trace was 1.5 μm thick and 100 μm wide. The pitch for the solder joints was 1 mm. Six Cu lines on the FR4 substrate were connected to the four bumps, and they were labeled as nodes 1–6, as shown in the figure. The Cu lines were 30 μm thick and 100 μm wide. With these six Cu lines, various experimental setups can be performed to measure the bump resistance for bump 2 or bump 3, or the resistance for the middle segment of the Al trace. In this study, current was applied through nodes 3 and 4, i.e., electrons flowing from the chip side to the substrate side for bump 3, and the opposite direction for bump 2, as illustrated in Fig. 1(a). The voltage change in bump 2 was monitored through nodes 1 and 2, whereas the voltage change in bump 3 was monitored through nodes 5 and 6. Therefore, the change in bump resistance during electromigration for the two bumps with opposite direction of electron flow can be monitored simultaneously. In general, void is formed in the chip side of bump 3 due to the serious current crowding effect.[2] Hence, we will present the results only for bump 3 in this letter. The power supply used in this measurement was a Keithley 2400, which has a 0.1 μV resolution in voltage measurement. The error in measuring resistance in this study was estimated to be 1–10 μΩ.

The schematic structure of the flip-chip bumps used in this study is shown in Fig. 1(b). The underbump metalliza-

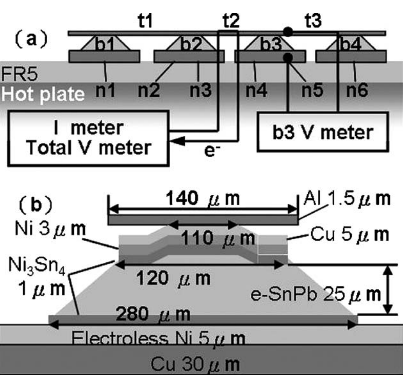

FIG. 1. (a) Cross-sectional schematic of the layout design. The Al trace connected all the four solder bumps together. (b) Schematic structure for the solder bump used in this study.

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TABLE I. The properties of materials used in the simulation models.

Materials	Al	Cu	Ni	Ni_3Sn_4	Eutectic SnPb	Electroless Ni
Resistivity	3.2	1.7	6.8	28.5	14.6	70 $\mu\Omega$ □ cm

tions (UBM) was 0.5 μm Ti/0.5 μm Cu/5 μm Cu/3 μm Ni. The Ti layer and the 0.5 μm Cu seed layer were sputtered, whereas the 5 μm Cu and the 3 μm Ni layers were electroplated. The passivation and UBM openings were 110 and 125 μm in diameter, respectively. Eutectic SnPb solder was used for the joint. The dimension of the pad opening was 280 μm in diameter. Owing to the large opening in the substrate side, the bump height was as small as 25 μm. Our previous simulation results showed that current crowding effect occurred within 20 μm depth in solder bump near the entrance of the electron flows on the chip side.[17] Therefore, it is expected that mechanism of void formation for these low-bump-height joints should be quite similar to those with normal bump height of about 100 μm.

3D simulation was performed to examine the change in bump resistance due to void formation. The morphology of Ni_3Sn_4 intermetallic compound (IMC) was assumed to be of layered type with uniform thickness of 1.0 μm, as shown in Fig. 1(b). The resistivity values of the materials used in this simulation are listed in Table I. ANSYS simulation software was employed and the model used in this study was SOLID5 eight-node hexahedral coupled field element.

The increase in bump resistance during electromigration can be precisely measured using Kelvin bump probes, and it can be employed to monitor the void formation and microstructure change during electromigration. Figure 2(a) shows the total resistance for the stressing circuit as a function of stressing time up to failure when powered by 0.8 A at 150 °C. The initial resistance was 1.77 Ω, and no obvious increase in resistance could be observed until 90% of the stressing time. Yet, the enlarged curve up to 80% of the failure time shows that the total resistance decreased initially, and then increased with stressing time, as illustrated in the inset of Fig. 2(a). The decrease in total resistance may be attributed to the reduction in contact resistance of the whole stressing circuit. The total resistance increased about 30 mΩ after stressing for 80% of the failure time. This resistance increase may be mainly due to the degradation or oxidation of Cu lines in the FR4 substrate and of the Cu wires used to connect the package to the power supply during current stressing, since no obvious resistance increase was detected in the Al trace between bumps 2 and 3. In addition, the noise of the resistance curve was about 5–10 mΩ. The noise may be mainly attributed to the temperature coefficient of resistance (TCR). If we take the average TCR value for the stressing circuit to be 4×10^{-3} K^{-1}, the fluctuation in resistance in the stressing circuit would be 7 mΩ/deg. However, the bump resistance measured by Kelvin bump probes showed a different behavior. This can be seen in Fig. 2(b), which shows the measured resistance of bump 3 up to failure. The initial bump resistance was only 0.6 mΩ. As the stressing time increased, the bump resistance continued to increase slowly up to 80% of failure time, and the bump failed when the resistance rose abruptly at around 756.6 h. The inset in Fig. 2(b) shows the data in 2(b) up to 80% of the stressing time. The bump resistance started to increase after 20 h. The time for the resistance to reach 1.03 times of the initial value

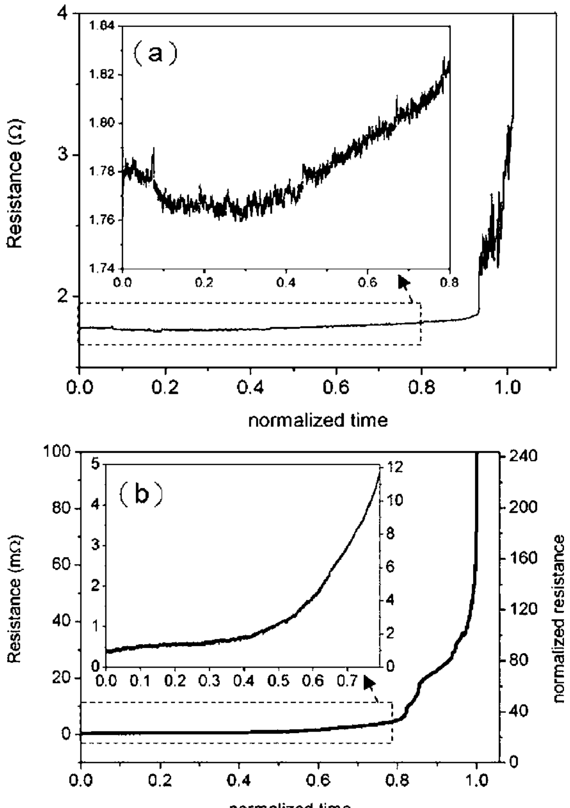

FIG. 2. (a) The total resistance as a function of normalized stressing time. The inset shows the change in resistance up to 80% of the failure time. (b) The bump resistance measured as a function of normalized stressing time up to failure. The inset shows the data up to 80% of the failure time.

was 29.8 h, which was 4% of the failure time. Voids may start to form at this stage, and we will discuss this point below. In contrast to the results from the daisy-chain structure, this technique can detect the subtle change in bump resistance. This is because the total resistance of the daisy-chain circuit was in the order of several ohms and noise in resistance due to TCR effect was over 7 mΩ,[2] whereas the increase in resistance in the initial stage of void formation is less than 1 mΩ. Therefore, the noise in the total resistance makes it difficult for the daisy-chain structure to detect the slight change in resistance due to void formation.

The initial bump resistance was only 0.6 mΩ measured at 0.8 A at 150 °C, which was much lower than expected. Two reasons may be responsible for this low bump resistance. First, the bump height was only 25 μm, which was about a quarter of the typical value. Second, the Kelvin probes for measuring voltage drop were located in a low current density region of the Al pad. Our previous 3D simulation showed that the current did not spread uniformly in the UBM opening, instead the current crowded into the solder bump in a small volume near the entrance point of the Al trace.[17] Since only a small amount of the current passed through the opposite end of the entrance point of the current, the voltage drop measured by the Kelvin probes was lower than expected.

The Kelvin probes can detect different stages of void formation and propagation, and Figs. 3(a)–3(c) show the void formation at different stages. Figure 3(a) shows the cross-sectional scanning electron microscope (SEM) image for the bump before current stressing, while Fig. 3(b) shows the SEM image for another bump stressed by 0.8 A at

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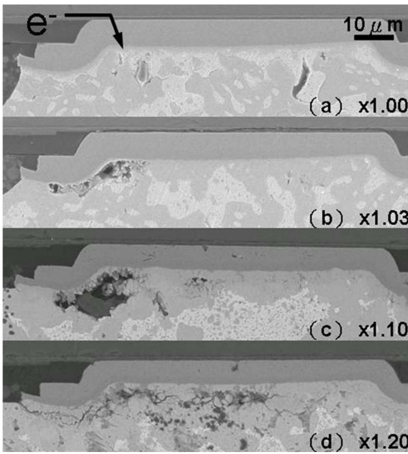

FIG. 3. (a) Cross-sectional SEM image for the bump before current stressing; cross-sectional SEM image for the bump stressed by 0.8 A at 150 °C for (b) 29.8 h and (c) 101.5 h.

150 °C for 29.8 h. The bump resistance increased from 0.60 to 0.62 mΩ after the current stressing, which is an increase of 1.03 times the initial value. The direction of the electron flow is indicated by the arrow in the figure. This condition is denoted as stage I in this letter. Small voids started to form under the IMC layer in the left corner of the passivation opening, where current crowding occurred most seriously. Owing to the slower IMC formation rate between Ni and Sn, no clear IMC formation was observed in the initial stage. Another bump was stressed at the same condition for 101.0 h, and the current was terminated when the bump resistance reached 1.10 times the initial value. The cross-section image is shown in Fig. 3(c), which shows larger voids at the interface of the solder and the IMC. This condition is denoted as stage II. Under the stressing conditions, voids started to form at approximately 5% of the failure time, and they grew for the rest of the stressing time. The incubation time for void formation is relatively short compared with the failure time. This may be attributed to the fact that the cross section of the UBM opening is quite large, and thus it takes time for the voids to propagate and deplete the UBM opening.

To investigate the change in bump resistance due to void formation, 3D modeling was performed to simulate the voltage distribution in the solder joint. Figure 4(a) shows the voltage distribution in the solder joint without void formation when 0.2 A was applied. The voltage drop on the right-hand side was much smaller than that on the left-hand side, resulting in the low bump resistance of about 0.5 mΩ measured by the Kelvin probes. The simulated voltage drop across the right-hand side of the solder was 0.002 mV, and thus the corresponding bump resistance was 0.4 mΩ, which is close to the experimental values. Figure 4(b) illustrates the voltage distribution in the solder joint for stage I when a small void is formed near the entrance of the Al trace on the left-hand side. The void depleted about 8% of the UBM opening. The bump resistance increased only 0.02 mΩ, which is about 1.04 times of the initial value. As the void grew bigger, the available cross section for conducting current became smaller and more current drifted to the right-hand side of the bump, resulting in the increased bump resistance, as shown in Figs. 4(c). The bump resistance increased to 1.11 times its initial value for stage II. The experimental and simulation results for the two stages show good agreement.

In summary, the Kelvin probes appear to be very sensitive to void formation and propagation, so they can detect the different stages of void formation during electromigration. Therefore, they can be employed to investigate the electromigration behavior systematically.

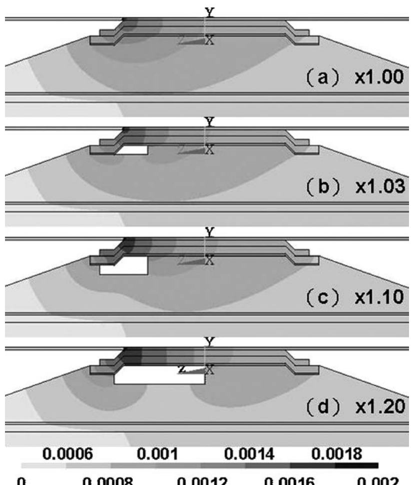

FIG. 4. (a) Simulation results showing the voltage distribution in the solder joint when 0.2 A was applied (a) without void formation, and then after the void formed (b) at stage I and (c) at stage II.

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