

# SSH and SHH GaInP/GaAs HBT divide-by-3 prescalers with true 50% duty cycle

S.C. Tseng, C.C. Meng and W.Y. Chen

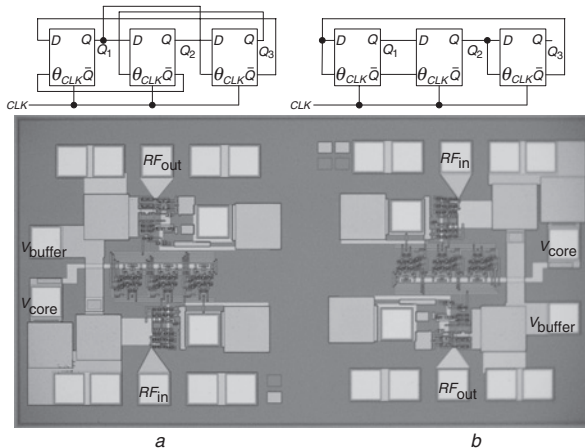
Two 50% duty cycle divide-by-3 prescalers – sample-sample-hold (SSH) and sample-hold-hold (SHH) prescalers – in the 2 μm GaInP/GaAs heterojunction bipolar transistor (HBT) technology are realised. Current switchable emitter couple logic *D* flip-flops are employed to form both prescalers. The proposed SHH prescaler functions up to 2.6 GHz while the SSH prescaler operates from DC to 1.75 GHz. The maximum operating frequency of the SHH prescaler is enhanced about 50% compared with that of the SSH prescaler owing to better signal synchronisation.

**Introduction:** Regarding the overall communication system, the frequency planning largely influences the hardware architectures and circuits. The frequency divider is indispensable to support good frequency planning. The most commonly used frequency divider is a divide-by-2 prescaler which has been studied by many researchers [1]. However, in the frequency planning, other divisors such as 3, 5, 7, and so on, are needed and a fractional divisor was also developed [2]. For example, the divide-by-3 circuit is employed in the dual-band GSM system to reduce the interferences between a local oscillator and a mixer [3]. Nevertheless, the traditional divide-by-3 prescaler utilising two *D* flip-flops triggered at the rising edge of the clock to perform frequency division has a 33% duty-cycle output and results in both odd and even harmonics. An imperfect 50% duty-cycle signal can deteriorate the performance of high-speed circuits and its even harmonics also affect mixer performance, especially in a direct conversion system.

Two methods of generating a 50% duty-cycle signal were offered in [4, 5]. Yao and Tsai employed a duty-cycle trimming circuit to trim the output signal length while Chen applied an exclusive OR gate to change the clock state. These two methods need more circuits and reduce the speed of a prescaler. A new current switchable emitter couple logic *D* flip-flop is utilised to construct a 50% duty-cycle divide-by-3 prescaler without extra circuits [6]. This novel *D* flip-flop can form two different architectures of prescalers – sample-sample-hold (SSH) and sample-hold-hold (SHH) prescalers – by connecting the switching signals among *D* flip-flops in a different way. The SHH prescaler is proposed in this Letter, while the SSH prescaler is derived from Magoon and Molnar's paper [6].

**Circuit design:** Because the traditional *D* flip-flop updates data only at the rising or falling edge of the clock, the output level cannot change in the middle of a three-cycle duration to generate a 50% duty-cycle divide-by-3 signal. In this Letter, these 50% duty-cycle divide-by-3 prescalers are based on a current switchable emitter couple logic *D* flip-flop shown in Fig. 6 in [6]. A current-switching quad is inserted between the sample-and-hold stage and the clock stage to commutate the clock current signal and switch the triggering edge of the clock for sample-and-hold. Sampling data occurs when clock and current-switching control signal,  $\theta$ , are the same, while holding data occurs when clock and  $\theta$  are opposite. This current switchable *D* flip-flop can reload data at the half cycle of the clock and then the output, *Q*, can alternate between high and low levels at the rising and falling edges of the clock. Thus, a 50% duty cycle divide-by-3 prescaler can be realised.

The architecture of the SSH divide-by-3 prescaler shown in Fig. 1a is altered from the divide-by-3 prescaler proposed by Magoon and Molnar [6]. Their prescaler is negatively triggered while the positive triggered architecture is adopted in this Letter. The polarity of the switching signal determines the trigger edge of the prescaler. The operation mode of the current switchable *D* flip-flops in this prescaler is sample-sample-hold repeatedly in this order, and the duration of each state is half clock cycle. This operation constructs a 50% duty-cycle divide-by-3 prescaler. In this structure, the switching signal of a *D* flip-flop is related to the output of the following *D* flip-flop. However, the data signal has relation with the output of the previous *D* flip-flop. The signal asynchrony between the switching and data signals should be reduced to enhance the maximum operating frequency of the prescaler.

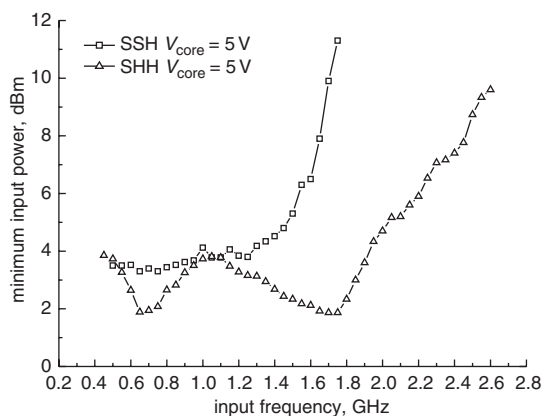


**Fig. 1** Architectures and die photos of sample-sample-hold (SSH) and sample-hold-hold (SHH) divide-by-3 prescalers with 50% duty cycle

a SSH prescaler  
b SHH prescaler

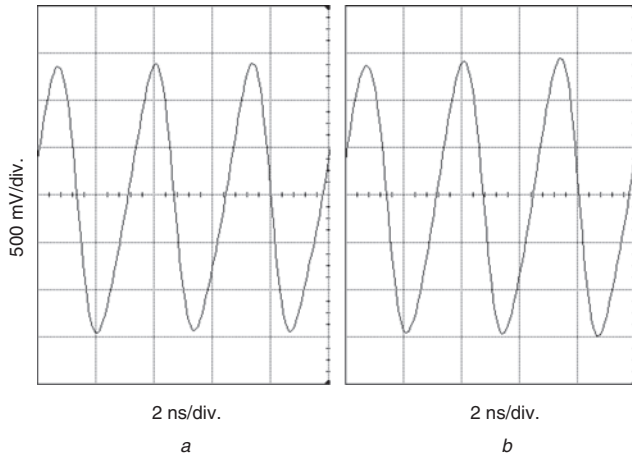
An improved structure – SHH prescaler – is proposed in this Letter and shown in Fig. 1b. The operation mode of the *D* flip-flops in this prescaler is sample-hold-hold repeatedly in this order. The only difference between SSH and SHH prescalers is connection of the switching signals of the current switchable *D* flip-flops. Thus, power consumption is almost the same. Obviously, the switching and data signals are related to the outputs of the same previous *D* flip-flop. There is no time delay between the switching signal,  $\theta$ , and data input signal, *D*. Because of better signal synchronisation, the maximum operating frequency of the SHH prescaler can be enhanced 50% compared with that of the SSH one from our experiments.

**Measurement results:** The die photos of the 2 μm GaInP/GaAs HBT SSH and SHH prescalers are shown in Fig. 1 and each size including pads is about 1 × 1 mm<sup>2</sup>. Both prescalers have 17 mA current consumption at 5 V supply. Fig. 2 shows the measured sensitivity. The SHH prescaler can function up to 2.6 GHz while the SSH counterpart works only up to 1.75 GHz. Clearly, the SHH structure has about 50% performance improvement in maximum operating frequency, because the SHH prescaler has the synchronous data and switching signals (*D* and  $\theta$ ). The input sensitivity level is 2–11 dBm.



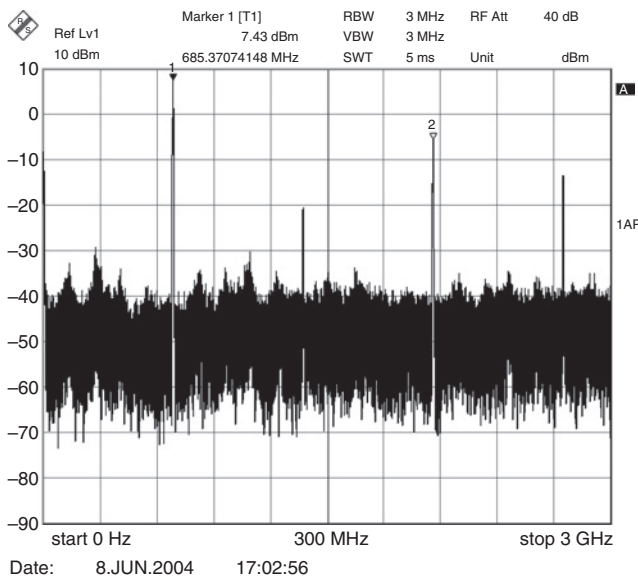
**Fig. 2** Sensitivity of SSH and SHH divide-by-3 prescalers with 50% duty cycle

The output waveforms of these prescalers with a 900 MHz input signal are shown in Fig. 3 and both have true 50% duty cycle. The output spectrum of the SHH prescaler with a 2.05 GHz input signal is shown in Fig. 4. The second harmonic of the output signal is 30 dB lower than the fundamental tone and 17 dB lower than the third-harmonic tone. Because of the true 50% duty cycle of the output signal, the even harmonics are lower than the odd harmonics.



**Fig. 3** Output waveforms of SSH and SHH 50% duty cycle divide-by-3 prescalers with 900 MHz input signal

a SSH prescaler  
b SHH prescaler



**Fig. 4** Spectrum of 50% duty-cycle divide-by-3 SHH prescalers with 2.05 GHz input signal

**Conclusion:** Two 50% duty-cycle divide-by-3 prescalers fabricated in the 2  $\mu\text{m}$  GaInP/GaAs HBT technology are sample-sample-hold and sample-hold-hold prescalers. A current switch quad is used in the  $D$  flip-flop to switch the current and alternate the output level at either positive or negative clock edges. The SSH prescaler works from DC to 1.75 GHz while the SHH operates up to 2.6 GHz. The switching signal in the SHH structure is synchronous to the data signal. Thus, the SHH prescaler has 50% performance improvement in the maximum operating frequency over the SSH counterpart.

**Acknowledgments:** This work was supported in part by the National Science Council of the Republic of China under contract NSC 94-2752-E-009-001-PAE, NSC 94-2219-E-009-014, in part by the Ministry of Economic Affairs under contract 94-EC-17-A-05-S1-020, and by the National Chip Implementation Center (CIC).

© The Institution of Engineering and Technology 2006  
9 March 2006

*Electronics Letters* online no: 20060553  
doi: 10.1049/el:20060553

S.C. Tseng, C.C. Meng and W.Y. Chen (*Department of Communication Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, Republic of China*)

## References

- 1 Mokhtari, M., Fields, C., Rajavel, R.D., Sokolich, M., Jensen, J.F., and Stanchina, W.E.: '100 + GHz static divide-by-2 circuit in InP-DHBT technology', *IEEE J. Solid-State Circuits*, 2003, **38**, (9), pp. 1540–1544
- 2 Yang, Y.C., Yu, S.A., Wang, T., and Lu, S.S.: 'A dual-mode truly modular programmable fractional divider based on a 1/1.5 divider cell', *IEEE Microw. Wirel. Compon. Lett.*, 2005, **15**, (11), pp. 754–756
- 3 Magoon, R., Molnar, A., Zachan, J., Hatcher, G., and Rhee, W.: 'A single chip quad band (850/900/1800/1900 MHz) direct conversion GSM/GPRS RF transceiver with integrated VCOs and fractional-N synthesizer', *IEEE J. Solid-State Circuits*, 2002, **37**, (12), pp. 1710–1720
- 4 Yao, C.-Y., and Tsai, J.-W.: 'Programmable divide-by-N counter with 50% duty-cycle output', *Electron. Lett.*, 1999, **35**, (8), pp. 624–625
- 5 Chen, C.F.: 'Design of a divide-by-N asynchronous odd-number counter with 50/50 duty cycle', *Proc. IEEE*, 1974, **62**, (9), pp. 1278–1279
- 6 Magoon, R., and Molnar, A.: 'RF local oscillator path for GSM direct conversion transceiver with true 50% duty cycle divide by three and active third harmonic cancellation'. *IEEE RFIC Symp.*, 2002, pp. 23–26