Strain enhanced DC-RF performance of 0.13 µm nMOSFETs on flexible plastic substrate

A. Chin, H.L. Kao, C.H. Kao, C.C. Liao, Y.Y. Tseng and C.C. Chi

A 14.3% saturation current $I_{d,sat}$ improvement and 0.75 dB minimum noise figure ($NF_{\min}$) at 10 GHz were measured by applying ~0.7% tensile strain for 16 finger, 0.13 µm RF MOSFETs with thin-body (40 µm) substrate mounted on plastic. These excellent results for mechanical-strain on DC-RF MOSFETs are better than those of SiN-capped 90 nm strained-Si nMOSFETs and consistent with device simulations.

Introduction: To integrate the Si-base RF integrated circuits (ICs) on high-resistivity Si substrate [1] is an important technology. Since the passive devices have a poor Q-factor [1–4] arising from the low resistivity (10 Ω-cm) VLSI-standard Si substrates, integrating RF ICs on insulating plastic provides better passive devices at lower cost than those on lossy VLSI-standard Si substrates. In addition, the thin-body Si IC on plastic is useful for flexible electronics, RF ID, wireless displays and system-on-plastic [5, 6]. The thin-body Si substrate provides flexibility for applying mechanical strain. In this Letter we report the DC and RF performance of 0.13 µm thin-body (40 µm) Si MOSFETs on plastic with mechanical strain. The saturation drain current ($I_{d,sat}$) was improved 14.3% and a 0.75 dB lower minimum noise figure ($NF_{\min}$) was obtained at 10 GHz for 0.13 µm MOSFETs on plastic with ~0.7% tensile strain. The excellent performance is better than that for SiN-capped, 90 nm node, strained-Si nMOS (11%) [7]. Such DC-RF performance improvements were confirmed by TMA simulations for strained 0.13 µm MOSFETs. They arise from the thin body thickness (t_b) and high flexibility, where the surface strain increases with $1/t_b^2$ [8]. The RF noise improvement fits well an analytical $NF_{\min}$ equation [9], and is due to the increase in the g_m and the RF gain under strain.

Experiment procedure: In this study we used 180 µm low-cost, highly-insulating polyethylene substrates, which had a resistivity of 10^8–10^9 Ω-cm. The multiple-gate-finger 0.13 µm RF MOSFETs with microstrip line layout were designed on 8-inch wafers at an IC foundry [9]. The multiple-gate-finger structure can reduce the thermal noise generated from gate resistance. The microstrip line layout can shield the RF noise generated in the lossy Si substrate network, instead of a conventional coplanar waveguide (CPW) structure [9]. To achieve integration onto plastic, we first thinned-down the Si substrate from 500 to 40 µm using the chemical mechanical polish (CMP) process and then glued it onto a 180 µm-thick plastic (Fig. 1*a*). Fig. 1*b* shows the large surface strain on 40 µm Si substrate. Owing to the flexibility of the thinned-down Si substrate, we can apply large mechanical strain onto the Si substrate without any cracking to measure the DC and RF characteristic. Furthermore, the surface strain can be calculated using ANSYS 8.0 simulation software and the device characteristics were simulated under various applied tensile strain using TMA process-device simulation software. The DC, *S*-parameters and noise figure were measured using HP4155C, a HP8110 network analyser and the ATN-NP5B noise parameter measurement system, respectively [9].

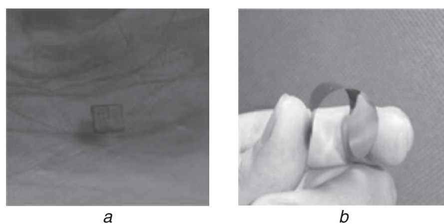

Fig. 1 *Image of die with multiple-gate-finger 0.13 µm RF MOSFET on transparent plastic, and high flexibility of ~40 µm-thick Si substrate (t_b) under mechanical strain*

a Image of die with multiple-gate-finger 0.13 µm RF MOSFET on transparent plastic (held by hand)
Substrate of die thinned to ~40 µm
b High flexibility of ~40 µm-thick Si substrate (t_b) under mechanical strain (proportional to $1/t_b^2$)

Results and discussion: The DC characteristics of 16-gate-finger 0.13 µm RF MOSFETs on a VLSI-standard Si substrate, and on plastic, are shown in Fig. 2. The $I_d - V_d$ characteristics show almost identical before and after thinning and mounting on plastic. Similarly, little change appeared in the measured RF current gain $|H_{21}|^2$, as depicted in Fig. 3. It is indicated that the thinned-down process did not damage the devices. This improvement over the previous ICP etching and thinning process [5] is due to the fact that CMP technique avoids plasma damage. In addition, Figs. 2 and 3 show the modelling data using the TMA process-device simulations software. Good agreement between measured and simulated $I_d - V_d$ and $|H_{21}|^2$ were obtained using the accurate TMA process-device simulations on VLSI-standard Si substrate.

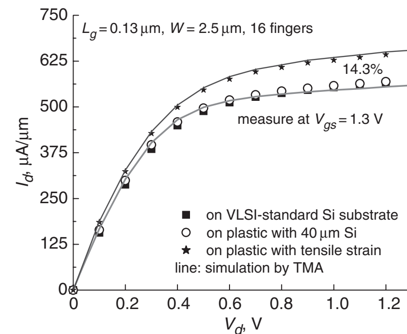

Fig. 2 *Measured and simulated $I_d - V_d$ for 16-gate-finger 0.13 µm RF MOSFETs on VLSI-standard substrate and on plastic with 40 µm Si, with or without tensile strain*

Solid lines are TMA-simulated data for VLSI-standard Si substrate and on plastic under ~0.7% tensile strain

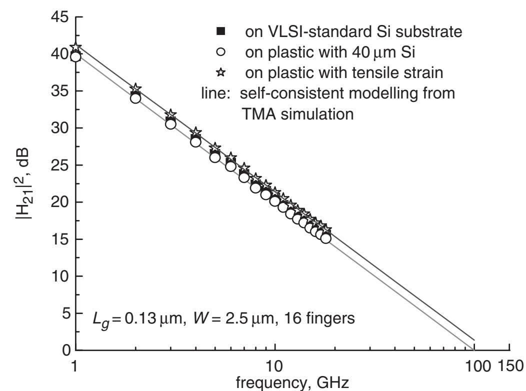

Fig. 3 *Measured and simulated $|H_{21}|^2$ against frequency for 16-gate-finger 0.13 µm RF MOSFETs on VLSI-standard substrate and on plastic with 40 µm Si with or without tensile strain*

Line is modelled data

Because of the flexibility of the thinned-down Si substrate it can be subjected to large levels of strain. The large surface strain ($\varepsilon = 3aF/bt_b^2E$) [8] results from the applied force (F) associated with a bending distance (a) and width (b). We calculated the surface tensile strain using ANSYS 8.0 software, as shown in Fig. 4. The bending distance is about 0.17 cm when we applied 0.8 GPa stress on 40 µm Si substrate. Therefore, tensile strain is 0.7% (= 0.8 GPa/115 GPa) where the Young's modulus of Si is 115 GPa.

In this condition, we measured the $I_d - V_d$, *S*-parameter and $NF_{\min}$. Figs. 2 and 3 show the $I_d - V_d$ characteristic and RF current gain $|H_{21}|^2$ of 16-gate-finger 0.13 µm RF MOSFETs on plastic with and without tensile strain, respectively. The f_T is extracted on RF current gain $|H_{21}|^2$ equal to 1. Under the applied 0.7% tensile strain on plastic, the $I_{d,sat}$ increased 14.3% and the unity-gain cutoff frequency f_T increased from 103 to 118 GHz. Such improved $I_{d,sat}$ and f_T under strain is also confirmed by TMA simulation and also shown in Figs. 2 and 3. It is indicated that the increased $I_{d,sat}$ and f_T are the result of increased electron mobility which is the result of the reduced intervalley scattering under tensile strain [10]. A large improvement occurred compared with SiN-capped 90 nm strained-Si nMOS (11%) [7], owing to the $1/t_b^2$ dependence of the strain for thin-body Si.

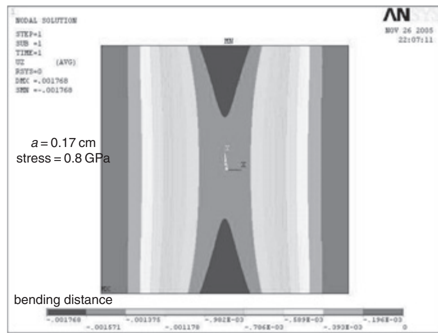

Fig. 4 *Mechanical stress calculated using ANSYS 8.0 simulation software*

Fig. 5 shows the $NF_{\min}$ and associated gain of 0.13 µm transistors under tensile strain. The $NF_{\min}$ decreased from 0.89 to 0.75 dB and the associate gain increased from 14.2 to 15.3 dB at 10 GHz. The $NF_{\min}$ is lower than the unstrained case over the whole frequency range. The lower $NF_{\min}$ from strain arises through [9]:

$$NF_{\min} \cong 1 + 2\gamma(1 + g_m R_g/\gamma)^{0.5} f/f_T \quad (1)$$

The close agreement between the measured and simulated $NF_{\min}$, as shown in Fig. 5, indicates that the lower $NF_{\min}$ arises from the strain-improved f_T. The $NF_{\min}$ is better than those for 90 nm node SiN-capped strained-Si nMOS [7] in Fig. 5. The large DC-RF improvements with strain are some of the advantages of thin-Si-body flexible electronics on plastic.

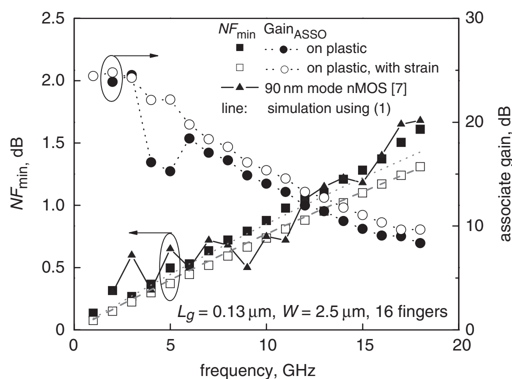

Fig. 5 *Frequency dependence of NF_{min} and associate gain of body-thinned 16-gate-finger 0.13 µm RF MOSFETs on plastic under strain*

Conclusion: High performance was achieved for thin-body 0.13 µm MOSFETs on plastic. These devices showed excellent low noise performance (0.75 dB at 10 GHz), high associated gain (15.3 dB) and a 14.3% $I_{d,sat}$ increase. Such high performance RF transistors are improved by thinning the substrate and making it flexible to apply tensile strain.

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A. Chin, H.L. Kao, C.C. Liao and Y.Y. Tseng (*Department of Electronic Engineering, National Chiao Tung Univeristy, Nano Science Technology Center, University System of Taiwan, Hsinchu 30050, Taiwan, Republic of China*)

E-mail: achin@cc.nctu.edu.tw

C.H. Kao (*Department of Accounting Information, Takming College, Taiwan, Republic of China*)

C.C. Chi (*Department of Physics, National Tsing Hua University, Hsinchu, Taiwan, Republic of China*)

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