Nitridization of the Stacked Poly-Si Gate to Suppress the Boron Penetration in pMOS

Yung Hao Lin, *Student Member, IEEE*, Chao Sung Lai, *Student Member, IEEE*, Chung Len Lee, *Senior Member, IEEE*, Tan Fu Lei, and Tien Sheng Chao, *Member, IEEE*

Abstract— **NH_3-nitridation to create nitrogen-rich layers in-between the stacked layers of the poly-Si gate for pMOS application is proposed and demonstrated. Due to the blocking of fluorine diffusion in the poly-Si gate by the nitrogen-rich layers, the amount of fluorine in the gate oxide, consequently, the fluorine enhancement on boron penetration is reduced. The negative effects of the NH_3-nitridized oxide were not found in this work. Moreover, this nitridized stacked poly-Si gate improves significantly the electrical characteristics of the gate oxide as a result of the indirect and slight nitridation at the gate oxide.**

I. Introduction

Recently, a p^+-poly-Si gate was recommended for the surface-channel pMOSFET to avoid the short-channel effects in sub-micron CMOS [1]. The boron implantation, due to its channeling effect , alleviates its use in forming shallow junctions. Thus, for the self-alignment process in doping gates and forming S/D shallow junctions, BF_2^+-implantation is generally used [2]. However, the boron used to dope this p^+-polysilicon gate easily penetrates through the gate oxide into the underlying Si-substrate, especially when fluorine is incorporated [3]–[7] in the BF_2^+-implantation. This causes device reliability problems such as the positive shift of the threshold voltage and degradation of the p-channel inverse subthreshold [6]–[7].

Suppression of the boron penetration in pMOS by using an oxynitride was studied [8]–[11]. NH_3-nitridized oxide is effective in preventing the boron penetration due to the nitrogen incorporation into the gate oxide. However, the unintended incorporated hydrogen results in higher electron trapping rates, lower charge to breakdown, and larger interface state generation [9]–[10]. Although reoxidization can reduce the hydrogen content in the gate oxide and thus improve the electrical characteristics [8], it simultaneously reduces the incorporated nitrogen in the gate oxide and consequently reduces the effectiveness in suppressing the boron penetration [8], [11]. Recently, N_2O was used to nitridize the gate oxide, to replace NH_3, due to its freedom from hydrogen-related effects [8]–[11]. However, the N_2O-nitridation results in less nitrogen incorporation at the gate oxide than that of NH_3, and is not that effective in suppressing the boron penetration [9].

Previously, a stacked gate structure to effectively suppress the boron penetration was proposed [12]. Recently, a method of using an oxide gettering effect to reduce the fluorine enhancement on boron penetration for the BF_2^+-implanted pMOS was also proposed [13]. In this work, NH_3-nitridation the poly-Si gate, instead of the gate oxide, is proposed to create nitrogen-rich layers in-between the stacked layers. It is to be demonstrated that this further suppresses the boron penetration and significantly improves the electrical characteristics of MOS devices. It is due to nitrogen-rich layers, which were created by nitridation that block the fluorine diffusion in the poly-Si film and consequently reduce the amount of fluorine in the gate oxide. Therefore it reduces the enhancement of the boron penetration by fluorine [3]–[7], [13]–[14]. SIMS analysis shows that nitrogen atoms piled-up at the nitridized poly-Si interface and diffuse into the underlying gate oxide. The nitrogen incorporation in the gate oxide significantly improves the breakdown fields and breakdown charges in the oxide. Unlike the conventional directly NH_3-nitridized gate oxide, the hydrogen-related effects do not exist due to less hydrogen incorporated as a result of the effective H-gettering effect of grain boundaries [15] of the polysilicon gate and the low pressure nitridation [16].

II. Experimental

The NH_3-nitridized stacked poly-Si gate pMOS capacitors, as illustrated in Fig. 1 with the "PHPP" sample as an example, were fabricated on (100), 5~10 Ω-cm, n-type Si wafers with a 80 Å gate oxide. The gate oxide was grown in diluted dry O_2 ($O_2/N_2 = 1/6$) at 900 °C and annealed in N_2 at the same temperature for 15 min. After that, an undoped polysilicon was deposited at 625 °C in a low pressure chemical vapor deposition (LPCVD) system in three steps, 1000 Å in each step; and a low pressure (120 mTorr) nitridation in NH_3 at 900 °C for 80 min was performed between poly I and poly II for the sample "PHPP" or between poly II and poly III for the sample "PPHP". The nitridized silicon films were soaked in diluted HF ($HF/H_2O = 1/50$) before the following poly-Si layer deposition. To study the thermal effect and the N_2O-nitridation effect on the poly-Si gate, some samples were annealed in atmospheric pressure Ar (PAPP and PPAP) or N_2O (PNPP and PPNP), also at 900 °C for 80 min, with the corresponding NH_3-annealed samples (PHPP and PPHP). For comparison, control samples with the same stacked poly-Si

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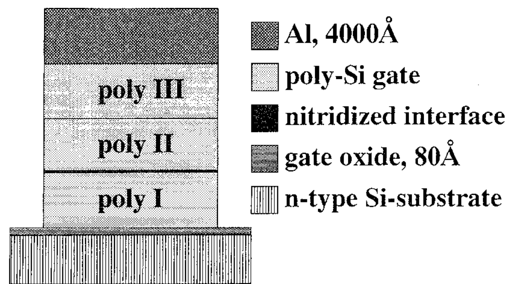


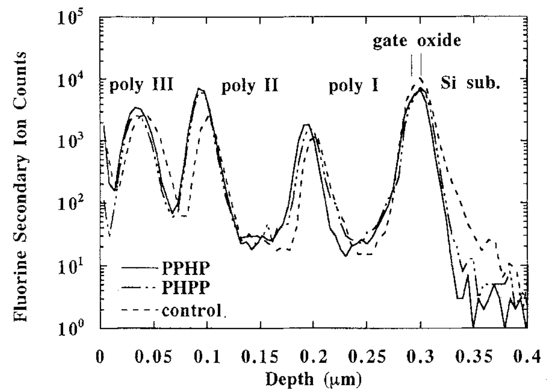
Fig. 1. The pMOS capacitor structure of PHPP with the NH_3-nitridized poly-Si gate.

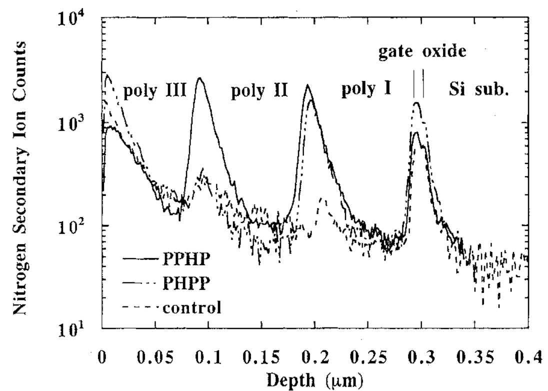
gate but without thermal annealing were also fabricated. Then all the samples were implanted with BF_2^+ at 50 KeV of a dose 5×10^{15} cm^{-2}, and annealed first at 800 °C in O_2 for 30 min to prevent boron out-diffusion and then at 900 °C in N_2 for 10, 20, 30, and 40 min, respectively. After the polyoxide was removed, Al was deposited and annealed at 400 °C in N_2 for 30 min to make MOS capacitors.

III. Results and Discussions

Fig. 2(a)–(c) show the SIMS fluorine, nitrogen, boron and hydrogen profiles of the 900 °C, 40 min N_2-annealed PPHP, PHPP, and control samples, respectively. It is seen in Fig. 2(a) that fluorine atoms diffused rapidly along grain boundaries in the poly-Si film and segregated at the gate oxide as well as at the interfaces of stacked layers after the post-implant-annealing [17], [18]. For the control sample which had the conventional stacked gate structure [12], although the interfaces of stacked layers acted as sinks for implanted fluorine, however, it had the highest fluorine at the gate oxide, as compared to PPHP and PHPP samples. It was because for PPHP and PHPP samples, NH_3 nitridation to the poly-Si gate created a large amount of nitrogen piling up at the interfaces of stacked layers, as seen from Fig. 2(b). These nitrogen-rich layers somehow blocked the fluorine diffusion through the poly-Si gate, as shown in Fig. 2(a) where the fluorine peaks of PPHP and PHPP samples were higher than those of the control sample at the interfaces of stacked poly-Si layers. Thus, the fluorine enhancement on boron penetration in the gate oxide was reduced [3]–[7], [13]–[14]. And both boron curves of PPHP and PHPP had lower peaks at the SiO_2/Si interface and shallower profiles in the Si substrate than that of control sample, as shown in Fig. 2(c).

On the other hand, due to the nitrogen diffusion along the grain boundaries of poly-Si, nitridation effect also occurred at the interface between poly I and poly II and at the gate oxide for both PHPP and PPHP samples. At the gate oxide region, due to the gate oxidation in the diluted O_2, nitrogen had been incorporated into the control sample. However, the nitrogen curves of PPHP and PHPP are higher than that of the control sample, especially at the region near the poly-Si/SiO_2 interface. PHPP had more nitrogen incorporated into the gate oxide due to its thinner nitridized poly-Si film (1000 Å) than that of PPHP (2000 Å). These incorporated nitrogen relieved the interfacial strain between the poly-Si film and the gate oxide, similar to the effect of nitrogen in the directly nitridized gate oxide [19], [20], and hence improved the electrical characteristics, which were to be shown latter.





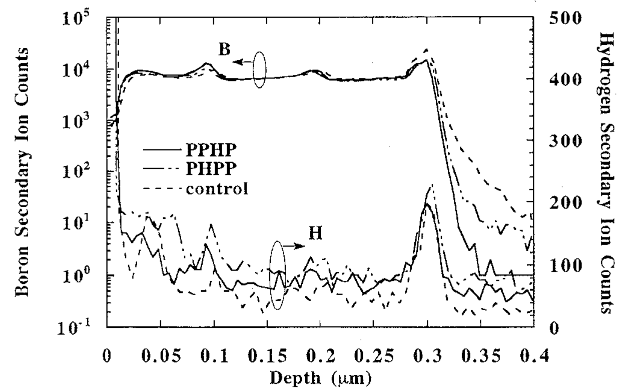


Fig. 2. The (a) fluorine, (b) nitrogen, and (c) boron and hydrogen SIMS profiles of the 900 °C 40 min annealed PPHP, PHPP, and control samples.

Fig. 3 shows the positive shifts of the flatband voltage (V_{fb}) of the capacitors after the prolonged post-implant annealing. These were due to the negative fixed charges generated by F-B complexes and a very shallow p-type layer in the Si-substrate as the result of the boron penetration [9]–[11]. PPHP and PHPP, which had the NH_3-nitridized poly-Si gate, had the least V_{fb} shift among all the samples. This indicates that the fluorine enhancement on boron penetration was reduced by the

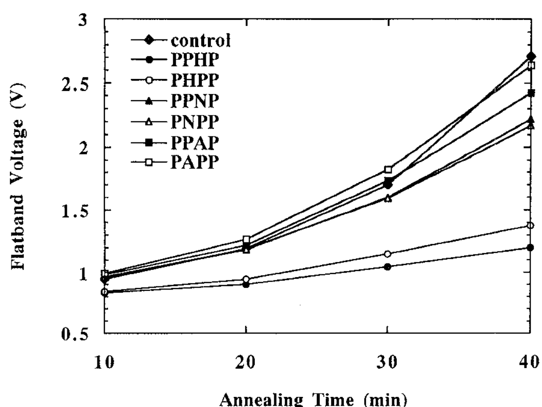


Fig. 3. The flatband voltage (V_{fb}) versus the post-implant annealing time at 900 °C.

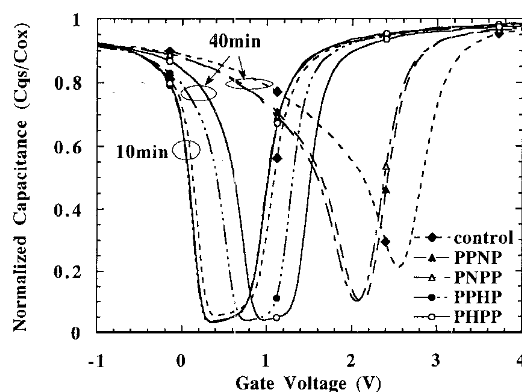


Fig. 4. The normalized quasistatic C-V curves (C_{qs}/C_{ox}) of the 900 °C, 10 and 40 min annealed samples.

nitrogen-rich layers at the stacked poly-Si gate. Furthermore, the better thermal stability of PPHP than that of PHPP indicates that the two nitrogen-rich layers of PPHP blocked more fluorine diffusion than the one layer of PHPP. In the figure, although the PPNP and PNPP samples with the N_2O-nitridized poly-Si gate [21] also had better thermal stability than that of the control sample, they were not as effective as PPHP and PHPP in suppressing the boron penetration. This is believed to be due to that the N_2O nitridation incorporated less nitrogen than NH_3. Moreover, although the high temperature (900 °C) annealing process may have changed the micro-structure of the poly-Si gate, the least V_{fb} shifts of PPHP and PHPP samples were not due to the above thermal effect on the poly-Si gate, since the Ar-annealed PPAP and PAPP samples, which had gone through the similar thermal process, had nearly the same V_{fb} shifts as those of the control samples.

Fig. 4 compiles the quasistatic C-V curves for the 900 °C 10 and 40 min annealed PPNP, PNPP, PPHP, PHPP and control samples. These curves can reveal the degraded integrity of the Si/SiO_2 interface [22] and the formation of the boron-related defect centers [9] caused by the boron penetration. All the C-V curves of the 10 min annealed samples, with the flatband voltage close to the theoretical value of 0.86 V for the pMOS capacitors with p^+ poly-Si gate, had good shapes. While for the 40 min N_2-annealed samples, the C-V curve of the control sample, with the mid-gap interface state density (D_{it}) increasing from the initial value of 8.3×10^9 to 5×10^{11} state/eV/cm^2, shifted positively and had a broadened shape. However, for the PHPP and PPHP samples with the NH_3-nitridized stacked gate, their C-V curves kept remaining in good shapes and had D_{it} values stay at a low value of about 1.2×10^{10} state/eV/cm^2 even for the long post-implant-annealing time.

Fig. 5 plots the breakdown fields (E_{bd}) with respect to the post-implant-annealing time at 900°C. With the increasing annealing time, E_{bd}'s decreased as the result of the degraded integrity of the gate oxide caused by the boron penetration. However, for PPHP and PHPP samples, their E_{bd}'s remained nearly unchanged due to the suppression on the boron penetration. Moreover, the indirect nitridation to the gate oxide of PPHP and PHPP also resulted in the much larger E_{bd}'s than

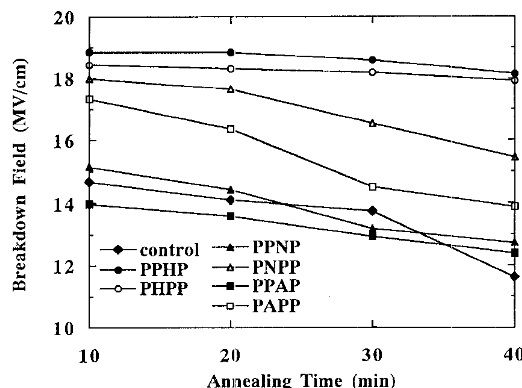


Fig. 5. The breakdown field (E_{bd}) of all the samples plotted with respect to the post-implant annealing time at 900 °C.

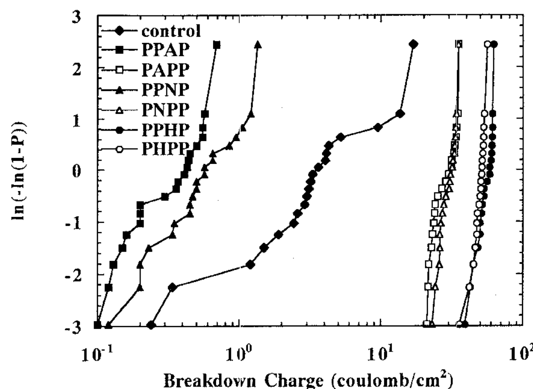


Fig. 6. The Weiball plots of the breakdown charge (Q_{bd}) of the 900 °C, 10 min annealed samples under the constant current (10 mA/cm^2) stress.

their corresponding counterparts. The same results are shown in Fig. 6, which compiles the Weiball plots of the breakdown charges (Q_{bd}) for the 900 °C, 10 min annealed samples. The Q_{bd}-distributions of PPHP and PHPP were higher and tighter than those of other samples.

When considering the thermal effect, it had been reported that the post-poly-annealing had negative effects on the electrical performance, such as the higher electron trapping rate and

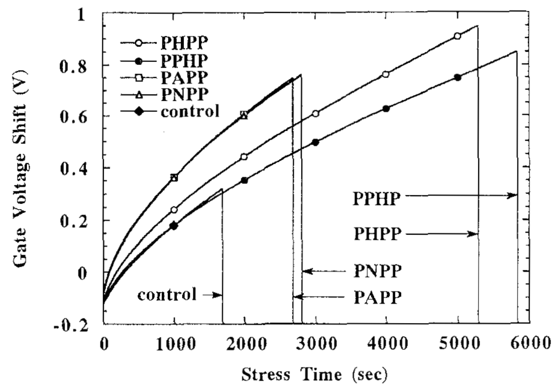


Fig. 7. The curves of the gate voltage shift (ΔV_g) versus the stress time under the constant current (10 mA/cm^2) stress for the 900 °C, 10 min annealed samples.

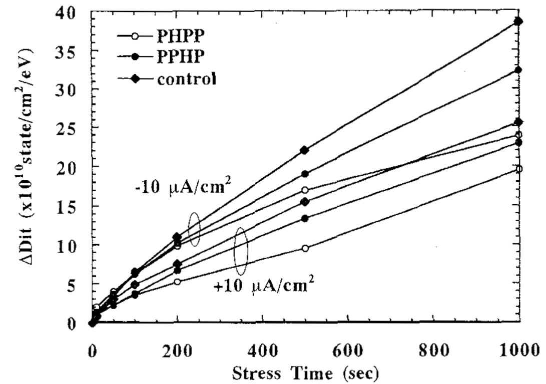


Fig. 8. The increase of the mid-gap interface state density ($\Delta D_{\rm it}$) versus the stress time under the constant current (+10 and −10 μA/cm^2) stresses for the 900 °C, 10 min annealed samples.

smaller $Q_{\rm bd}$ [23]. They were attributed to the fact that, after the poly-Si deposition, the gate oxide was sandwiched between the poly-Si gate and the Si-substrate, thus its volume change was inhibited when high temperature annealing was performed. This induced a stress in the oxide film, thus affected the integrity of gate oxide and degraded its electrical characteristics. For PPNP, as well as PPAP, post-poly-annealing was performed after poly I and poly II were deposited. The induced stress in the gate oxide resulted in smaller $E_{\rm bd}$'s and $Q_{\rm bd}$'s which are seen in Figs. 5 and 6 respectively. However, for PAPP and PNPP, their $E_{\rm bd}$'s and $Q_{\rm bd}$'s were larger than those of the control sample. This might be attributed by that, during post-poly-annealing, only one layer poly-Si film existed on the gate oxide, thus induced smaller stress. Moreover, the thermal process, like post-oxide-annealing, could also relax the stress in the gate oxide and improve the Si/SiO_2 interface flatness [23]. In addition, it is worth to be noted that, in spite of the negative effects of the post-poly-annealing, both PPHP and PHPP had better electrical characteristics than those of the control sample due to their nitridized gate oxide; and the slightly larger $E_{\rm bd}$ and $Q_{\rm bd}$ of the N_2O-annealed samples (PPNP and PNPP) than those of Ar-annealed samples (PPAP and PAPP) was believed to be resulted from the slight incorporation of nitrogen into the gate oxide [21].

Fig. 7 shows the incremental gate voltage shift under the +10 mA/cm^2 constant current stress. PAPP and PNPP had the same but higher electron trapping rate than that of the control sample due to the negative effect of post-poly-annealing [23]. However, for PPHP and PHPP, with the same thermal process on the poly-Si gate as that of PPAP and PAPP, indirect nitridation to the gate oxide reduced the electron trapping rate and much enhanced the times-to-breakdown. Moreover, although boron penetration degraded the integrity of the gate oxide, thus decreased the $Q_{\rm bd}$, the times-to-breakdown of PPHP and PHPP, even after 40 min annealing, were larger than that of the control samples annealed at 900 °C for 10 min [24].

Unlike the conventional NH_3-nitridized gate oxide, which has a larger electron trapping rate and a smaller $Q_{\rm bd}$ due to the un-intended hydrogen incorporation, PPHP had nearly the same electron trapping rate and much larger $Q_{\rm bd}$, as compared with the control sample of 900 °C, 10 min annealing. This was attributed to that the NH_3-nitridation of the poly-Si gate also slightly nitridized the underlying gate oxide while incorporating less hydrogen into it as the result of H-trapping at poly-Si grain boundaries [15] and the low pressure (120 mTorr) nitridation [16]. In Fig. 2(c), PPHP, PHPP and control samples all had nearly the same hydrogen profiles, except that the curve of PHPP had a slightly higher peak at the gate oxide region. The better electrical characteristics, such as smaller electron trapping rates and larger breakdown charges and fields, of PPHP than those of PHPP was believed to be due to less hydrogen incorporated into the gate oxide during the NH_3-nitridation for PPHP. However, although the H-related effects of PHPP were more severe than those of PPHP, both PPHP and PHPP had much larger $E_{\rm bd}$ and $Q_{\rm bd}$ than the control sample.

On the other hand, the conventional larger mid-gap interface state generation ($\Delta D_{\rm it}$) under stress for the NH_3-nitridized oxide [9]–[10] was also not observed for the NH_3-nitridized poly-Si gate samples of this study. Fig. 8 compiles the $\Delta D_{\rm it}$ data for PPHP, PHPP and control samples after they were stressed under +10 and −10 μA/cm^2 for different times. PPHP and PHPP samples had smaller $\Delta D_{\rm it}$ than the control samples. The incorporated nitrogen near the SiO_2/Si interfaces of PPHP and PHPP reduced the interfacial strain gradient and the amount of strained Si–O bonds [19]–[20]. Thus, the interface state generation by bond-breaking under electric stress was reduced, especially for PHPP which had more nitrogen at the SiO_2/Si interface [20].

IV. Conclusion

Based on the above results and discussions, it can be concluded that the NH_3-nitridized poly-Si gate can be quite effective in suppressing the boron penetration for BF_2^+-implanted pMOS. Because the created nitrogen-rich layers block the fluorine diffusion in the poly-Si film, the fluorine-enhanced boron penetration in the gate oxide is significantly reduced. Moreover, in spite of the negative effect of the post-poly-annealing, the indirect nitridation to the gate oxide significantly improves the electrical characteristics of the devices. Due to

the low pressure nitridation of this process and H-trapping at grain boundaries of the poly-Si film, the negative effects of the NH_3-nitridized oxide were not found in this work.

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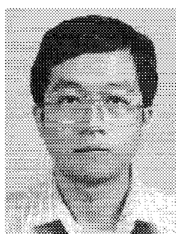

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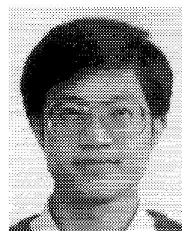
Chao Sung Lai (S'91), for a photograph and biography, see p. 331 of the February 1996 issue of this TRANSACTIONS.

Chung Len Lee (S'70–M'75–M'81–M'88–SM'92), for a photograph and biography, see p. 294 of the February 1996 issue of this TRANSACTIONS.

Tan Fu Lei, for a photograph and biography, see p. 294 of the February 1996 issue of this TRANSACTIONS.



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