

A carbon nanotube field effect transistor with tunable conduction-type by electrostatic effects

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Abstract

In this paper, we report a conduction-type-tunable carbon nanotube field effect transistor (CNT-FET) with double-gate structure (DG CNT-FET). In this study, a specially designed narrow top-gate is created to modulate the energy band in the middle region of a single CNT. In the proposed DG device structure, the top-gate and bottom-gate biases exhibit independent modulation behaviors. Depending on whether a positive or negative bias is applied to the top-gate, the CNT-FET can be operated in either n- or p-type conduction. Energy band diagram conducive to the physical mechanisms of the proposed DG CNT-FET device structure is proposed. Based on the proposed hypothesis, ambipolar CNT-FETs can indeed be converted to n- or p-type-like behaviors.

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1. Introduction

The single wall carbon nanotube field effect transistor (CNT-FET) possesses attractive properties indispensable for future nanoelectronics because of its superior high conductance and current carrying capability in a one-dimensional (1-D) nanoscale channel. For active device applications similar to the conventional FETs, the semi-conducting-type single-wall nanotube (SWNT) is more suitable than the metallic-type SWNT because in the former, the channel conductance can be controlled/modulated by the gate (voltage). It is also noted that if the CNTs are

multi-wall (MWNT) in nature, they will depict metallic-type electrical behaviors and will not be suitable for future nanoelectronics applications. In general, the CNT-FET acts like a p-type conduction device when it is exposed to air [1–5]. This phenomenon is ascribed to the absorbed oxygen between the interface of metal/SWNT, causing the pinning of Fermi level near the valance band [6–10]. Once the p-type CNT-FET is annealed in vacuum, the absorbed oxygen in the interface will be removed, and the CNT-FET is transformed from the pure p-type conduction to ambipolar or n-type conduction, depending on the annealing condition and/or the amount of remaining oxygen [10,13,15–17]. It is worth noting that if a device is ambipolar, it conducts either electrons or holes depending on the gate bias (In our study, this gate bias means bottom gate bias. For the conventional structure with a traditional

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Table 1
The electrical characteristics of device Type I and Type II

	The gate dielectric layer of bottom gate/deposition temperature/film thickness	The gate dielectric layer of top gate/deposition temperature/film thickness	Majority type of the devices on a wafer
^k	PE-oxide/400 °C/200 nm	PE-oxide/400 °C/200 nm	p-type ^a
Type II ^d	PE-oxide/400 °C/200 nm	PE-nitride/390 °C/200 nm	n-type ^b
^k	PE-nitride/390 °C/200 nm	PE-oxide/400 °C/200 nm	p-type ^a
Type II ^d	PE-nitride/390 °C/200 nm	PE-nitride/390 °C/200 nm	n-type ^b
Type I ^c	Thermal-oxide/400 °C/100 nm	PE-oxide/400 °C/200 nm	p-type ^a
^k	Thermal-oxide/400 °C/100 nm	PE-nitride/390 °C/200 nm	n-type ^b

^{a,b} Some of these devices contains Ambipolar-type characteristics.

^{c,d} The major differences between Type-I (Fig. 1d) and Type-II (Fig. 1e) lie in the separate bottom-gate design in Type-II structure and the different dielectric layers between the two types.

^k Data not shown.

single gate, the ambipolar phenomenon would be disastrous as the ambipolar phenomenon can not be easily suppressed). However, the electrical characteristics of the converted CNT-FETs vary widely and uncontrollably in this process, and the across-the-chip variations of FETs often widen and become intolerable after annealing.

Based on a former study of our group, we can manufacture air-stable n-type [12,13] or p-type CNT-FETs without any additional or complex annealing process (Table 1). However, we found that some ambipolar-type devices are always present in the Type-I devices due to process uniformity. And the Type-II devices always depict either n- or p-type characteristics rather than ambipolar-type, depending on the passivation layer deposited on the SWNTs. For practical applications, we must eliminate the ambipolar devices by converting them to n- or p-type devices as needed.

Nonetheless, it is difficult to alter the conduction-type of individual CNT-FET located on the same chip. In contrast, the novel DG CNT-FET structure proposed in this paper can provide a practical and reproducible method to form both n- and p-type-like CNT-FET devices as well as unipolar-type CNT-FET devices on the same chip [12,14]. The bias applied to the narrow top-gate plays the pivotal role of modulating the energy level within the CNT energy band. With the new approach, we can control the electrical characteristics of the CNT-FETs reliably without depending on complicated and often uncontrollable processes [15,16].

2. Experimental methods

Two double-gate (DG) device structures, i.e., Type-I and Type-II, were fabricated in this study. While Type-I DG device utilizes the substrate wafer as a universal bottom-gate, Type-II DG device employs a separate patterned Ti layer as its individual bottom-gate. More importantly, different dielectric layers (both oxide and nitride) were employed in both types of devices (Table 1), which allow us to study the effects of oxygen absorption behaviors on the devices. The key process flows for fabricating the two device types are described below:

A. Double gate (DG) CNT-FETs with substrate wafer as the universal bottom gate (Type-I)

The key process flow of the tunable Type-I DG CNT-FET structure with a universal substrate bottom-gate is shown in Fig. 1a–d. Briefly, a 100 nm silicon oxide was thermally grown on a 4-inch p-type silicon wafer. The silicon substrate wafer with a low resistivity of 0.02 Ωcm also serves as the universal bottom-gate (i.e., Si substrate acts as the back-gate). Then, a 150-nm Ti layer was deposited by RF sputter, patterned, and etched to serve as the source/drain metal, as shown in Fig. 1a. The spacing between the source and the drain electrodes is designed to be 2 μm. After the source/drain electrodes were patterned and etched, a prepared SWNT/Dimethylformamide (DMF) solution with the CNT density of 10,000/mm² (counted by SEM pictures manually, as shown in Fig. 1f) was spun on the wafer, as shown in Fig. 1b. Subsequently, a 200-nm low-temperature PE-CVD oxide was deposited at around 400 °C, as shown in Fig. 1c. Next, contact holes of the source/drain regions were etched in the MERIE (magnetic enhanced RIE) dry etcher using CHF₃ gas. Finally, a second 150-nm Ti layer was deposited by RF-sputter, patterned, and etched to serve as the top-gate, as shown in Fig. 1d. The top-gate length is designed to be either 0.6 μm or 0.8 μm, and is placed in the middle between the S/D regions. The patterned second Ti layer also served simultaneously as the pads for the source/drain contacts. In this way, a narrow top-gate was thus created on a bottom-gated SWNT FET, and the conduction type of the FET could be modulated by the bias applied to the narrow top-gate.

B. Double gate CNT-FETs with patterned Ti-layer as the individual bottom-gate (Type-II)

In order to strengthen the modulation of CNT-FET channel conduction, we modify the Type-I design (shown in Fig. 1d as described above) to that shown in Fig. 1e. It should be noted that a separate patterned bottom-gate is adopted while Type-I employs a universal bottom-gate. More importantly, while PECVD oxide was adopted as

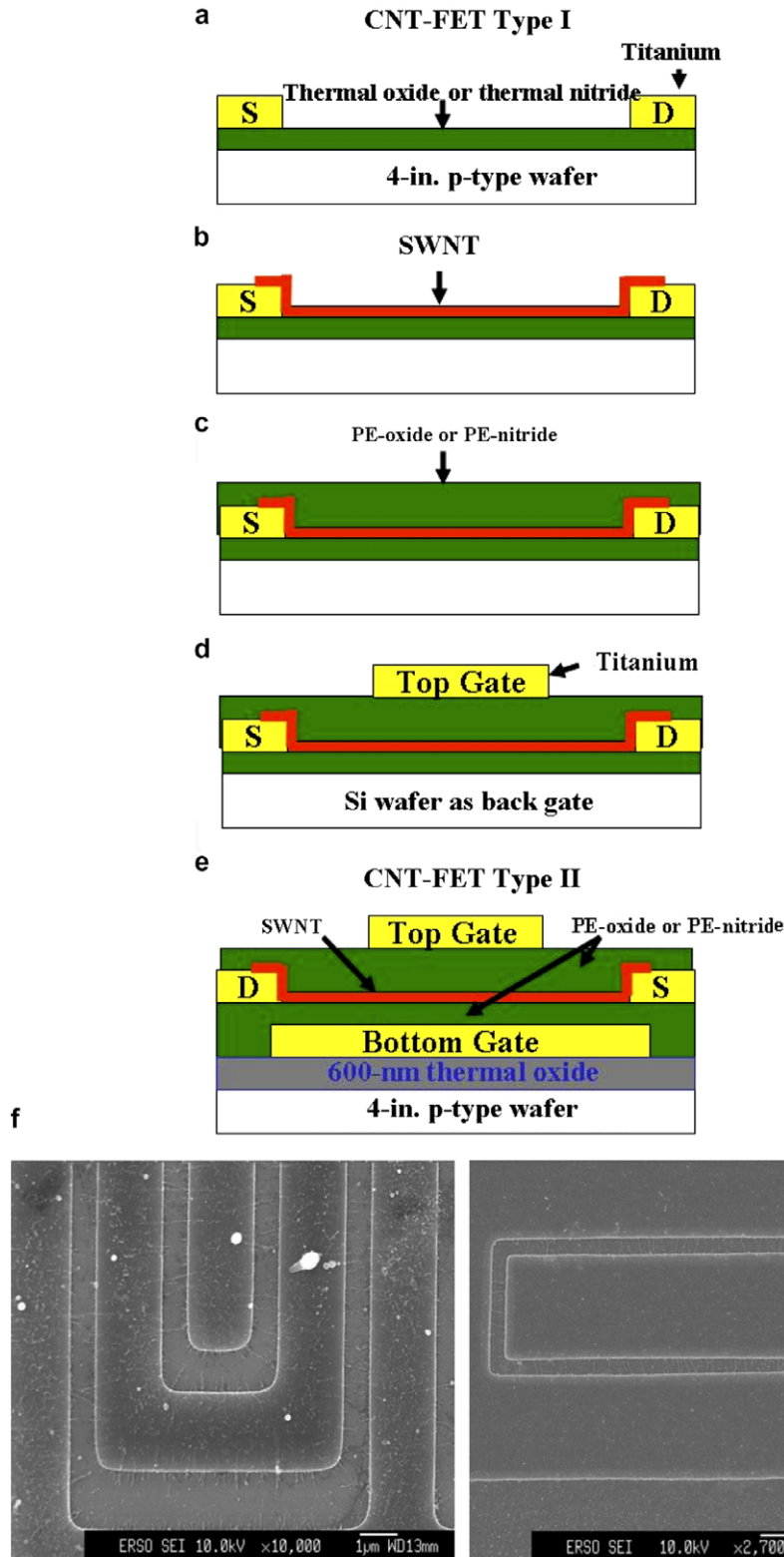


Fig. 1. Conduction-Type-Tunable CNT-FETs. (a–d) depict key process steps for Type-I structure, while (e) shows the cross-sectional view for Type-II structure, (a) 100 nm oxide or nitride was grown as the back-gate dielectric on p-type silicon wafer (0.02 Ω cm), followed by Ti deposition/pattern/etch to serve as the source/drain metal. (b) SWNT was spun-on the wafer in proper solution concentration. (c) Top-gate dielectric layer was deposited by low temperature PE-CVD (PE-oxide or PE-nitride). (d) second Ti layer was sputtered, patterned, and etched to serve as the top-gate. (e) Cross-sectional view of the new Type-II Double-gate (DG) CNT-FET structure. The major differences between Type-I (d) and Type-II (e) lie in the separate bottom-gate design in Type-II structure and the different dielectric layers between the two types. (f) Two of our SEM pictures are shown here for demonstration for SWNT/DMF solution spun on wafer.

the top-gate dielectric in Type-I devices, both PECVD oxide and nitride were tried as the top-gate dielectric layer in Type-II devices, which allowed us to study the effects of oxygen desorption on the CNT-FET behaviors. Briefly, to fabricate Type-II devices, a 600-nm SiO₂ field oxide layer was first grown by wet oxidation at 985 °C on the 4-inch p-type silicon wafer. Then, a 150-nm Ti layer was deposited by RF sputtering which was subsequently patterned and etched to serve as the bottom-gate metal. Afterwards, the wafer received a 200-nm low temperature PE-CVD oxide or nitride deposition process. A second 150-nm Ti layer was then deposited by RF sputtering, patterned, and etched to serve as the source/drain electrodes. Next, the SWNT/DMF solution was spun on the wafer, followed by another 200-nm PE-CVD dielectric deposition at around 390 °C (Table 1). Then, the contact holes of the source/drain regions were etched in the same MERIE dry etcher. Finally, a third 150-nm Ti layer was deposited by RF-sputtering, patterned, and etched as the top-gate. This patterned third Ti layer also served simultaneously as the pads for the source/drain contacts, while the position and dimension of the top-gate are nominally identical to those in Type-I structure. Afterwards, the wafers were annealed at 250 °C in the air to improve the metal/CNT contact. The final Type-II DG CNT-FET device structure is as shown in Fig. 1e. A commercial HP-4155A was applied to measure the I_d/V_g transfer curves of the CNT-FETs. The result will be discussed in the following sections.

3. Results and discussions

Since we have fabricated two types of DG CNT-FET device structures, the device characteristics of both structures will be discussed. For the first device structure (Type-I, as shown in Fig. 1d), the entire substrate wafer, which serves as the bottom-gate, was biased from -5 to +5 V at $V_{ds} = 1$ V; while the top-gate was biased from 0 to -12 V, at a step of -2 V. The resultant transfer curves (i.e., drain current versus bottom-gate voltage) of a Type-I CNT-FET are shown in Fig. 2. It can be seen that, for this particular Type-I CNT-FET, when the top-gate voltage is biased at 0 V, the CNT-FET exhibits ambipolar-type FET behavior. However, when the top-gate is biased toward more negative value (e.g., from 0 to -12 V), the transfer characteristics change significantly. Specifically, for a given positive bottom-gate voltage, the drain current I_{DS} decreases as the top-gate voltage V_{tg} decreases from 0 to -12 V, while I_{DS} for a given negative bottom-gate voltage increases in stead. It can be seen that when the top-gate is decreased to -12 V, the conducting channel under positive bottom-gate voltage is effectively pinched off, while the channel under the negative bottom-gate voltage is enhanced, as shown in Fig. 2. In a word, ambipolar-type CNT-FET is stepwise converted to p-type CNT-FET by simply changing the top-gate voltage. In Fig. 5c, it can be seen that a Type-I ambipolar device could be converted to n-type CNT-FET by applying a positive top-gate voltage.

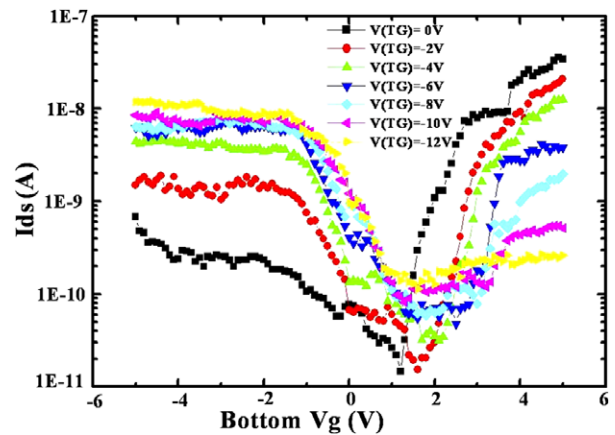


Fig. 2. Transfer characteristics (drain current versus bottom-gate voltage) highlighting that generic ambipolar-type CNT-FET can be stepwise converted to p-type CNT-FET by simply varying the top-gate bias at $V_{ds} = 1$ V.

A hypothesis based on the CNT-FET band gap structure is proposed to gain insights into the physical mechanisms of the conduction-type-tunable Type-I DG CNT-FET structure shown in Fig. 1d. It is worth noting that many generic (i.e., without top-gate bias) Type-I CNT-FET devices in our study exhibit ambipolar behaviors, rather than the n-type-only behaviors. This trend in Type-I devices is believed to be the result of using PECVD oxide as the top-gate dielectric. This is because at the process temperature of around 400 °C, even though high enough to desorb oxygen from CNT, a few oxygen atoms could be driven back to CNT during the PE-CVD TEOS oxide process [10,13,14]. We therefore choose a generic ambipolar, rather than the n-type-only, CNT-FET to illustrate the proposed hypothesis. Its transfer characteristics (drain current versus bottom-gate voltage) are as shown in Fig. 3a.

There has been increasing evidence to support that the interface behaves as a Schottky contact at the source and drain regions [10,11,13,15–17]. As shown in Fig. 3b, when the bottom-gate voltage is floating, a few holes can be conducting. However, as shown in Fig. 3d, when a positive bottom-gate voltage (with the top-gate floating) is applied to the CNT-FET, the energy band corresponding to the middle CNT channel region will be pulled down, decreasing the effective electron tunneling barrier. As a result, more electrons can tunnel through the interface barrier, and the electron current increases. On the other hand, as shown in Fig. 3c, when a negative bottom-gate bias is applied (with the top-gate still floating), the energy band corresponding to the middle CNT channel region will be raised, so the holes can drift through the interface barrier easily. Consequently, the DG CNT-FET with the top-gate floating exhibits ambipolar characteristics.

Fig. 4 shows the band diagram when the effect of the top-gate bias is superimposed to our DG CNT-FET. As mentioned above, for a given positive bottom-gate, the energy band will be pulled down, and allows the electrons

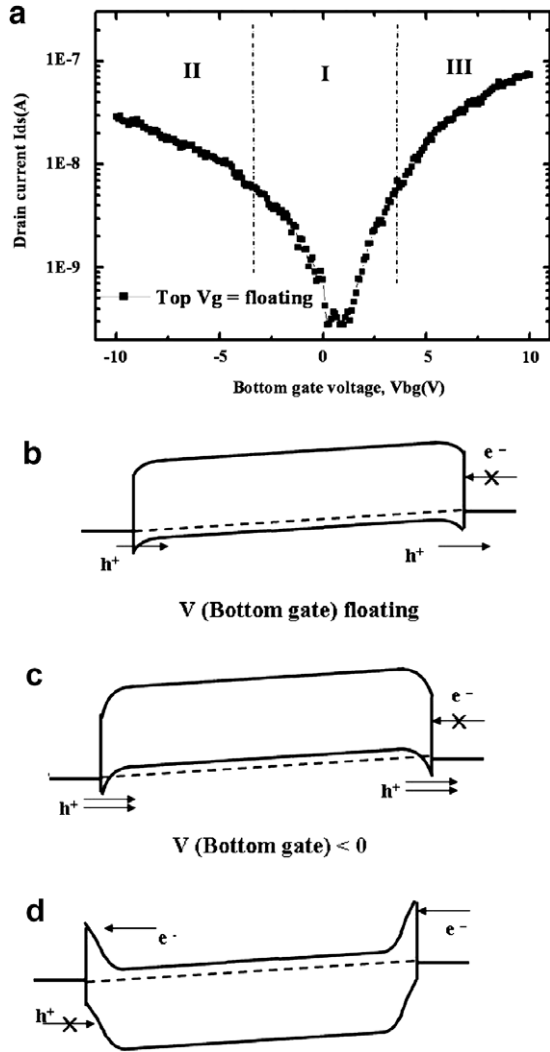


Fig. 3. (a) Transfer characteristics (i.e., drain current versus bottom-gate voltage) with floating top gate showing ambipolar behaviors. (b) Band diagram with floating top-gate and bottom-gate, only a few holes can drift through the interface Schottky Barrier, corresponding to the region, of (a). (c) Band diagram with floating top-gate and negative bottom-gate, the hole will flow easily through the interface Schottky barrier, corresponding to the region II of (a). (d) Band diagram with floating top-gate and positive bottom-gate, the electron will tunnel easily through the interface Schottky barrier, corresponding to the region III of (a).

to tunnel through easily. By simultaneously applying a top-gate voltage to the DG CNT-FET, the energy band of CNT region directly under the top-gate electrode is altered. Specifically, when a positive bias is applied to the top-gate, the energy band of CNT region directly under the top-gate electrode is pulled further down, while the barrier at the metal-CNT interface remains unchanged, as shown in Fig. 4a. The current, resulting from electron flow, therefore remains essentially unchanged. If a large positive top-gate voltage is applied, the down-bending potential profile will slightly accelerate the electron flow in the CNT due to the barrier lowering effect, and the drain current will increase slightly. However, when a negative bias is applied to the top-gate, the energy band of CNT region directly

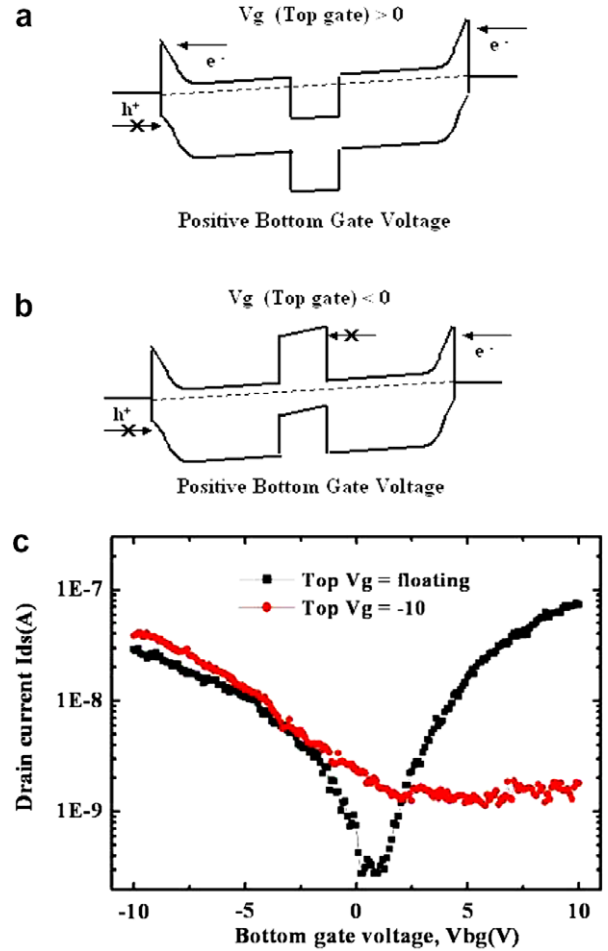


Fig. 4. By varying the top-gate voltage from positive to negative in the presence of positive bottom-gate voltage, the energy band within the CNT will be shifted as follows: (a) With positive top-gate, the electron flow will act as if no top-gate bias is applied. (Even if a large positive bias is applied to the top-gate, the down-bending potential profile will only slightly accelerate the electron flow in the CNT due to the barrier lowering effect, and the drain current will increase only slightly.) (b) With negative top-gate, the electron flow will be suppressed (red solid circle line), and the current level will drop down effectively, (c) Transfer characteristics corresponding to (b). (For interpretation of the references in colour in this figure legend, the reader is referred to the web version of this article.)

under the top-gate electrode is pulled up instead, as shown in Fig. 4b. Since the extra electron barrier at the conduction band is created within the CNT region itself, the electron flux inside the CNT is effectively blocked. Therefore, even though the initial CNT-FET shows ambipolar behaviors, the electron flow channel is effectively blocked off by the negative top-gate bias. At the same time, the hole current at the negative bottom-gate region remains essentially unchanged because the extra barrier exists at the conduction band only (Fig. 5a). The CNT-FET now behaves like a p-type conduction, as shown in Fig. 4c ($V_{ds}=1V$). The more negative the top-gate bias is, the lower the conducting current can be obtained at a given positive bottom-gate bias. This is consistent with the trend shown previously in Fig. 2. This explains why the Type-I DG CNT-FET will

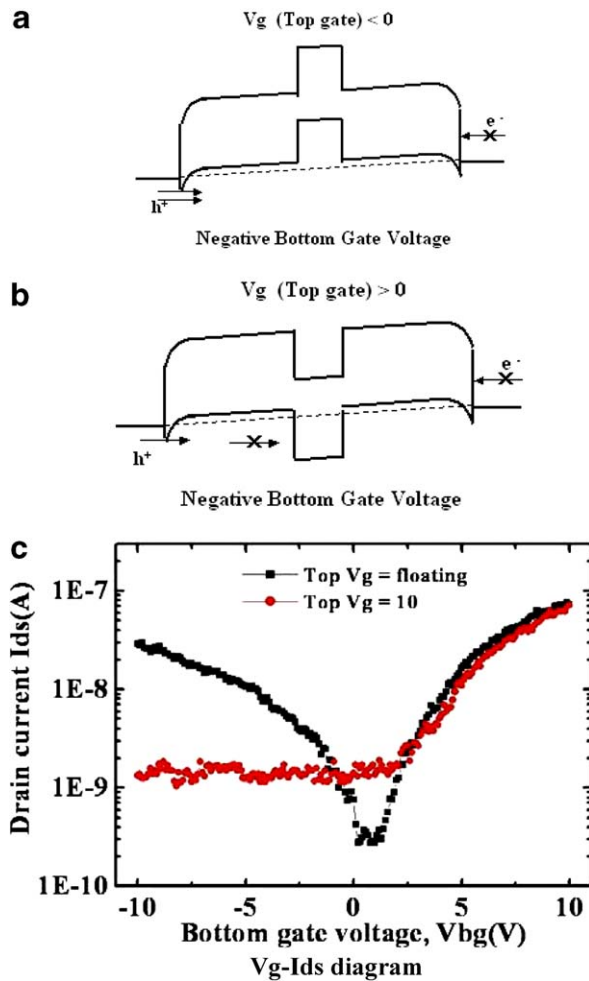


Fig. 5. By varying the top-gate bias from negative to positive in the presence of negative bottom-gate voltage, the energy band within the CNT will be shifted as follows: (a) With negative top-gate bias, the hole current will act as if no top-gate bias is applied (When the top-gate voltage is at a much more negative bias, the barrier lowering effect occurs at the drain side, and results in a significant increase of hole-tunneling). (b) With positive top-gate bias, the hole flow will be suppressed (red solid circle line), and the current level will drop effectively. (c) Transfer characteristics corresponding to (b). (For interpretation of the references in colour in this figure legend, the reader is referred to the web version of this article.)

behave like p-type FET under the negative top-gate bias, even the generic Type-I CNT-FET (i.e., the device without the top-gate modulation) depicts ambipolar behaviors.

Fig. 5 shows the case for the negative bottom-gate bias. When a negative bias is applied to the top-gate simultaneously, the barrier lowering effect occurs at the drain side which results in a significant increase of hole-tunneling, as shown in Fig. 5a [18]. However, when a positive bias is applied to the top-gate, as shown in Fig. 5b, the hole flux is blocked. This will suppress the conductance of holes, and the generic ambipolar CNT-FET now depicts n-type FET characteristics, as shown in Fig. 5c ($V_{ds} = 1$ V).

Since for the mainstream CMOS circuit applications, both p- and n-type MOSFETs are called for on the same chip. It is necessary to form n-type, in addition to p-type

CNT-FETs, on the same chip for the complementary circuits. Several approaches have been previously reported to form n-type CNT-FETs by employing complex doping processes (adopting alkali metals) [19–21] or thermal/electrical annealing processes [10]. These approaches, however, require extra processing and masking steps to convert generic p-type CNT-FETs in vacuum or in the inert gas. In contrast, no extra annealing steps are needed to form air stable n-type CNT-FETs [12,13] selectively using the DG CNT-FET structure proposed in this study. As mentioned previously, for the Type-II structure both PE-oxide and PE-Nitride were tried as the top-gate dielectric. By using PE-Nitride as the top-gate dielectric, the process temperature of the deposition would be high enough to simultaneously remove the oxygen atoms from the CNT or CNT/metal interface in the PE-CVD deposition chamber. So we can fabricate n-type CNT-FETs by selectively converting generic Type-II structures without extra processing steps. This is because when the oxygen atoms are removed during the PE-CVD process, the Fermi-level in Type-II structure moves away from the valence band and becomes closer to the middle of the bandgap, compared to that of Type-I structure shown already in Fig. 3b. So by applying a negative bias to the bottom-gate of Type-II CNT-FETs selectively, the hole cannot tunnel through the energy barrier efficiently, and we could selectively create n-type CNT-FETs on the chip.

Although we can create n-type CNT-FETs selectively, how to control the uniformity of electrical characteristics of these devices remains an open question. Since the generic Type-I devices tend to depict ambipolar behaviors, the electrical characteristics of the Type-I devices, however, can be tuned to either n- or p-type behaviors precisely, according to the hypothesis described above.

As shown in Fig. 6a, the initial transfer characteristics of the Type-II CNT-FET depict pure n-type behavior with $I_{max} = 63.2$ nA at $V_{bg} = 10$ V and $V_{ds} = 1$ V, representing on/off ratio of greater than 10^5 . Depending on whether a positive or negative bias is applied to the top-gate, the Type-II CNT-FET will behave differently. When the top-gate is negatively biased, the drain current of Type-II CNT-FET decreases, and reaches complete pinch-off when the top-gate becomes more negative than $V_{tg} = -10$ V. On the other hand, the drain current increases slowly as the top-gate increases toward more positive value. These trends could again be explained by the proposed hypotheses shown previously in Figs. 4 and 5. At $V_{tg} = -10$ V, the down-bending energy band in the Type-II CNT FET, similar to that shown in Fig. 4b for the Type-I structure, is pulled up instead in the region directly under the top-gate, which effectively blocks the electron flow. On the contrary, when a positive top-gate is applied, the down-bending potential profile, similar to that shown previously in Fig. 4a for Type-I structure, will slightly accelerate the electron flow due to the barrier lowering effect, and the drain current increases slightly, as shown in Fig. 6b. It is noticed that the current in Fig. 6a decreases in the negative bottom-

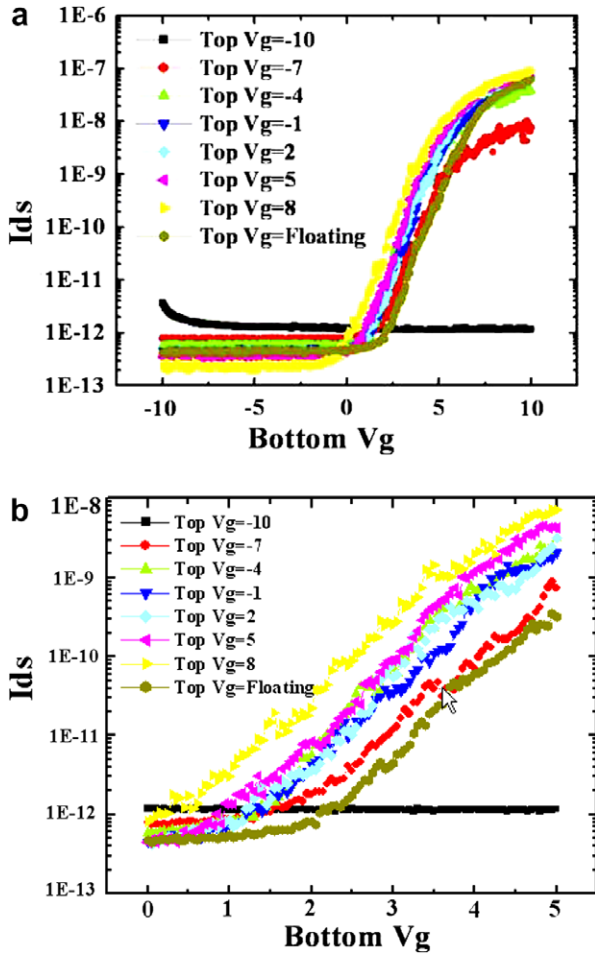


Fig. 6. (a) According to the hypothesis proposed in Fig. 4, n-type behavior in Type-II CNT-FET can be fully suppressed by applying negative bias to the top-gate. In other word, the on/off ratio can be controlled at will. (b) A bloated view of (a) with bottom-gate varying between 0 and 5 V. With positive top-gate bias, the down-bending potential profile shown in Fig. 4a will slightly accelerate the electron flow due to the barrier lowering effect, and the drain current will increase slightly.

gate region when the top-gate voltage increases. This is because according to Fig. 5b, when the top-gate voltage becomes more positive, the energy band directly under the top-gate will be bent down further, and this down-bending potential will block the hole tunneling.

This hypothesis could also be applied to explain the suppression of the p-type behavior in Type II devices (Fig. 7). Fig. 6 shows a generic n-type Type-II device with its n-type characteristics being gradually suppressed under negative top gate biases, while Fig. 7 depicts a generic p-type Type-II device with its p-type characteristics being gradually suppressed under positive top gate biases. These trends are consistent with our proposed hypothesis.

By resorting to DG CNT-FET structure, V_{th} of the device can be modulated by varying the biases of the top-gate and the bottom-gate. When the roles of the top-gate and the bottom-gate are reversed, the transfer curves (drain current versus top-gate voltage) of DG CNT-FET are plot-

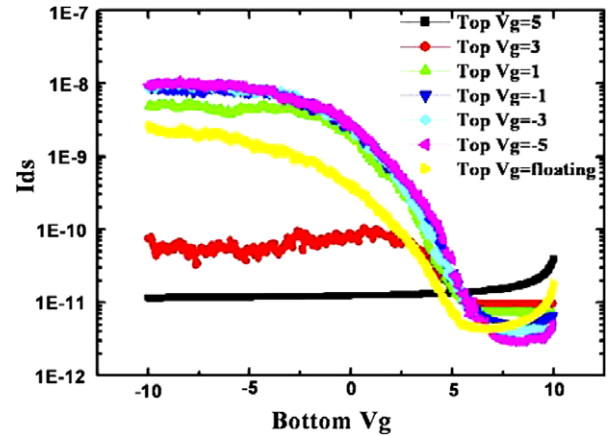


Fig. 7. According to the hypothesis proposed in Fig. 5, p-type behavior in Type-II CNT-FET can be fully suppressed by applying positive bias to the top-gate. This figure shows stepwise conversion by simply varying the top-gate bias at $V_{ds} = 1$ V.

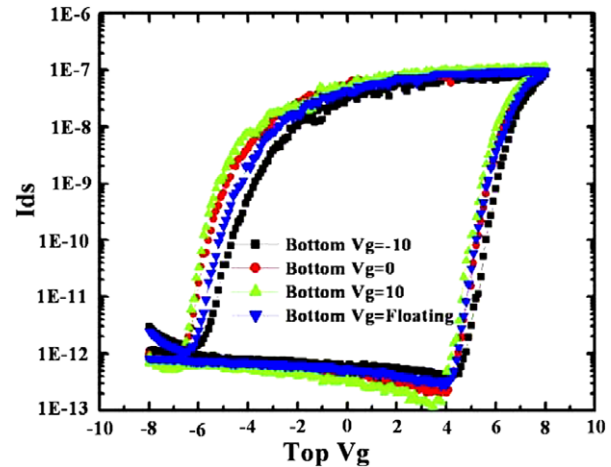


Fig. 8. The top-gate can be used to shift the Fermi-level of the entire CNT. This feature can be utilized to adjust V_{th} of DG CNT-FETs precisely.

ted in Fig. 8. It can be seen that when the bottom-gate is floating and the top-gate voltage is swept from -8 to $+8$ V and back to -8 V, a pronounced hysteresis loop is observed [22–25]. In our work, four kinds of bottom-gate and top-gate dielectric layers (i.e., PE-oxide, PE-nitride, thermal-oxide, and thermal-nitride) were studied, and the hysteresis phenomenon persists. Here in Fig. 8 we only depict the data with PE-nitride as both the bottom- and top-gate dielectric layers. When $V_{bg} > 0$ V, by sweeping from $-V_{tg}$ to $+V_{tg}$, the corresponding energy band switches from that shown in Fig. 4b to Fig. 4a; and by sweeping from $+V_{tg}$ back to $-V_{tg}$, the corresponding energy band switches from that shown in Fig. 4a back to Fig. 4b. The energy band shift that occurs during V_{tg} sweeping accounts for the observed hysteresis loop observed in Fig. 8. Similarly, When $V_{bg} < 0$ V, by sweeping from $-V_{tg}$ to $+V_{tg}$, the corresponding energy band

switches from that shown in Fig. 5a to b, and vice versa. The corresponding shift in energy band between the two cases (i.e., from Fig. 4b to a, compared to that from Fig. 5a to b; and vice versa) is essentially identical. This explains why the hysteresis loops between the curves with either positive or negative bottom-gate biases are essentially identical, as shown in Fig. 8.

4. Conclusion

In this paper, a novel double gate structure is proposed to control the conducting type of the CNT-FET in order to achieve unipolar-type devices without resorting to complex processes. Our results show that ambipolar-type CNT-FET can be converted to n- and p-type CNT-FETs by controlling the biases applied to the top- and bottom-gate electrodes. Our approach opens the possibility of creating specific type of CNT-FETs with well-controlled characteristics. This is crucial for CMOS circuits as well as certain circuit applications, such the detector applications where p-type CNT-FET sensor with high on/off current ratio is required for negative charge enzyme system [26]. In the proposed DG CNT-FET structure, the I - V characteristics of each random device can be well-tuned to the same level, and the ambipolar character of CNT-FETs can be annihilated. Furthermore, the threshold voltage of CNT-FETs can be possibly adjusted by using different bottom-gate and top-gate biases. These features make the new structure especially promising for applications in future ultrahigh sensitive sensors.

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